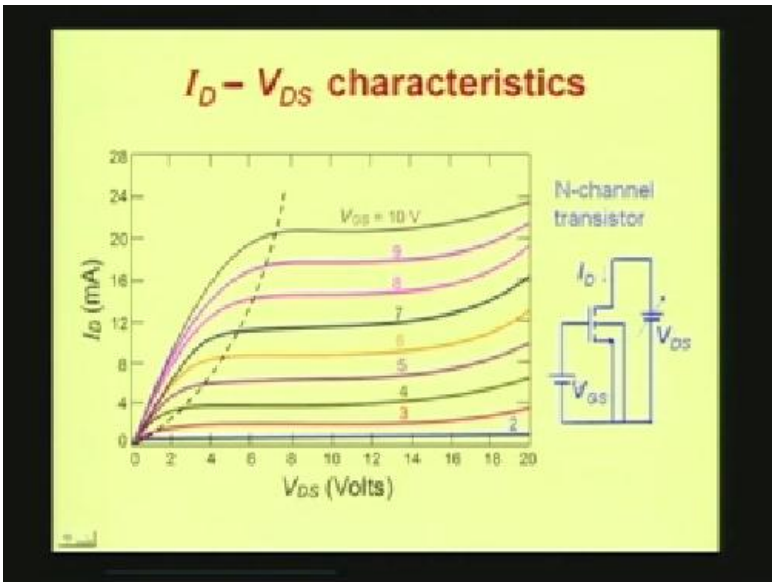
Solid State Devices
Dr. S. Karmalkar
Department of Electronics and Communication Engineering
Indian Institute of Technology, Madras
Lecture - 38
MOS Field Effect Transistor

In this lecture we will begin a new topic namely the Metal-Oxide-Semiconductor Field Effect Transistor.

(Refer Slide Time: 01:16)

Now there are a number of different field effect transistors such as junction field effect transistor, the metal semiconductor field effect transistor and in recent times there have been other field effect transistors such as hetero-structure field effect transistor and so on. The MOSFET is one of the primary field effect transistors. So we will discuss about this particular device in detail which is based on the operation of the MOS junction or capacitor. Let us see the goal of our discussions on this topic.

(Refer Slide Time: 08:10)



First we will try to explain these current voltage characteristics. These characteristics are similar to the output characteristics of a bipolar transistor. The only thing is, here the nomenclature for the terminals is a little different from that of a bipolar transistor. For example, look at the biasing arrangement shown here. This is a symbolic representation of the MOSFET. We will explain why this symbol is used to represent the MOSFET device. But before we do that let us understand the various terminals.

This is the so-called the drain terminal which is analogous to the collector terminal of the MOS transistor. The input terminal is the gate which is analogous to the base of the bipolar transistor. This terminal is the source which is analogous to the emitter of the bipolar transistor. Now you see one difference between bipolar transistor and the field effect transistor that you also have what is called the bulk or the substrate terminal which was not there in bipolar transistor. This fourth terminal is the so-called bulk or the substrate terminal. You can apply a voltage between this bulk and the source terminal and that will introduce what we call as the body effect, something that was discussed in the context of MOS capacitor. So, though we can apply a voltage between this terminal that is bulk and the source in this particular biasing arrangement the voltage applied has been 0. So bulk to source voltage or substrate to source voltage here is 0.

These characteristics which you see on the left hand side here is the place you are plotting the drain current as a function of drain to source voltage So what is being done here is that you keep the gate to source voltage constant but more than the threshold voltage then you get a current I_D, then you vary the V_{DS} from 0 to large values to see how I_D changes keeping V_{GS} constant. When you do that you trace one of these particular family of curves. For example, this curve is traced by keeping V_{GS} is equal to 3V and then varying V_{DS} from 0 to 20V. Then you change your V_{GS} to different values maybe 4V and again sweep the V_{DS} and that is how you get this entire family of curves.

Now it is to be noted that these characteristics are shown for an N-channel transistor. So N-channel transistor is a device in which the current is carried by electrons. In such a transistor the drain current is into the drain terminal and the drain to source voltage is positive therefore

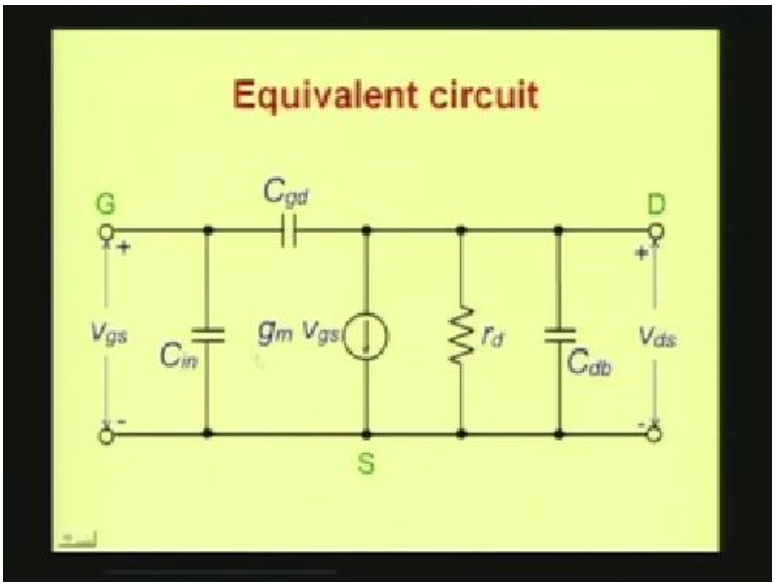
in this case you have positive currents and positive voltages. You can see very clearly that there are two regions of operation that can be identified here which are separated by this dotted line which is somewhat analogous to the bipolar transistor. The only difference is that this region to the left of the dotted line which was called the saturation region in the context of bipolar transistor is given a different name here in the MOS transistor this is called the ohmic region or the resistive region. This region is much wider than what you had in bipolar transistor.

In bipolar transistor this region was about 0.7V or something like that whereas here you can see that the region goes on increasing from low V_{GS} to high V_{GS} and it is of the order of a few volts. Beyond this dotted line to the right of this is what you have a region where the current is almost constant and analogous to the bipolar transistor. So here this is the so-called active region. In the context of MOS transistor this region is also referred to as the saturation region because the current saturates. So the saturation region in bipolar transistor means the region to the left of the dotted line whereas in the MOS transistor it means the region to the right of the dotted line.

We will also see why this kind of confusion exits about the nomenclature. In these characteristics we have not shown the breakdown region something we had shown for the bipolar transistor we are not showing in the MOS transistor. Our main purpose will be to explain these DC characteristics. Now, from the DC characteristics you can also get the small-signal equivalent circuit because when you use the transistor as an amplifier you are going to operate it in small-signal condition. The equivalent circuit for that particular case that is for small-signal operations is very similar to the hybrid-pi equivalent circuit of the bipolar transistor.

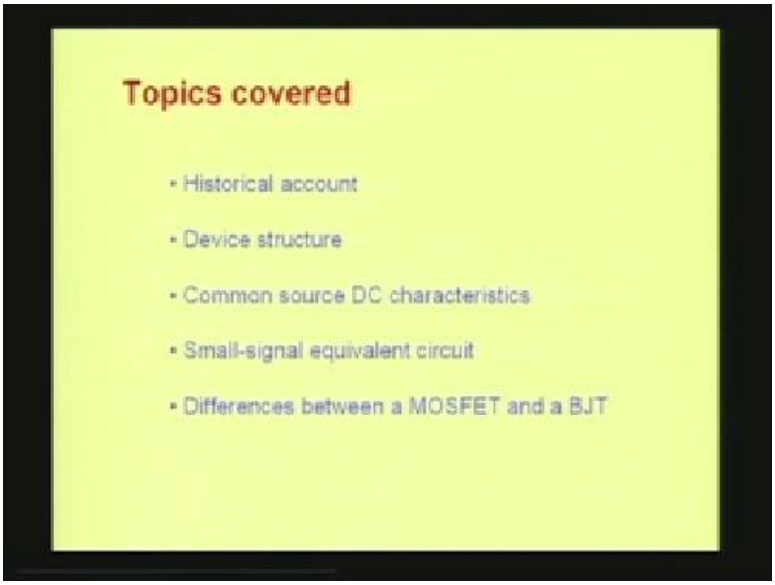
Now you do not have h-parameter equivalent circuit for the MOS transistor. This is because if you look at the diagram here you really do not have any input current voltage characteristics for this device because there is no DC gate current flowing in the device and the gate is isolated from the channel through which the current flows. So the channel flows from the drain to the source along this line and this channel is isolated from the gate. Therefore there is no DC gate current so you do not have input characteristics of input current versus input voltage. That being the case you do not have a parameter like the beta of a bipolar transistor which is a current gain from the base of the bipolar transistor to the collector of the bipolar transistor. So, output current by input current that is what is beta. Whereas in a MOS transistor there is no input current and the input current is 0 for the DC case. Therefore we do not have an h-parameter equivalent circuit and you only have an equivalent circuit which looks somewhat like the hybrid-pie equivalent circuit of the bipolar transistor. Let us see what this equivalent circuit looks like.

(Refer Slide Time: 09:45)



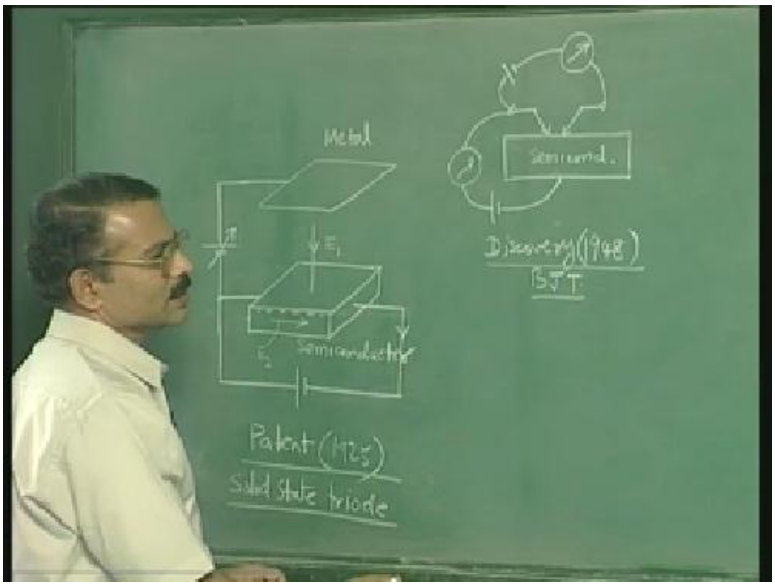
The equivalent circuit looks like this. Here this is also a trans-conductance based equivalent circuit so MOS transistor for small-signal purposes is a trans-conductance amplifier. And similar to the bipolar case you have the capacitances at the input then you have a capacitance here between the input and output, here gate is input drain is output and source is the common terminal in analogy to the common emitter bipolar transistor case where emitter is the common terminal base is the input terminal and collector is the output terminal. Then you have a resistance here between drain and source and you also have a capacitance. You do not have a resistance at the input and that is the only difference. So we will try to explain the various parameters of this equivalent circuit. To do this we will be proceeding in the following manner. So here is a very brief outline of our discussion on MOS field effect transistor.

(Refer Slide Time: 10:26)



First we will give a very brief historical account of how this device has come into existence. Then we will consider the device structure and how it is fabricated. Then we will see the common source DC current voltage characteristics. Then we will see the small-signal equivalent circuit and finally we will see the difference between the MOSFET and a BJT. So let us begin with a brief history of how this device came into being. Let us recall the lecture on the bipolar junction transistor which discuss with the history of bipolar junction transistor.

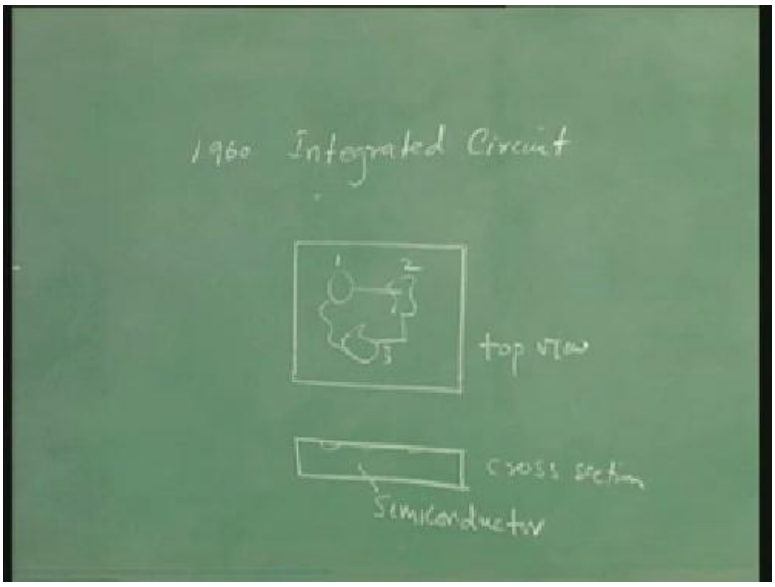
(Refer Slide Time: 18:45)



If you recall we talked about a patent solid state triode as early as 1925 wherein you had a semiconductor block here and a metal here. This was a diagram in the patent and the idea was that if you apply a voltage to the metal with respect to semiconductor a field will be created which will attract carriers to the surface of the semiconductor and therefore modulate the surface conductivity. Now in this region of enhanced carrier concentration the conductivity will be small and therefore if you apply a voltage between these two points and superimpose a longitudinal field here in the semiconductor then this field with carry the current from positive terminal to the negative terminal and this current can therefore be modulated by this electric field which will change the concentration of carriers here.

So modulation of this current in this direction by a field in this direction was the idea of a solid state triode or a solid state amplifier. In fact this is essentially the field effect transistor idea. Then when people started working on this idea for about two decades they could not make this device work then they tried to realize and practice and they were analysing the reasons for their failure. They were doing an experiment on a semiconductor block and that put two probes in close proximity. And when they monitored their currents in these two circuits they found this current was linked to this current and that is how they discovered the basic transistor action of the bipolar junction transistor. This was in 1948. After the discovery of this transistor whose principle was much different from the principle of the solid state triode people forgot about this solid state triode as such because this was a very good amplifying device they discovered. So they went on with it until in 1960 another new idea was invented and that was the Integrated Circuit.

(Refer Slide Time: 18:42)



In fact this particular idea of Integrated Circuit is supposed to be a very revolutionary idea of this of the previous century. There were two inventors Kilby and Noyce of which Kilby was given a Noble prize about 40 years later in the beginning of this century for this idea. In fact he was the only engineering to have been given a Noble prize in Physics because this particular engineering invention of the Integrated Circuit in which later on people developed the idea of miniaturization of the various devices to integrate more and more devices on the same plane. And this miniaturized device has given rise to lot of new Physics. So very low dimensional device has given rise to lot of new Physics because of which the inventor of the Integrated Circuit was given a Noble prize because his idea has lead to so much of new Physics and so much of new research related to various physical phenomena.

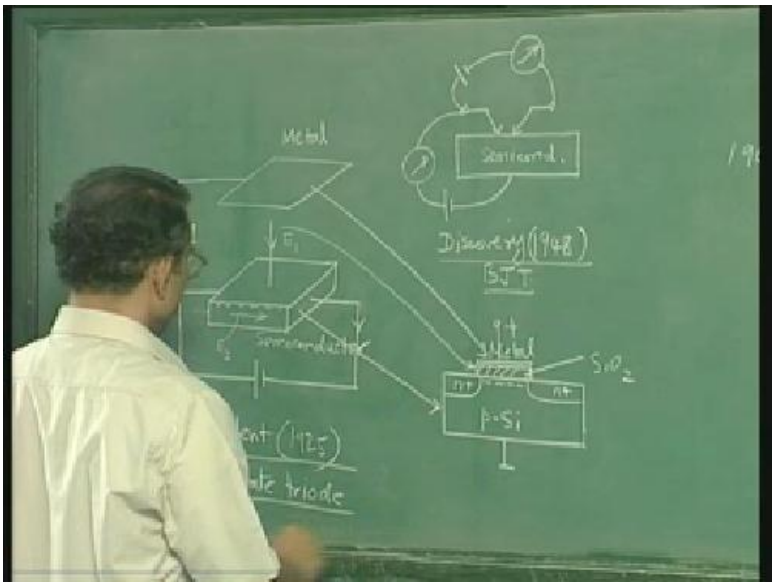
Coming back to the Integrated Circuit the idea was that you have a plane in which you can make a number of different devices and interconnect them. Now, this is the same idea as the idea of a printed circuit board. That is what you do on a printed circuit board you put different devices and then you interconnect them, solder wires and so on. Here it was exactly an analogy to the idea of printed circuit board but here what was suggested was that all these devices we made simultaneously on a piece of semiconductor. So this is the top view and this is a cross section. So it is different devices being made simultaneously in this semiconductor and then they will also be interconnected simultaneously.

In other words, it is a simultaneous processing of all the devices to build a circuit on a single plane. This concept is different from the concept of PCB where you make different devices discrete devices individually then you put all these devices and then you put the connecting wires. In contrast to this idea here in Integrated Circuit you are going to put all the devices at the same time and then all the devices will be interconnected at the same time. So the various processes related to thousands of devices take place at the same time that is the idea of Integrated Circuit. And the inventor proposed that if you adopt this approach to make circuits then your size will be small and the reliability will be very high and also the speed of the operation of the circuit and so on can be increased tremendously.

So, once this idea of Integrated Circuit was proposed then it was found that the bipolar junction transistor was not so much suitable for this particular idea. Though now-a-days you do have Integrated Circuits based on bipolar transistors but definitely the MOS field effect transistor is more suitable for integration and for Integrated Circuit. That is why the most popular Integrated Circuit is the CMOS that is the Complimentary MOS device. That is when people realized that if you try to the implement this idea of the solid state triode directly in a semiconductor and if you are successful in it that particular device will be more suitable than the BJT for integration.

Now because of a lot of work that went on the BJT people had perfected the making of an insulator on silicon. This process of making an insulator on silicon was perfected which was the key to the realization of this particular solid state triode. And so this particular device structure called the MOSFET then became realizable after 1960 that is after about an additional decade of work on this particular device by that time the Integrated Circuit was invented. The idea of the solid state triode could be realized in practice. So the idea was realized in practice as follows. This was the structure that was analogues to this solid state triode which was realized in practice.

(Refer Slide Time: 20:55)

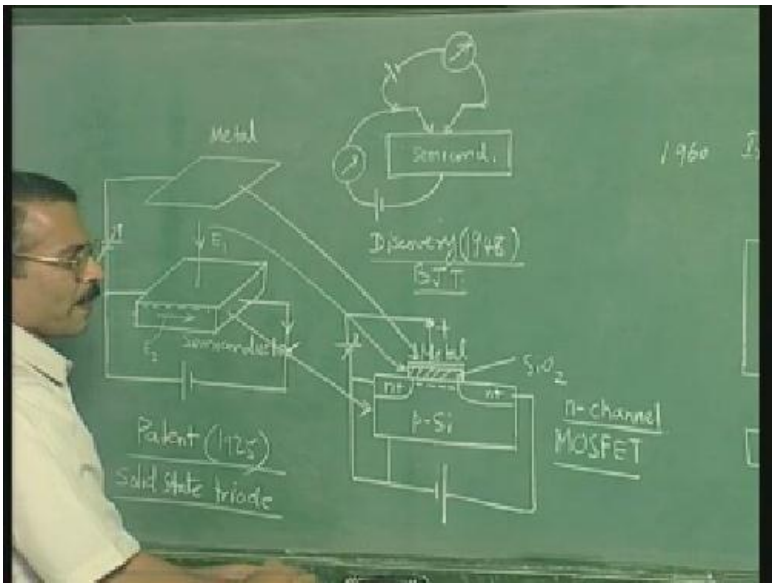


So you have silicon semiconductor and on this, you grow silicon dioxide layer which is of high quality. The silicon dioxide silicon interface is very good provided you may maintain certain conditions. This we had discussed little bit in the context of MOS capacitor. On the top of this you put a gate, a metal and then here you have electrodes which are made using doped regions. So you let us say we have p-type silicon to start with.

Now you can see the analogy between this figure and this device. So this semiconductor is this, this metal is this and here between the metal and the semiconductor there was vacuum so instead of vacuum you have this insulator silicon dioxide directory. You need contacts on the both sides these are the contacts on both sides of the semiconductor. Now what happens is, when you apply a voltage to this particular terminal with respect to the substrate let us assume the substrate to be common. Then electrons are attracted. Let us say you apply positive voltage, you know from the theory of MOS capacitors that electrons will be attracted

and you will create an inversion layer of electrons here. This inversion layer can be used for transferring current from this terminal to this terminal. In fact if you want to see an analogy between this and this then this voltage is applied with respect to this instead of the substrate so you could do that here.

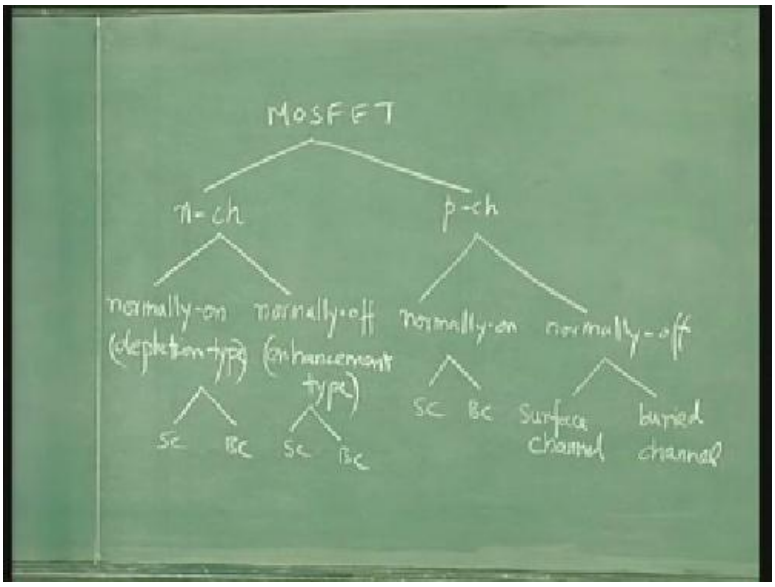
(Refer Slide Time: 23:01)



You can apply a voltage here between these two and then you have to apply a voltage between these two so in fact here the voltage is with this polarity and that is how you get a current. And you modulate this current between these two by changing this particular voltage. The substrate is also there, in fact in practice the substrate is also connected to a terminal. So either this is grounded which means it will be connected here like this or you can connect a power supply between this and this. But this is the device which is a direct translation of this idea. So this was the so-called MOS field effect transistor.

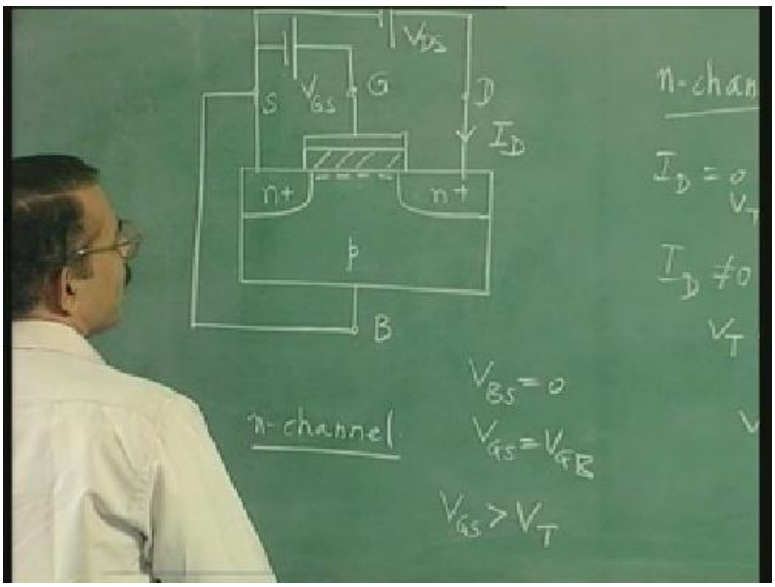
After 1960 people quickly started concentrating on the MOS field effect transistor that is this particular device and they perfected it and then started an era of different kinds of circuits on this particular device. Now let us see the kinds of MOSFET that are possible. Once we that this is the basic structure clearly here the current flows because of electrons so therefore this is an n-channel MOSFET. In analogy to this you can have the p-channel MOSFET if you replace these n regions by p regions and replace this p-type silicon substrate by n-type silicon substrate. And of course you change the polarities then you will have operation using a p-channel MOSFET. Now, apart from the channel type that is n or p-channel you also have another classification for MOSFETs. That is normally-on and normally-off.

(Refer Slide Time: 39:20)



So, MOSFETs can be n-channel or p-channel and further each of these devices can be normally-on or normally-off. This normally-on device is also referred to as depletion-type device while the normally-off device is referred to as enhancement type device. Now let us understand the meaning of these terms normally-on and normally-off. For this purpose let us look at the device structure and its operation in a little bit more detail.

(Refer Slide Time: 34:32)



So this is an n-channel MOSFET. Let us name the various terminals here, this is the gate, this is the substrate. Now we shall call the substrate as the bulk. The reason is substrate and the source both have letter starting with s. So when you use symbols with the starting letter to denote the particular terminal there will be confusion between substrate and source because both have (s) as the starting letters. Therefore we use the word bulk to represent the substrate. So B stands for Bulk.

Then how do you name these two terminals? For this purpose you recognize the fact that it is a symmetric device. That is, supposing I call this as source and this as drain I could call this terminal as source and this terminal as drain. Now how do you decide which is source and which is drain? It depends on the polarity of the voltage applied. So let us put the polarity of various voltages. This is the gate with respect to this supposing we use this as the common point so we are applying a positive gate voltage. You must apply a positive gate voltage in an n-channel device because you want to attract electrons.

You want to create an inversion layer which will carry the current from this terminal to this terminal. Please note that you should avoid any current through the substrate because a current flowing through the substrate or across the substrate cannot be controlled by gate. It is only the inversion layer charge that is controlled by the gate. And unless you can control the current by the gate you really do not have a triode or an amplifying device. The current should be controlled by a gate. So this is the inversion layer and to form this inversion layer this should be positive with respect to this. Of course this should be positive with respect to this also.

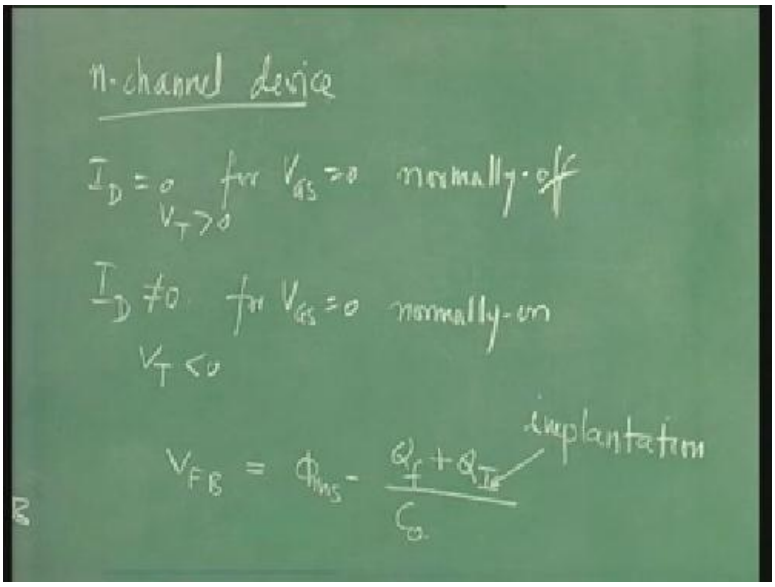
Now you have a choice of connecting a power supply to the bulk between source and bulk. You can either connect a negative supply or a zero bias between this terminal and the bulk terminal. We will now explain why this is called the source. For simplicity let us assume this is shorted or this is 0. Now, to pass a current there should be a voltage drop between this and this terminal. Here, clearly I cannot apply a negative voltage to this terminal with respect to this because if I apply a negative voltage here then between substrate and this terminal also there will be a negative voltage. This will be positive this will be negative because you have connected this here. That means there will be a forward bias across this junction which is not correct because if you have a forward bias a large current will flow and then that current which is coming in this terminal cannot be controlled by the gate so that current is of no use as far as our main purpose is concerned to use the device as an amplifier. Therefore it means that in this arrangement if I choose this as the common terminal this voltage will always be positive with respect to this terminal. So let us apply that voltage.

Once this voltage is positive you know that the current always flows from positive terminal to the negative terminal so this is the common terminal which means the current with flow into the terminal. This is the conventional current that is the current because of positive charge. Now the electron current on the other hand will flow from negative terminal to positive terminal. So the electrons are flowing from this terminal to this terminal. That means this terminal is acting like a source of electrons. That is why this terminal is called the source and this terminal is draining all the electrons which are being supplied from the source that is why this is called the drain.

With this operation you can understand the meaning of a normally-off device and a normally-on device. The question is, how much voltage do have to apply here? Now this voltage is called the V_{GS} gate to source voltage. This voltage is called the V_{DS}. How much voltage you must apply here so that the inversion layer forms? Now, in the context of MOS capacitor we have explained that inversion layer forms only beyond a threshold voltage. In this particular a simple circuit please note that gate to source voltage is the same as gate to bulk voltage because source and bulk are shorted. We can assume this V_{GS} also as V_{GB} because S and B are both shorted. In other words, we can connect this discussion to MOS capacitor discussion we had earlier. So this V_{GS} should be greater than the threshold voltage of the device so that you have an inversion layer. So V_{GS} is greater than V_T.

Now the question is what is V_T?
If the V_T is positive then you will have to apply a voltage more positive than V_T. Therefore you will have to apply a non-zero voltage to create the inversion charge. In such a case if you do not have any voltage applied or if the gate to the source voltage is zero you do not have any channel here so there is no conduction between these points or there is no current. These are the so-called drain current.

(Refer Slide Time: 34:55)



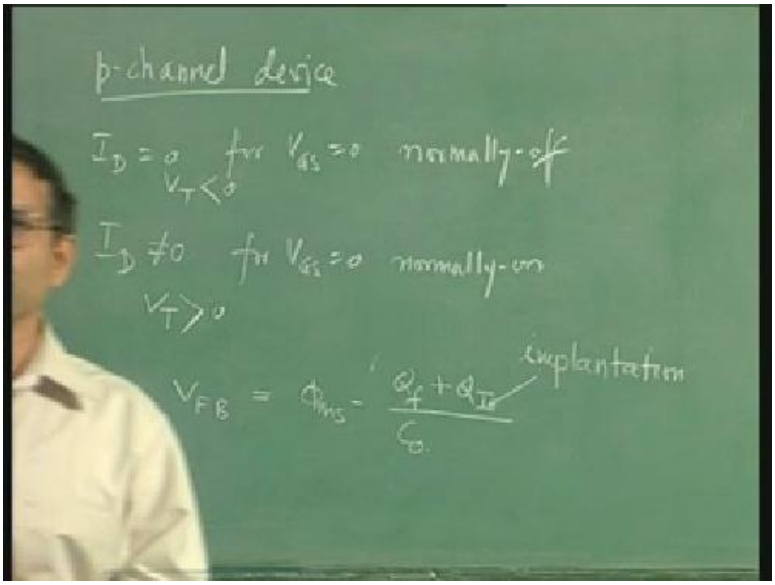
So if I_D is 0 for V_{GS} is 0 then this is called a normally-off device, there is no current and the device is off when there is no gate voltage. So this particular condition is called normal condition when there is no gate source voltage. So, in a normal condition the device is off. On the other hand, if I_D is non-zero for gate source voltage equal to 0 then this is called a normally-on device and here this is normally-off. So this condition will be true if V_T is less than 0 and this condition will be true if V_T is greater than 0. Now obviously this is a discussion for n-channel device. So when V_T is less than 0 that means even when V_{GS} is equal to 0 you will still have a channel because 0 is more than any negative quantity. So V_{GS} is equal to 0 will be greater than threshold condition and therefore you will have channel even when there is no gate to source voltage.

How can V_T of an n-channel device be negative?
You know that from the theory of MOS capacitor the threshold voltage depends on the Flat-band voltage and the Flat-band voltage in turn depends on the work function difference between the gate and substrate and also the fixed oxide charge. So V_{FB} is given by this formula. Now this V_{FB} can be tailored if you can alter any of these two terms. In practice you can change this term. There are ways of changing the term corresponding to Q_f.

Instead of changing the Q_f itself that is the interface fixed charge you can add additional charges at the interface by doping. And these charges can be either positive or negative polarity depending on the type of doping whether it is acceptor type or donor type. So, not only by changing the Q_f but by adding additional charges here. We can call this Q_I. Normally these additional charges because of doping are added by a process of implantation. Now Q_I can be positive or negative in polarity depending on the doping. These charges are created at

the interface. So you create a very thin doped layer here at the interface and that will give you this particular modification of the term and that is how you can control the V_{FB}. Now, by controlling the V_{FB} you can control the V_T. That is how you can get both positive and negative V_Ts. Now whatever we have discussed for n-channel applies for p-channel also in an analogous manner.

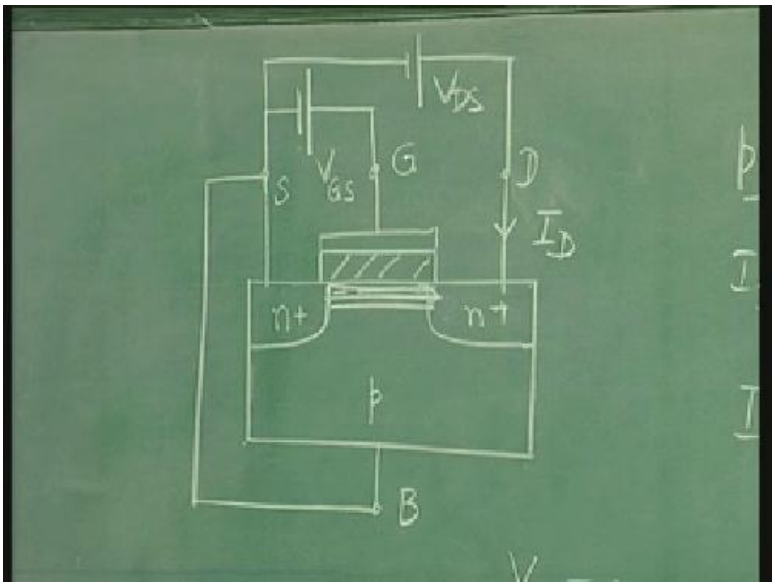
(Refer Slide Time: 39:26)



That is, if you consider a p-channel device then for a normally-off device V_T is less than 0 and for a normally-on device V_T is greater than 0. Again the change in the threshold voltage is obtained by changing the Flat-band voltage V_{FB}. Now, apart from normally-on and normally-off device classification there is another classification and that is any of these devices can be either surface channelled or buried channel. So here for example, this normally-off device would be surface channelled or it could be buried channel. This obviously applies to each of these devices. So we can abbreviate surface channel as SE and buried channel as BC. The enhancement type devices are abbreviated as E and depletion-type devices abbreviated as D.

Now, what are the surface channel and buried channel type of devices?
Basically these nomenclatures refer to the location of current flow. For example, look at this particular MOSFET. If the current flow is because of inversion layer here then the inversion layer is attracted to the interface and therefore it is right next to the interface so all the carriers are pressing against the interface. In other words, the current flow will be at the interface or at the surface of the semiconductor. So the interface is also referred to as the surface of this semiconductor. Therefore if the current flow is through an inversion layer then it is a surface channel device. On the other hand, as we explained you can change the threshold voltage by changing the Flat-band voltage which in turn can be changed by creating a thin doped layer.

(Refer Slide Time: 39:44)

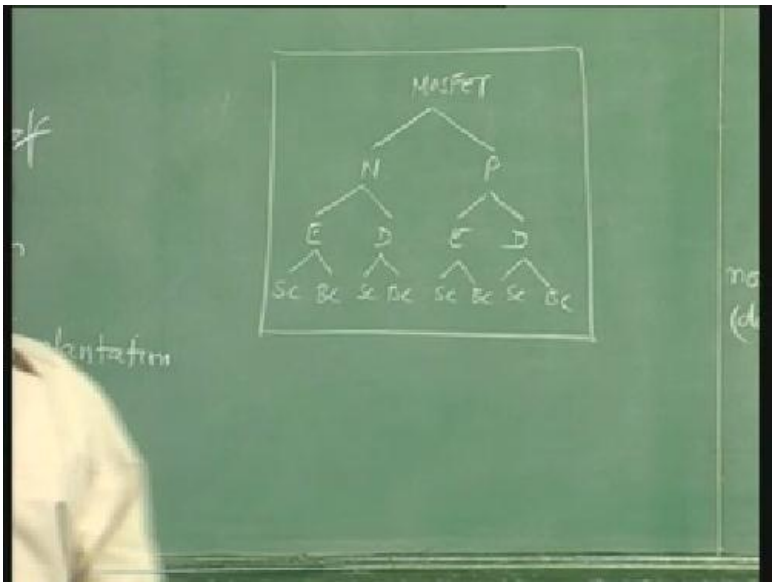


For example, if you create a thin doped layer of donors or n-type material here in order to create a change in threshold voltage then the current flow will not be right at the interface in fact it will be distributed over this doped layer. So it would be at the interface as well as in the bulk that is inside this doped layer. In fact most of the current flow will be away from the interface. Then the current flow is said to be buried under the interface it is not at the interface but buried inside. Therefore the device will then be called the buried channel device in such a case. So whenever you have a doped layer connecting between source and drain the device becomes a buried channel device. If you do not have doped layer then it becomes a surface channel device because the channel is created by inversion layer carriers.

Sometimes there is confusion among students about buried channel, surface channel, depletion-type and enhancement type. Many times students think whenever there is a doped layer between source and drain then the device is always depletion-type so buried channel and depletion-type devices are identical. This is actually not correct, this is very clearly shown here by this classification. Even a normally-off device can be buried channel or a normally-on device can be surface channel. It all depends on how you are adjusting your threshold. That is, is your threshold being adjusted by adjusting the Q_f or is it being adjusted by having implantation. So you can have a situation where you have a doped layer here of donors and that doped layer is totally depleted for gate source voltage equal to 0. Then to open the conduction channel between source and drain you will have to un-deplete this doped layer.

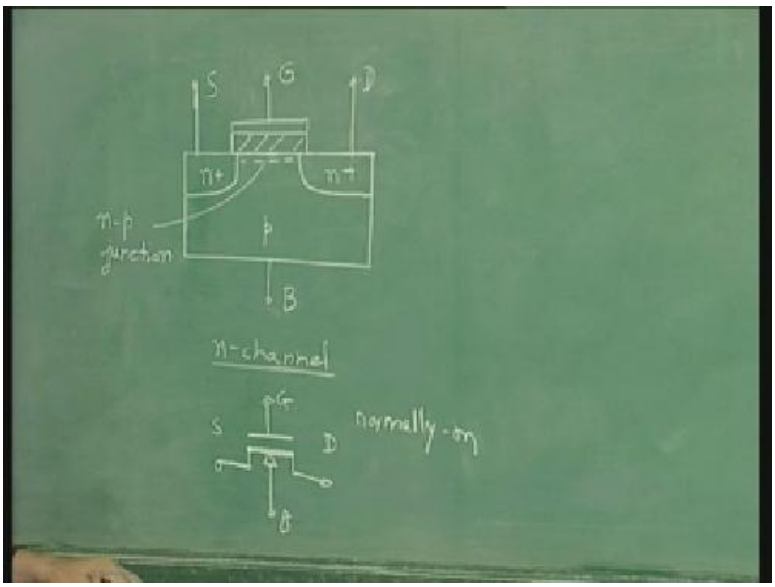
So, in practice a buried channel device can be both normally-off and normally-on and surface channel device also can be normally-off or normally-on. So this kind of a classification of devices is not there in bipolar transistors. You have either n-type bipolar transistors or n-p-n device or you have a p-n-p device that is the only classification whereas here you have normally-on, normally-off and surface and buried channel. In fact one can show these using abbreviations very easily.

(Refer Slide Time: 41:00)



This is the MOSFET, you can have either n-type or p-type. Each of these can be enhancement or depletion and each of these devices further can be either surface channel or buried channel. So these are all the different types of MOSFETs we have. Having discussed the various types of devices and broadly seen the device structure let us understand the symbol of MOSFET also now.

(Refer Slide Time: 43:59)

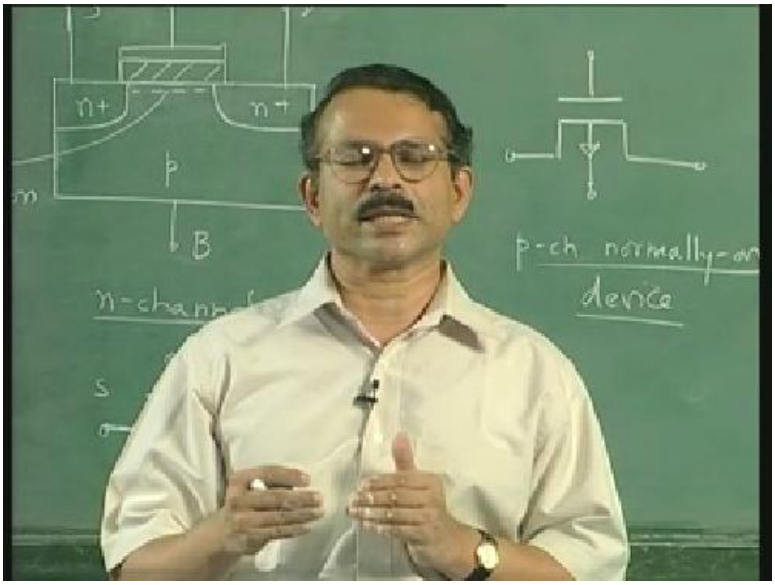


Let us look at this structure of an n-channel device and correlate the structure to the symbol. So you have the gate then you have the channel. Now, if this is a normally-off device then the channel will not be connected between source and drain when there is no gate source voltage and in such a case the channel is shown by dotted line. So if the channel is shown by dotted line it is a normally-off device. Now you have this source and drain terminals, this is the gate, source and drain.

Of course you can have this as drain and that as source that is also possible. To know whether it is normally-on or normally-off you have indicated using the dotted line or solid line here for the channel. Now how do you indicate the type of the device as whether it is n-channel or p-channel? This is indicated as follows. If this is an n-channel device as it is here then the channel will be n-type in which case there is what is called an induced n-p junction here. If this is made of inversion layer there is an induced n-p junction but if it is a doped layer then it is an n-p junction that is created, in either case there is an n-p junction.

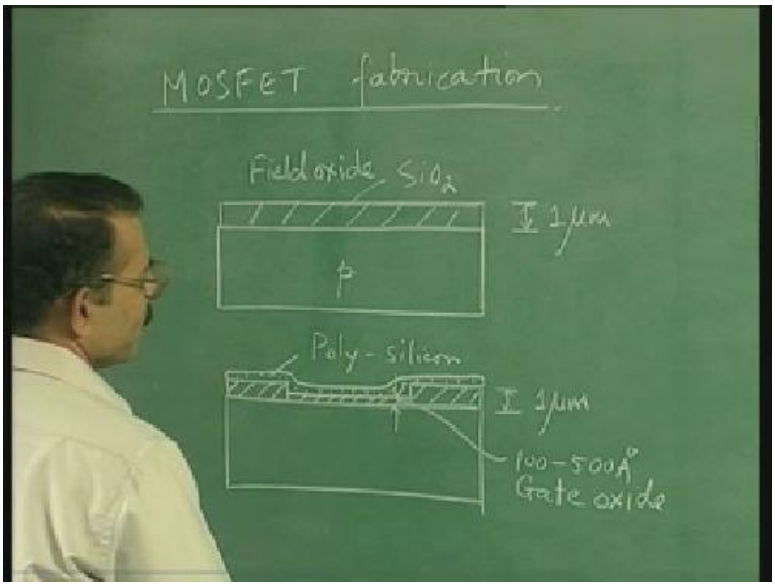
Now you can use a diode to show that n-p junction. In this case since the channel is n-type and substrate is p-type the bulk channel diode is p-n for an n-type device. The channel is n and bulk or substrate is p and that is why the diode symbol is like this p-n. Therefore the arrow indicates the type of the channel and the dotted line or solid line indicates the normally-on or normally-off nature of this device. So this is the symbol for a normally-off n-channel device. Now, how would you draw the symbol of a normally-on n-channel device? So normally-on n-channel device would be, you change this dotted line to a solid line then this is normally-on.

(Refer Slide Time: 45:30)



This symbol for example indicates a normally-on device because this line is solid and it indicates the p-channel device because the channel is p and substrate is n so it is p-n and that is the direction of this diode. So this is a p-channel normally-on device. This is how you build up the symbols for the various types of devices. There is no differentiation between buried channel and surface channel devices as far as the symbol is concerned. The symbol only indicates whether it is normally-on or normally-off and it indicates whether it is n-channel or p-channel. Now, depending on the process employed and the device structure you will get a buried channel or surface channel device which is not shown in the symbol. After this we will discuss the essential fabrication steps for creating this particular device structure. After discussion of the fabrication steps we will take up the characteristics.

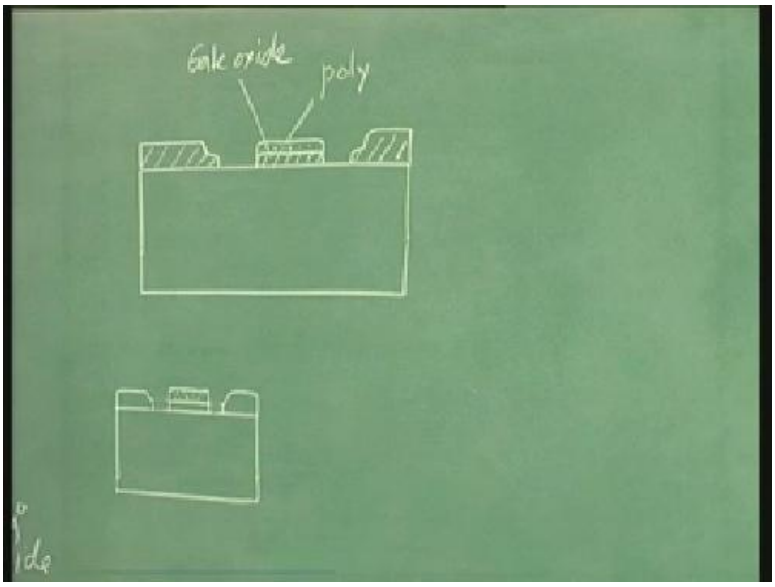
(Refer Slide Time: 50:33)



MOSFET fabrication:
We will be discussing the steps for n-channel MOSFET which is made on a p-channel substrate. You can construct a sequence of steps for p-channel MOSFET in a similar manner. Also, we will be discussing the essential steps; the actual number of steps is rather large so we will be discussing only the very important steps here. Let us start with a p-type substrate and then on the top of this we grow a thick silicon dioxide layer, this is of the order of a micron. After doing the silicon dioxide layer we isolate those regions where we will make the transistor.

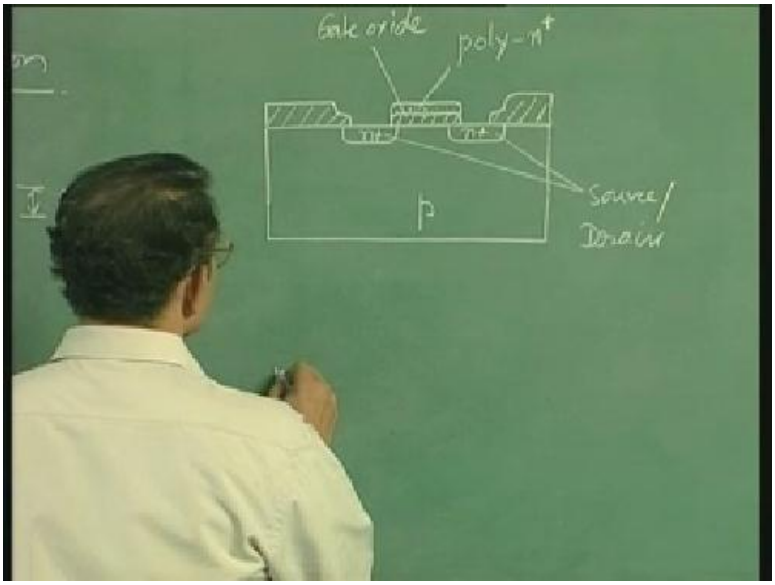
This is 1 micron thick oxide. By lithography we have defined these particular regions where we will make the n-channel transistor. The next step is to grow a thin very high quality oxide that will be used as the gate oxide. So the thickness of this oxide depends on the design of the MOSFET. It can vary anywhere between 100 to 500 Angstroms in present day MOSFETs. In fact people are going below 100 Angstroms. This particular oxide is called the gate oxide and this silicon dioxide is called the field oxide. The gate oxide is done as against this particular field oxide. After this is done what we do is we deposit the poly-silicon which is used for making the electrode on the gate. So this is the poly-silicon. Now we need to define the gate region here. This is done by lithography which is the next step.

(Refer Slide Time 51:13)



Here this is the poly-silicon gate, we will just write it as poly and this is the field oxide and this is the gate oxide. Now, notice that here in the lithography what is done is first we etch this poly-silicon to the required dimension so poly-silicon is removed from other regions and then we are etching the oxide. So there are two etching steps here which involved. First is etching the poly-silicon to the required dimension and then etching the gate oxide as follows: Here if you see, you have to first etch this poly-silicon up to this much distance. So when you do that the structure would look something like this. This is the poly-silicon, it has been etched to the gate dimension. Now you are going to etch the oxide in the remaining portions and it is something like this. That is what you see here, the blown up portion.

(Refer Slide Time: 53:55)

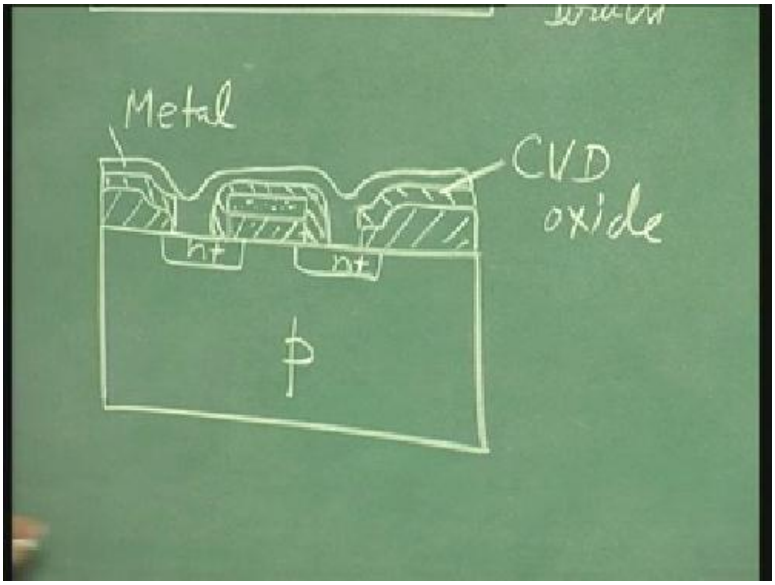


Now this poly-silicon as it is not really doped heavily so its resistivity will be large. Now, in the next step when you create the source and drain regions the poly-silicon will get doped heavily. In this case since it is an n-channel device your source and drain will be heavily

doped n-type. So when you are creating this n plus layers from the top this poly-silicon also will get doped by this particular n plus diffusing atoms. So here in this particular process the poly-silicon is going to become n-type at the end of this step. This is the so-called source or drain. Now you have to make a contact to the source and drain using metal. But you will see that if you make a contact right on top of this if you put metal that metal will get shorted to the gate so you will have to isolate the metal contact from the gate electrode. For this purpose what is done is an oxide is grown on the top of this.

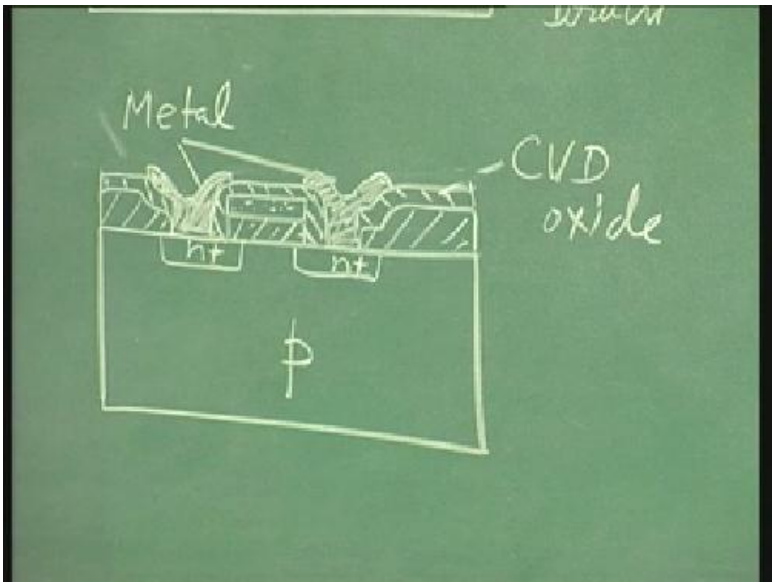
Now at this point we must distinguish between two types of oxidation. One type of oxidation involves passing oxygen at high temperatures of 1000 to 1200 degree C over silicon. Then what happens is a part of silicon on the surface will react with the oxygen and get converted into silicon dioxide. So the silicon required for silicon dioxide formation will be taken from the substrate. On the other hand, you can have another type of oxide that is deposited. This involves passing chemical gases over a substrate which is raised to about 600 degree C so the temperature of this oxidation is not that high. Then the gases react with each other and the product of this reaction is silicon dioxide which gets deposited on the silicon wafer. So this type of oxide is called CVD deposited oxide. What we are doing now here is, we are depositing an oxide using the CVD technique.

(Refer Slide Time: 55:28)



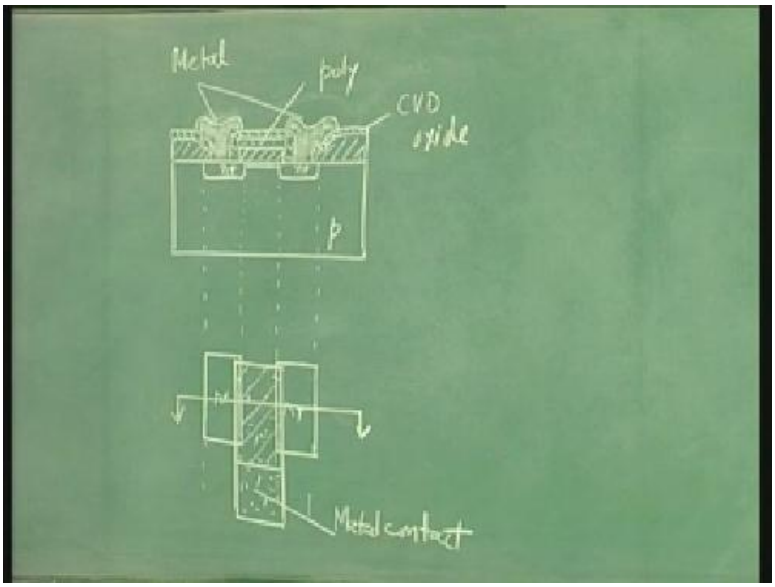
Now when you do that this is how your device will look. So this is the field oxide, this is the gate oxide and now you are depositing the CVD oxide on the top of this. The next step will be to etch this oxide in these areas where you want the contact. Please note that the n plus region is already there. So by lithography what will be done is the oxide will be removed in this region above the n plus regions which is something like this. Now to make the metal contact a metal layer will be grown on the top of this. And the final step will be the etching of the metal from unwanted areas so that you have contact to the n plus regions. So when you etch out metal it will look like this.

(Refer Slide Time: 55:55)



So this is the metal and there are the metal contacts. Now sometimes students have a doubt that how do you make a contact to the poly.

(Refer Slide Time: 57:40)



To understand how you make a contact to this poly you should look at the top view. The top view looks something like this. This is your source and drain and this is your poly. So you see that the poly is extending out of the gate region. Now this oxide that is shown is present on the top of this. So when you take a cross section here you will this structure. But here this oxide is not there so the oxtrite its present only up to some region here. So this is covered with oxide. But here there is no oxide and the oxide is removed so that you can make a metal contact. That is the sequence of fabrication steps used to make the MOSFET.

We must emphasize that some steps which are important have not been shown in our description so far. For example in this region you do a doping to adjust the threshold voltage

of the device. This is a critical step which we did not show because if you want to show all these steps then the process looks very complicated. The theory we developed in this first course helps us to assume a simple MOSFET structure. In the next class we shall discuss the current voltage characteristics.