Solid State Devices
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Lecture - 37
Metal-Oxide-Semiconductor (MOS) Junction
(Contd….)

This is the last lecture on the topic of MOS junction or capacitor.

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Let us quickly summarize what we achieved in the previous lecture. In the previous lecture we explained the low frequency and high frequency C - V characteristics. Then we did some calculations to show how we can get the critical capacitance and voltage values on the measured capacitance voltage curve. This was our measured capacitance voltage curve.

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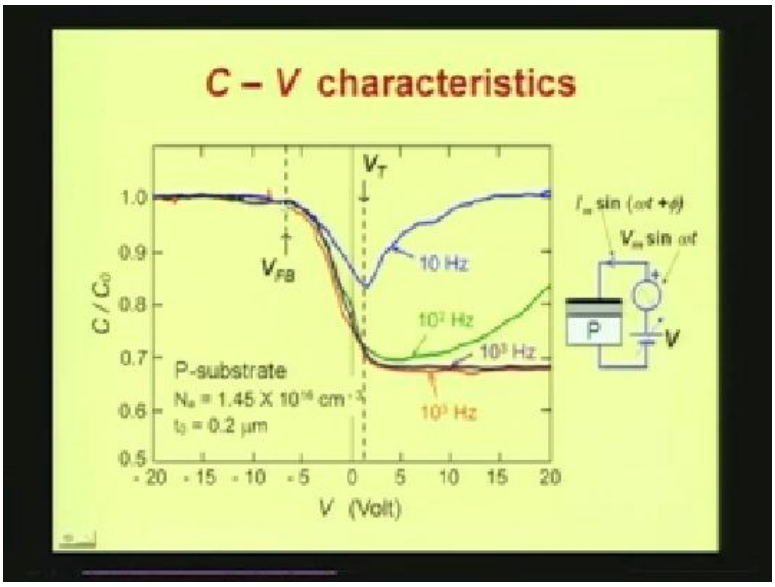

Our calculations starting from the doping level of the substrate, the oxide thickness and the fact that the gate was made of aluminium metal gave us the following characteristics:

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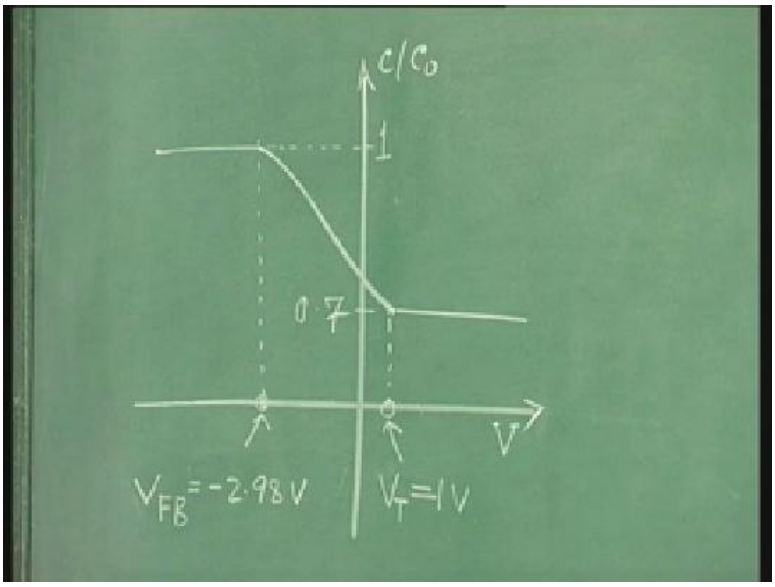

So the critical values of the minimum capacitance were 0.7 this is normalized capacitance. So minimum normalized capacitance was 0.7 and the threshold voltage was 1V. This 1V threshold voltage was actually obtained directly from the measured characteristics whereas this 0.7 value was estimated. And then we also estimated the Flat-band voltage. Now let us look at this Flat-band voltage in more detail. This value 0.7 is very close to 0.685 that we observed on the C - V characteristics. So, on the C-V characteristics if you see this minimum value here is little less than 0.7 but quite close to 0.7. However, the Flat-band voltage is minus 2.98 as calculated which is very different from what we have been showing here. So, on the measured curve this appears to be the kind of approximate Flat-band point because

beyond this the curve has started dropping. Whereas according to our calculation the picture is something like this.

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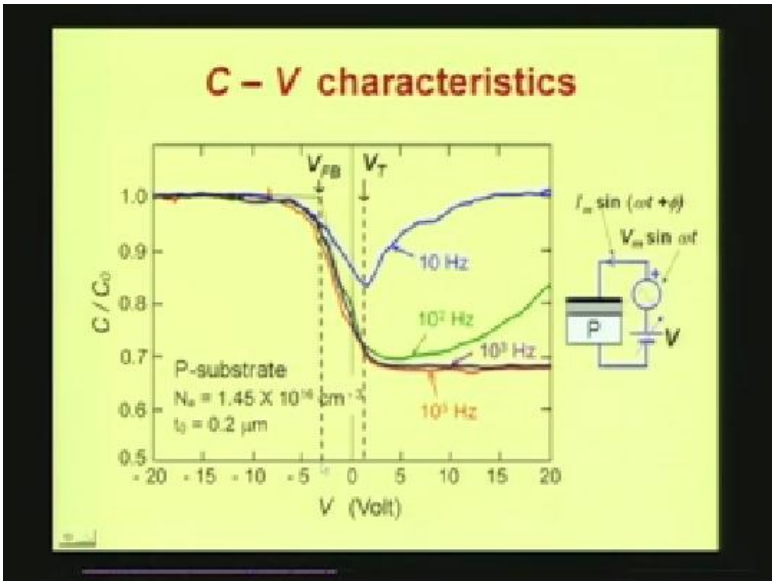

So Flat-band voltage is about minus 3. Now how do we explain this? This is an important point we have to understand.

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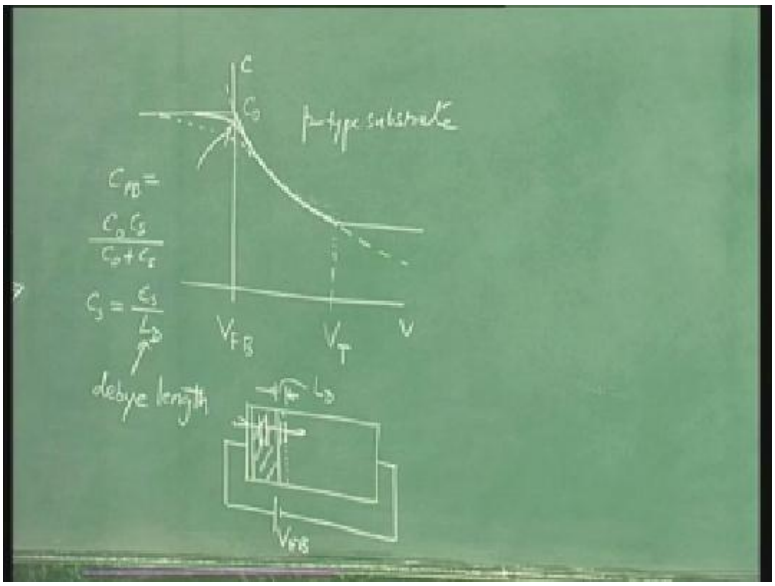

The fact is, what we have derived is an approximate C - V curve which has three segments. Suppose this is the Flat-band point and this is the threshold point the curve C versus V has to be in segments, one is the constant segment. Then you have a segment that is a kind of square law which goes like this. This is a quadratic equation for capacitance versus voltage which is cut-off. This segment is cut-off at the threshold voltage point. For high frequency capacitance you have another constant segment here but for low frequency capacitance it goes up to this value which is C_0. So this curve is actually an approximate curve, you cannot have a sharp

transition like this at this point at the Flat-band voltage. In fact your actual curve if you make rigorous calculations would turn out to be something like this. So here at the Flat-band point the capacitance is not exactly C_0. In fact this capacitance C Flat-band can be shown to be equal to a series combination of C_0 and a semiconductor capacitance given by C_0 into Cs by C_0 plus C_s where C_s is equal to E_s by L_D where L_D is called Debye length which we have talked about earlier in the context of PN junction. So, at the Flat-band point the picture is something like this:

This is the oxide layer and you have a small space charge layer like this whose length is equal to the Debye length. So this is the Flat-band voltage which you are applying. So the capacitance therefore is a series of combination of the oxide capacitance which comes here and the semiconductor capacitance which comes there so it is these two capacitances. That is one of the reasons why if you see the Flat-band point on the C - V curve you find that the capacitance has dropped below the value C_0 or normalized capacitance has dropped below 1. This is one of the reasons why again the Flat-band point is somewhat difficult to locate.

Now, apart from that there are also other deviations which we have not considered. So the measured characteristics will also have effects of the interface charges Q_{it} and in the interface charge the behaviour is somewhat more complex as a function of voltage. Unlike the fixed charge the interface charge Q_{it} can change with voltage. Therefore there will be a stretch out effect of this curve. In other words, the curve will not be this but it would be something like this. So this is another reason why the Flat-band point will deviate from the calculated value to more negative values for a p-type substrate. So this explains why although the calculated Flat-band point is somewhere here as shown on the slide at minus 3. The actual Flat-band point could be away somewhere here. In fact this point has to be located by some involved calculations or argumentations. We have explained the kind of deviations of the measured characteristics from the calculated characteristics. Now we come to the final topic of the MOS junction or capacitor and that is the body effect where we come to the discussion of the three terminal MOS junction or capacitor.

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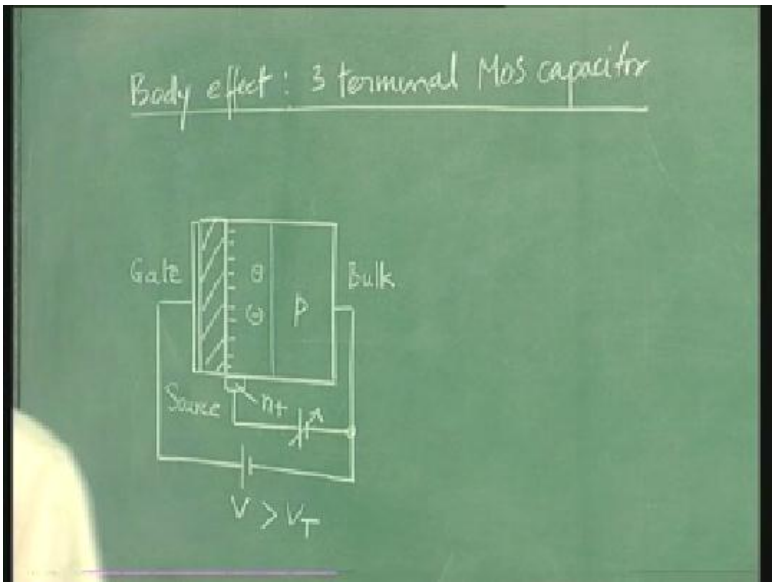

So this body effect is seen when you have a capacitor like this and we connect another contact here. For the purpose of simplicity we will assume that the contact is really very small and this contact is made of n plus. This contact enables you to establish a connection with the inversion layer here which appears if you apply a voltage more than the threshold voltage. So here this voltage is more than threshold voltage so as a result you have created an inversion layer here of electrons. Of course you have the depletion layer already and you are using this contact to connect to this inversion layer of electrons and that is why the contact is n plus.

Now what we want to study is, what will happen if you change the potential of the inversion layer of electrons by applying a voltage to the n plus contact? So here we apply a voltage with respect to the bulk. So this bulk point is being taken as common for both gate as well as for this particular contact. We want to see what effect it will have on the charge here if you vary this voltage. That is why this is called a three terminal MOS capacitor where you have this terminal, this terminal and this third terminal.

The question is what do we call this contact as? We will call this contact as the source. So this is the gate and this is the source and this contact is called the bulk. This is called the source because it can be shown that, if you make small changes in the voltages then even at high frequencies you will be able to get the layer of electrons change in response to change in voltage because of this contact providing electrons to this layer.

So, in a two terminal MOS capacitor where this n plus contact is not there as we have discussed earlier if you make a change in the voltage at very high frequencies then the change in the charge occurs at the edge of the depletion layer. That is why the high frequency capacitance is constant at a minimum value whereas low frequency capacitance goes up to the oxide capacitance. So, unlike that situation in a three terminal MOS capacitor once you provide the n plus contact even if you make changes in the gate voltage at very high frequencies you can have this inversion layer responding to the change because this n plus region has a large supply of electrons and it can provide electrons as fast as this layer needs. That is why this contact is referred to as the source because it can source the electrons required for the inversion layer changes.

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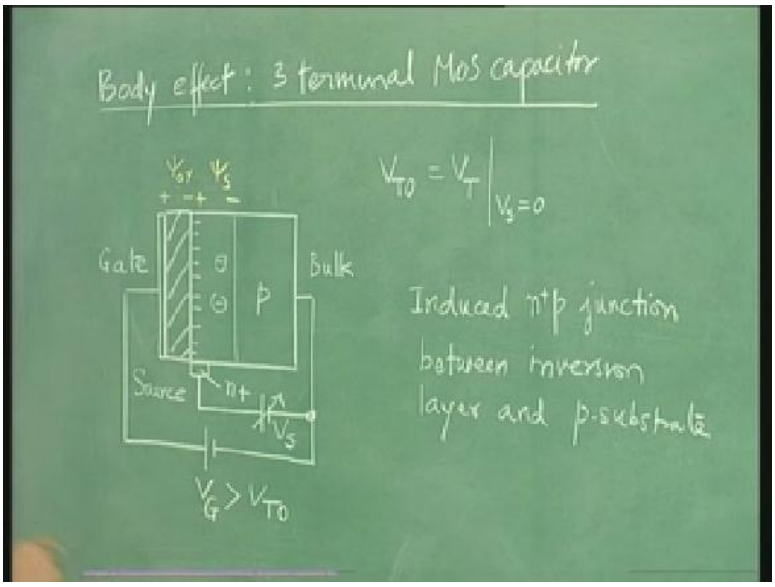

Since this is called the source and now there are two voltages here we should distinguish between the two voltages. So we will call this as V_S that is the source voltage and we will call this as the V_G that is the gate voltage. We did not have this problem in a two terminal capacitor because there was only one power supply.

Now as we will note the body effect is actually a change in the threshold voltage because of the power supply V_S. That being the case what we will do is we will define the threshold voltage for 0 source voltage that is the threshold voltage that we have estimated in the last class as V_{T0}. So V_{T0} is a threshold voltage of the device corresponding to V_S is equal to 0. So when V_S is equal to 0 this contact is shorted to the bulk and it can be shown that whether the contact is shorted to the bulk or whether it is kept open circuit it really has no effect on the inversion layer and therefore the device behaviour when this n plus contact is either open circuited or short circuited to the bulk is the same as the device behaviour of a two terminal MOS capacitor. So threshold voltage of that two terminal MOS capacitor is V_{T0}.

Now, to understand the effect of this V_S on the inversion layer what we should do is we should start with a gate voltage which is very large so that it more than the threshold voltage corresponding to V_S is equal to 0. In other words, what we are doing is we have the n plus contact but we do not apply this V_S so we blank out this V_S, there is no V_S and we apply a gate voltage which is much more than the threshold voltage corresponding to the condition when there was no V_S. So that ensures you have sufficiently large inversion layer charge.

Now we superimpose a V_S here, connect a V_S between the source and the bulk and you start increasing this V_S from very small values and you see the effect. Now one doubt will arise, what should be the polarity of V_S? Should it be positive or should it be negative? Now we have already explained this contact is n plus because the purpose of this contact is to provide a connection to this inversion layer and also this particular block should not provide any contact to p but we only want to contact the n plus. So the only way we can achieve this is to put an n plus region here. For example, if you put a p region it cannot make contact to the inversion layer which is large number of electrons. There will be a junction between the inversion layer and the p region here so you can only have n plus region there.

Now the question is, what is the polarity of V_S?
Note that if the n plus contact is made negative with respect to bulk then this PN plus junction will get forward biased. And when there is a forward bias across the junction you know that a large current flows. So what will happen is that if your n plus contact is made of negative polarity with respect to the bulk p-type region or substrate p-type region then a large current will flow through this contact. Also, you cannot vary the voltage over a very wide range because you know that beyond 0.7V the current starts shooting rapidly in the forward bias direction. Therefore, if you increase the voltage too much the current will be very large or dissipation will be large and the device may burn out. So if you apply a forward bias here there are two problems, one is that there is a large forward current in the device which you cannot control by the gate and also we cannot have a very wide variation in the voltage to control the inversion layer charge. Therefore we are only allowed a positive voltage to n plus contact with respect to p.

In other words, the PN plus junction should only be reversed biased. Now we start increasing V_S and what is the effect? To understand the effect of V_S on inversion layer it is useful to regard this particular region of the MOS capacitor next to the interface as an induced n plus p junction. So this induced n plus p junction is between inversion layer and p substrate. So inversion layer has majority electrons and p has majority holes therefore there is a PN junction here and we call it induced junction because this has been induced by application of a gate voltage beyond the threshold voltage. Once we recognise that this is an induced n plus p junction we can easily see what is the effect of applying a reverse bias V_S on this junction. Note that this voltage is getting transferred to this inversion layer.

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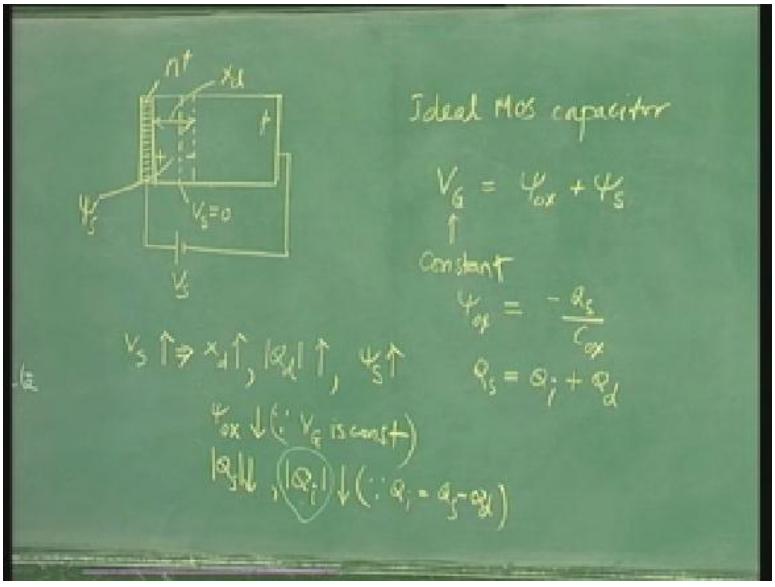

So the situation for this particular space charge region here can be shown as follows:
This is the inversion layer n plus and this is p, this is the depletion layer and the voltage across this is you are applying a voltage which is equal to V_S. So what is the effect of this V_S? Evidently the effect of the V_S is to expand the depletion layer because this is a reverse bias across this junction. So, if for V_S is equal to 0 your depletion layer was something like this so this is for V_S is equal to 0 so this was the depletion layer when you did not really connect the

power supply to the n plus contact. When you connect this V_S then the depletion layer obviously will increase.

In other words, this results in an increase in the depletion charge so as V_S increases you have increase in the depletion layer thickness so this is X_d depletion layer thickness which means you have increase in the magnitude of Q_d. It also means you have increase in the potential drop across the semiconductor. Now recall that whatever gate voltage you apply a part of it drops across the oxide and the remaining part drops across the semiconductor. Now what we will do is, when we are discussing the body effect we will start with an ideal MOS capacitor. Then you can always incorporate the effect of non-ideality by incorporating the non-zero Flat-band voltage. So if you assume an ideal MOS capacitor then you know that we can write V_G is equal to psi_{ox} plus psi_s which is the potential drop across oxide and potential drop across semiconductor. This psi_s is nothing but the potential drop here in the induced n plus p junction. Or if you look at it in terms of this MOS capacitor this is psi_{ox} and this is psi_s.

So clearly now what this diagram shows is that psi_s increases, your X_d is increasing, depletion charge is increasing and so psi_s is also increasing. So V_S increasing implies result of V_S increase is X_d increasing magnitude of Q_d increasing and psi_s also increasing. Now if psi_s increases but your gate voltage has been maintained constant, please recall this here. You have applied a gate voltage which is more than threshold voltage corresponding to $0V_S$ but we are not changing the V_G when we change V_S that is how you discuss the effect of any input parameter. If you have a number of parameters in a given situation and you want to see the effect of any one parameter other parameters should be maintained constant. So here you are maintaining V_G constant and as you change V_S your psi_s in increasing. This means that from here if psi_s increases V_G is constant and psi_{ox} decreases so psi_{ox} falls since V_G is constant.

Now what is the effect of psi_{ox} falling?
Recall that the potential drop across the oxide is equal to the total charge in silicon divided by the oxide capacitance. This is from a simple parallel plate capacitor Physics. So Q_s is the total charge in silicon including the inversion charge and the depletion charge. This psi_{ox} is Q_s by C_{ox} of course with a negative polarity because when you apply a positive voltage to the gate charge here is negative. When you write here psi_{ox} is equal to minus Q_s by C_{ox} and Q_s is Q_i plus Q_d that is inversion charge plus depletion charge then what follows from this condition is that Q_s falls if psi_{ox} is reduced then it obviously means Q_s is reduced. So another effect of V_S is Q_s falling.

Please note that we are proceeding in this order in a logical fashion. So first you start with the increase in the depletion width and then logically this means Q_d increases in magnitude which also means psi_s increases in magnitude and since V_G is constant it means psi_{ox} decreases in magnitude and psi_{ox} decreasing in magnitude means Q_s is also decreasing in magnitude. Now Q_d magnitude is increasing and Q_s is decreasing, look at this equation. If Q_s decreases in magnitude and Q_d increases then clearly Q_i is going to fall because Q_i is the difference of Q_s and Q_d. Now here we should put a modulus because Q_s is negative in polarity so magnitude of Q_s decreases so Q_i magnitude decreases since Q_i is equal to Q_s minus Q_d. This is the important result the consequence of increase in V_S.

So what we derive from here is that the effect of increase in V_S is decrease in the inversion charge but increase in the depletion charge. That means in this junction as this depletion width expands the amount of electrons in this n plus region will go on decreasing. Therefore

it appears quite logical that for some value of V_S this inversion charge which is decreasing can become equal to 0. Now, if the inversion charge becomes 0 obviously the device has reached a threshold condition because threshold condition corresponds to inversion charge just starting to increase if you are increasing the gate voltage. On the other hand if you decreasing the gate voltage it is a point when the inversion charge just goes to 0.

In this case we are not changing the gate voltage but we are changing the source voltage but that does not matter. What it means is, as you change the V_S at some point the inversion charge is coming to 0 and therefore this is a threshold point. What this means is that we started with the gate voltage which is more than threshold voltage at V_S corresponding to 0 but maintaining V_G at this value as you increased the V_S you came to a condition when the Q_i became 0 for some V_S which means now this gate voltage which was more than V_{T0} is actually a threshold condition for some non-zero value of V_S. Let us see what this value is for V_S at which Q_i will become 0. For this purpose we should write an expression for Q_i as a function of the various voltages. This can be done easily as follows:

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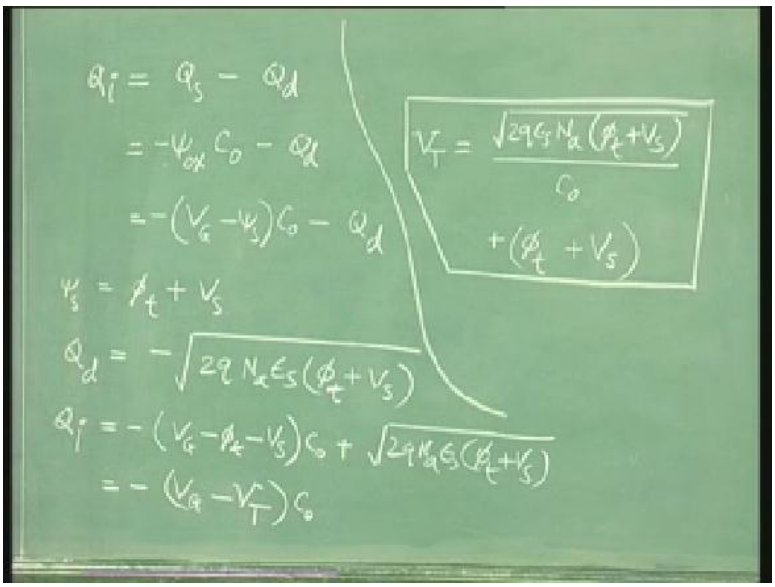

You write Q_i is equal to Q_s minus Q_d where Q_s is psi_{ox} into C_0 with a negative sign and this follows from this formula: Q_s is psi_{0x} into this is actually C_0 and we have been using the symbol C_0 instead of C_{ox} so minus psi_{ox} C_0 minus Q_d, psi_{ox} is nothing but V_G minus psi_s.

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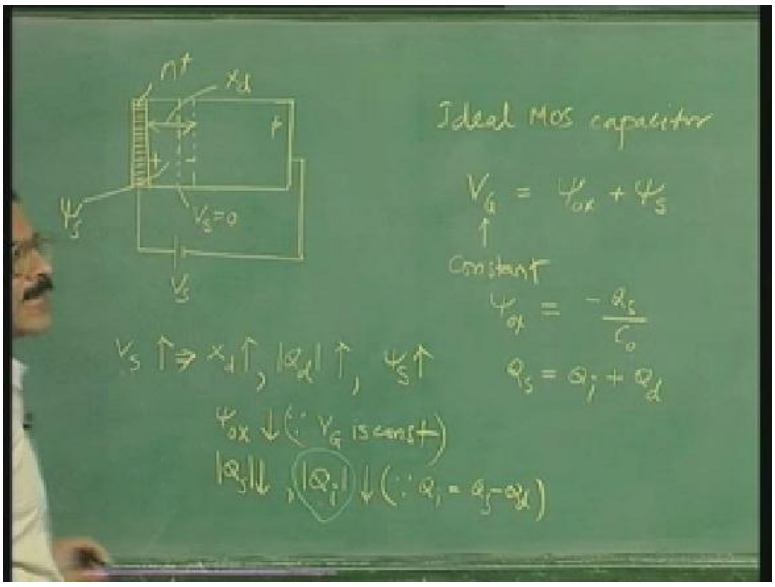

Now what is the value of psi_s?
psi_s is equal to the internal potential drop across the n plus p junction, the external applied reverse bias is V_S but when V_S is equal to 0 you still have a depletion layer because you know that there is a psi_s when you create an inversion layer and that psi_s is equal to phi_t or 2 phi_f. So when inversion layer is created obviously there is a potential drop in silicon otherwise you cannot create the inversion layer and that potential drop is equal to phi_t or 2 phi_f. So when V_S is equal to 0 psi_s is 2 phi_f or phi_t. So, for any non-zero reverse bias your potential drop across the induced NP junction from the PN junction theory will be the built-in potential plus the reverse bias.

Here the phi_t is like the built-in potential for this n plus p junction. So we can write psi_s is equal to phi_t plus V_S. Once we know this psi_s we can also write an expression for Q_d in terms of psi_s. So you recall that when the capacitor was an ideal capacitor under inversion then we wrote the expression for Q_d as square root of 2q N_a $epsilon_s$ into phi_t. It was a two terminal capacitor and it was an inversion. Now all you need to do is, you replace phi_t by phi_t plus V_S because this is the new value of psi_s, this phi_t is nothing but actually psi_s.

Of course this should have a negative sign here because the charge is negative in polarity. Now we can substitute these two terms here and we can get an expression for inversion charge as Q_i is equal to minus V_G minus phi_t minus V_S minus into C_0 minus Q_d where Q_d is minus of this quantity therefore you get plus square root of 2q N_a $epsilon_s$ into phi_t plus V_S. Now clearly from here you can slightly write this equation, reorganise the terms and you can write it as follows: minus (V_G minus V_T) C_0 you can write it in this form and you can recognise that the V_T here would be, from this equation you can see that this V_T is equal to square root of 2q N_a $epsilon_s$ N_a into phi_t plus V_S by C_0 plus phi_t plus V_S where this is the so-called potential drop in the oxide and this quantity is potential drop in silicon, that is the gate voltage V_T.

Now what is the idea in writing it in this form?
You recognise that Q_i is 0 when V_G is equal to V_T. This means this is your new threshold voltage as a function of V_S. So we can check this particular expression by considering a

limiting case. This expression must reduce to the expression we had for threshold voltage for V_S is equal to 0 if we substitute V_S is equal to 0. Now here if you substitute V_S is equal to 0 you end up getting that expression which we derived for ideal MOS capacitor earlier.

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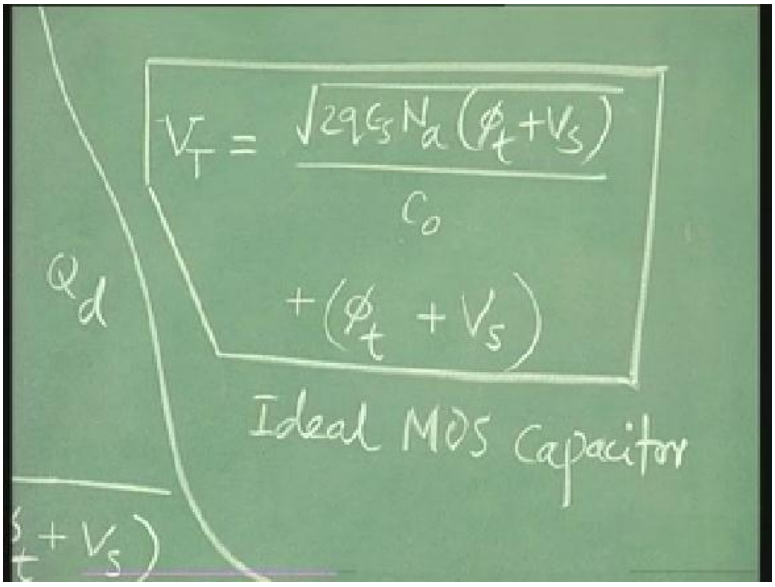

So this is the body effect, the increase in threshold voltage with V_S. Clearly the right hand side increases as you increase the V_S. So we can write this threshold voltage also in terms of V_{T0} to clearly show the increase in threshold voltage as compared to the condition V_S is equal to 0. So this is the V_T for an ideal MOS capacitor including body effect and this V_{T0} so we can write V_T minus V_{T0} normally referred to as delta V_T. So this delta V_T is equal to, this is actually denoting the body effect, you subtract this equation from the equation in which V_S was 0 therefore clearly you will get square root of 2q epsilon$_s$ N_a into phi$_t$ plus V_S.

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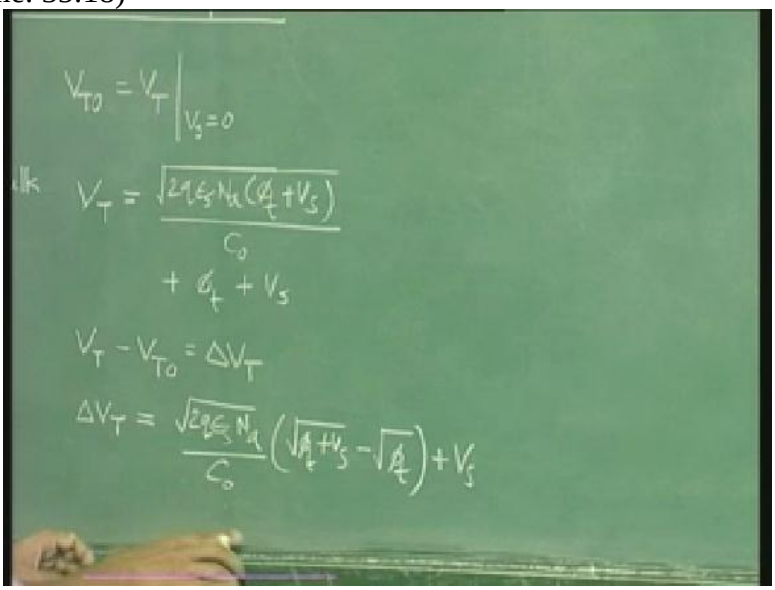

We can actually take this out square root of 2q epsilon$_s$ N_a so this by C_0 (square root of phi$_t$ plus V_S minus square root of phi$_t$) plus V_S, this is the delta V_T. We should emphasize that we

are using the bulk terminal as a common terminal for applying V_S and V_G. We will see later that this value gets modified if you use the source as a common terminal and apply gate voltage with respect to source and bulk voltage with respect to source. We will find that actually this term V_S will drop out and we will see this when we take up the MOSFET. Now, this term here is normally given the symbol gamma.

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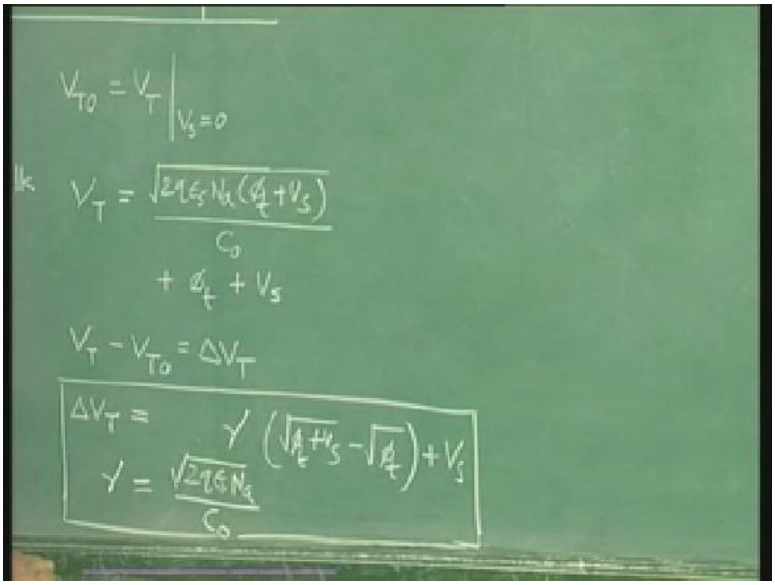

Normally delta V_T is written as gamma times this where this gamma is square root of 2q epsilon$_s$ N_a by C_0 so this is your body effect. Now we explained all these assuming an ideal MOS capacitor which means the Flat-band voltage was assumed to be 0. If the Flat-band voltage is not 0 we can now include its effect very easily. All that we need to do is we should replace V_T by V_T minus V_{FB}, delta V_T will not be affected because when you subtract V_{T0} from V_T both will have a Flat-band voltage term and that term will get cancelled. So including Flat-band voltage you can write the threshold voltage as Flat-band voltage plus V_S plus phi$_t$ plus gamma into square root of phi$_t$ plus V_S. So this is threshold voltage of a three terminal MOS capacitor.

In order that we understand the body effect very clearly we can discuss the same thing that we were elaborating upon so far in a slightly different way. So far we assumed V_G to be constant at a value greater than threshold voltage for V_S is equal to 0 and then we increased the V_S to see what is happening and we explained that the inversion charge is going to reduce. Let us try to see what will happen if you keep V_S constant and you increase V_G from 0. So instead of keeping V_G constant and increasing V_S from 0 we keep V_S keep constant and increase V_G from 0, so what is going to happen?

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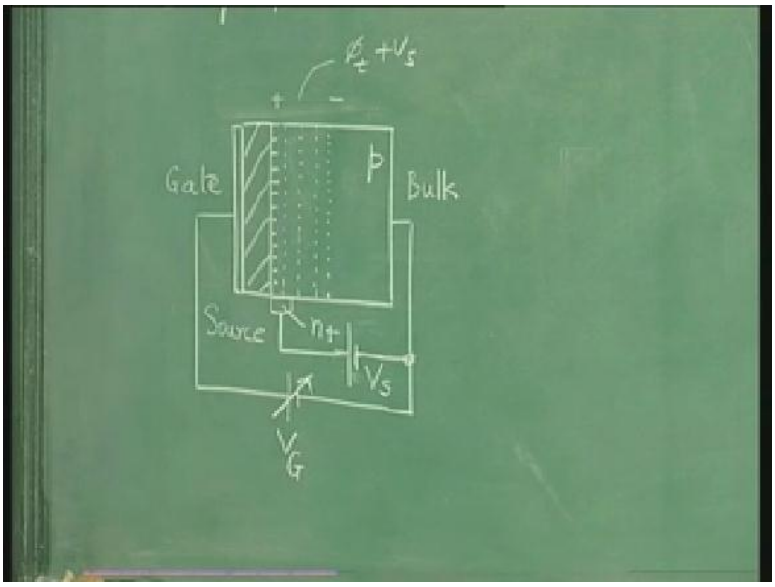

This is now a variable and this is a constant. What is the effect?
Now the effect will be that your depletion region will start increasing from 0. It will continue to increase until you have your gate voltage equal to the threshold voltage as explained earlier and as written in this expression. So until you reach this value of V_T your depletion width will go on expanding. So your depletion region first is here for small V_G then it expands further you increase your V_G. Now what is important is this will continue to expand until you reach V_G is equal to V_T taking into account the effect of V_S so that will be a larger V_T than the V_T that you had for V_S is equal to 0. So this will continue until that point and then an inversion layer will appear here. So, when the inversion layer appears that is when the threshold is reached then your voltage drop here will be phi_t plus V_S. Hence, the depletion region keeps on expanding until the voltage drop in silicon reaches phi_t plus V_S and thereafter an inversion layer develops. This can also be shown using a space charge diagram.

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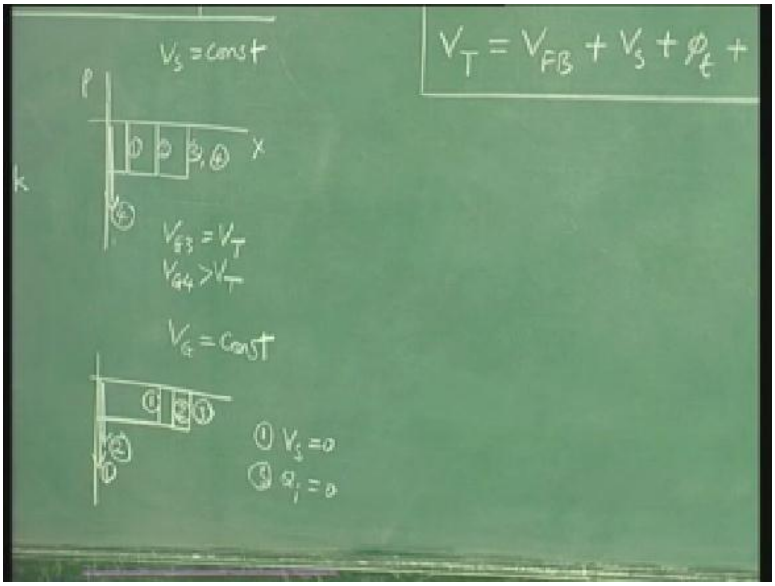

We are drawing this space charge conditions when V_S is constant and V_G is varying. So here what is happening is, you have a depletion layer like this to start with for one value of V_G and you go on increasing your V_G you have depletion region expanding until you come to threshold. Beyond threshold the depletion region stops expanding and you have the inversion charge. So let us call this 1, this is 2, this is 3 and this is also 4 because your depletion region almost stops expanding beyond threshold so 4 is into threshold. So V_{G3} is equal to V_T including the body effect and V_{G4} is greater than V_T. So, if you apply even higher voltage this inversion charge will go on increasing. Exactly similar diagram if you would like to draw for the condition V_G is constant and V_S varying this is what we had discussed earlier. So to complete the explanation we will draw that diagram also. That diagram would look something like this.

So first you are starting with the condition V_S is equal to 0 therefore if your depletion width was this much the device was inverted and therefore you had this charge, so this is the depletion width beyond threshold in inversion because this corresponds to V_S is equal to 0 and this is also 1. So 1 is V_S is equal to 0. Now you are going on increasing your V_S so what happens is this is expanding. So this is 2 and inversion charge is decreasing simultaneously. And for 3 which corresponds to threshold you reach the same depletion layer here that you had assuming that this V_S is the same as this V_S corresponding to this.

You started with a smaller depletion layer thickness than this because 1 corresponds to V_S is equal to 0 whereas this threshold condition corresponds to some value of V_S. So here when you keep V_G constant and you go on increasing your V_S your depletion region expands and inversion charge goes on falling. For 3 the inversion charge is 0 so we are not showing 3 here and this is a threshold condition. Therefore in summary that is the body effect. Many times the body effect is derived with the help of energy band diagram. We have avoided the use of energy band diagrams because the explanation in such a manner is simpler. So one can also use an energy band diagram and one can get the same information as well as some more additional information. Now let us do a simple numerical example to illustrate the body effect.

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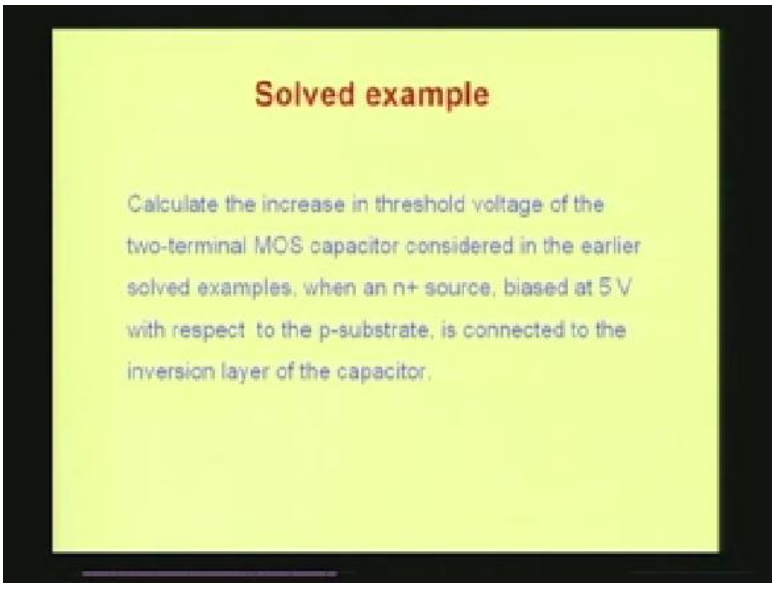

This is the example:
Calculate the increase in threshold voltage of the two-terminal MOS capacitor considered in the earlier solved examples when an n plus source biased at 5V with respect to the p-substrate is connected to the inversion layer of the capacitor.

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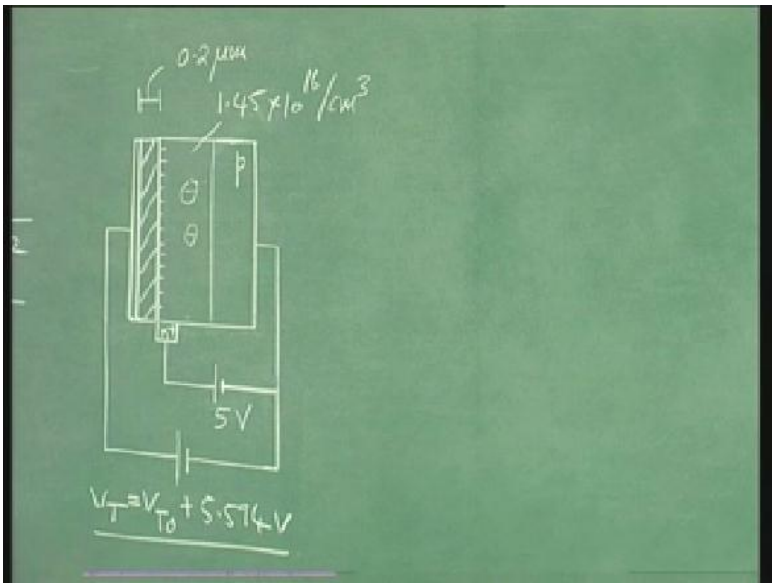

This is the diagram; this is the MOS capacitor, p-type substrate doping level 1.45 into 10 to the power 16 cm cube and oxide thickness of 0.2 micrometer. You are connecting an n plus source to the inversion layer which may form at the interface and we are applying 5V. We want to know because of the connection of this particular power supply and source how will the threshold voltage increase?
Threshold voltage is the voltage you must apply here so that you get an inversion layer. Of course when you have an inversion layer you will also have a depletion layer. Now let us look at the equation we have derived for this particular purpose.

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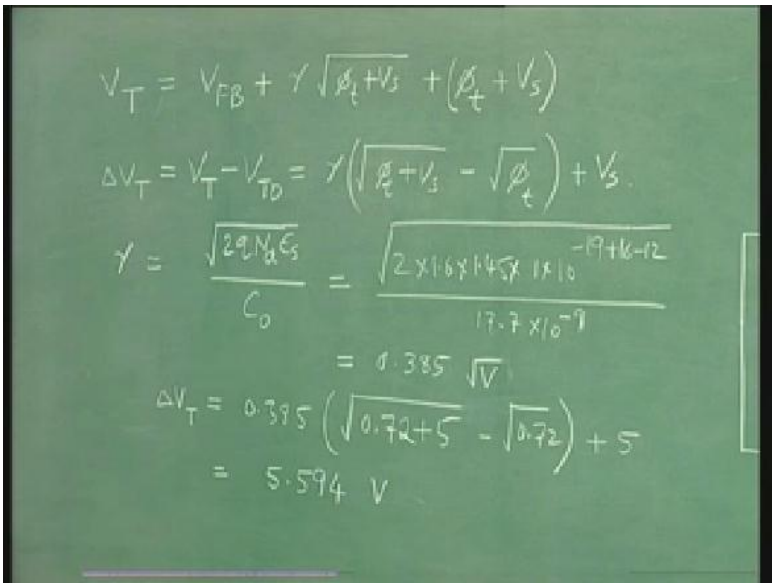

This is the expression for threshold voltage and this is the expression for change in threshold voltage. So you find, in the expression for change in threshold voltage we have only the source voltage V_S and the voltage drop in the semiconductor at inversion when the source voltage is 0 that is phi_t and the parameter gamma which contains the doping level of the substrate and the oxide capacitance. So you do not have the Flat-band voltage term coming in here. This means that for an ideal capacitor and for a real capacitor the change in threshold voltage with the source bias or the body effect is same.

Now let us substitute the values here; so gamma is equal to square root of 2 into 1.6 we collect the powers separately 10 to the power minus 19 into 1.45 10 to the power 16 into 10 to the power minus 12 by 17.7 into 10 to the power minus 9 F cm. So you check whether dimensionally this is correct. I am not using the dimensions here but you must put the dimensions and check. So, when you solve this you will get the result as 0.385. Now what will be the unit of this body effect parameter?

Please note from here that the unit of gamma into this quantity should be volts and that is the left hand side which is also the other term here. Since this is root volts obviously gamma should also be square root volts. So that is the body effect parameter gamma. Now you substitute this gamma here and you will get delta V_T is equal to 0.385 into square root of phi_t was about 0.72 plus V_S is 5 minus square root of 0.72 plus 5 that is the V_S here and this will turn out to be 5.594V so that is the increase in threshold voltage. The threshold voltage with respect to bulk has increased by 5.594V which is the new threshold voltage. Now, with this we come to the end of the discussion on body effect.

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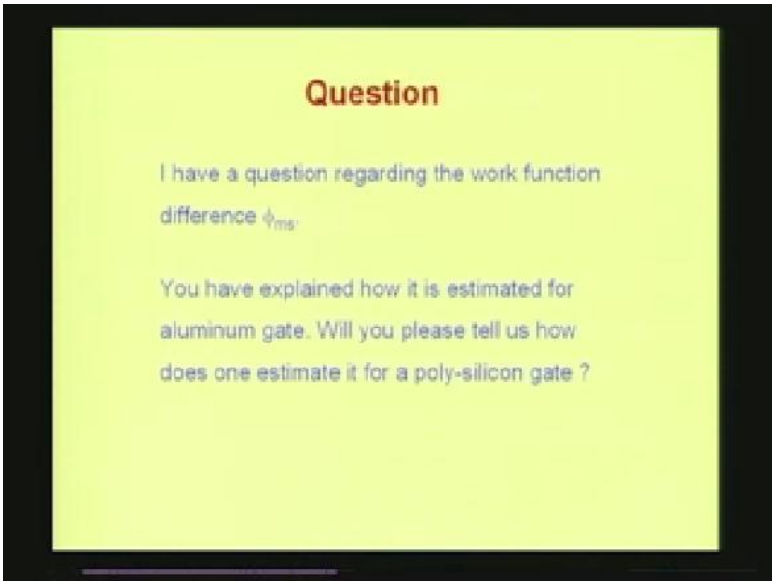

Student: Sir I have a question regarding the work function difference phi_{ms}. You have explained how it is estimated for aluminium gate. Will you please tell us how does one estimate it poly-silicon gate? The procedure for estimating phi ms for poly-silicon gate is very similar to that for a metal.

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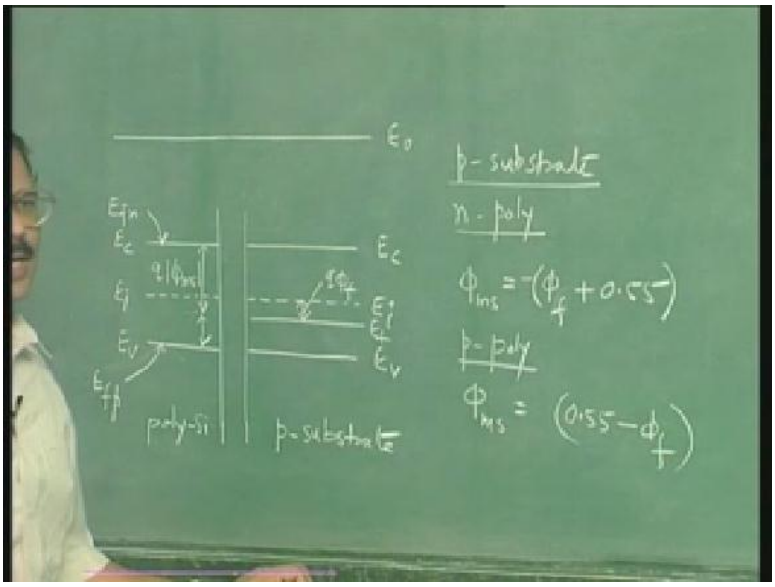

Look at this energy band diagram. This is p-type substrate and on the left hand side you have the poly-silicon gate. Now the poly-silicon gate is either heavily doped n-type or heavily doped p-type. Now please note that the poly-silicon gate is always heavily doped because its resistivity should be low, it should act like a conductor like a metal. So, unless you dope it heavily you will not get this low resistivity. Now generally if the poly-silicon gate is heavily n-type then the Fermi-level is assumed to coincide with the conduction band edge. So E_{fn} is here. On the other hand, if it is heavily doped p-type the Fermi-level is assumed to be at the valance band edge.

Once you know the location of the Fermi-level you can easily determine the phi_{ms}. For example, for n-type poly-silicon gate and p-type substrate the phi_{ms} is this much in magnitude. So you can write the phi_{ms} as, for n-ploy phi_{ms} is equal to this phi_f plus this half of the energy gap that is 0.55V so it is phi_f plus 0.55. Now E_f in the poly is above E_f in the semiconductor. So phi_m which is this difference is less than phi_s which is the difference between E_0 and E_f. Therefore this is negative in polarity so we are assuming a p-substrate. Similarly, if you have p-poly and p-substrate then from here it is clear that this is your Fermi-level difference, this and this. Now here your phi_m is more than phi_s. So this difference is 0.55 that is half of energy gap minus phi_f. So phi_{ms} is equal to 0.55 minus phi_f. Now let us see the next question.

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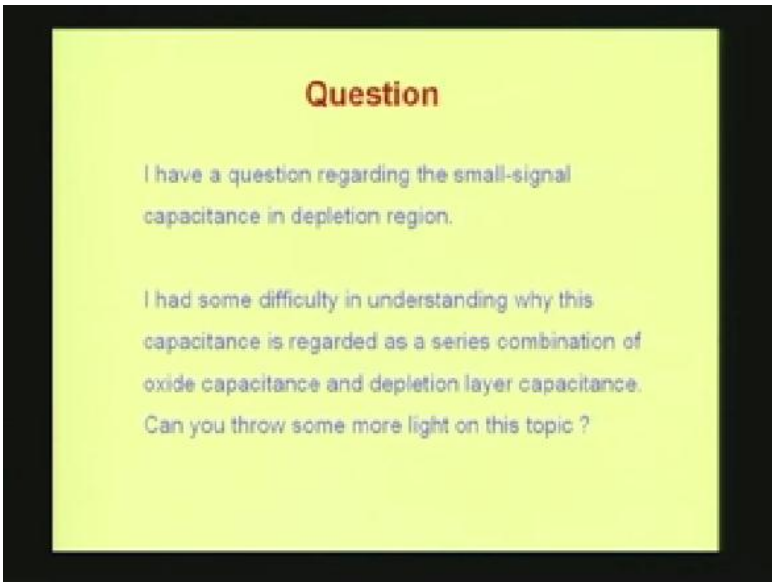

Student: Sir I have a question regarding the small-signal capacitance in depletion region. I had some difficulty in understanding why this capacitance is regarded as a series combination of oxide capacitance and depletion layer capacitance can you throw some more light on this topic. Let us understand your question with the help of this diagram.

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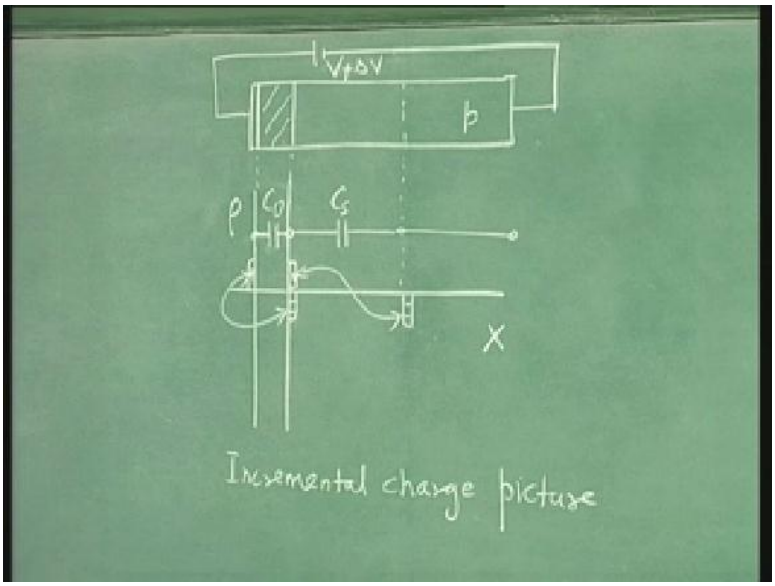

This is the incremental charge picture. That is, you have a MOS capacitor which is operating in a depletion region. So this is a depletion layer. The voltage applied is V, you make an incremental change in voltage and as a result you get a change in the charge. This is a change in the charge picture for increment delta V shown here. Now this is the picture relevant to the small-signal capacitance. You want to know why the charge here at the gate and a compensating charge at the edge of the depletion layer results in a capacitance of this MOS capacitor which is a series combination of the oxide capacitance and the depletion layer capacitance. You want to understand how this is possible.

A very simple way of explaining this is as follows:
Supposing you introduce a negative charge at the interface equal to the positive charge here and you also superimpose on this negative charge a positive charge which is equal to the magnitude of this negative charge. Now these two charges are equal, the positive charge here and negative charge here are equal. Therefore these two are equal and therefore in effect we have not introduced any charge because this plus this is 0. But now supposing you pair up these two charges they amount to a capacitance equal to the oxide capacitance here C_0. Then you pair up these two charges, they amount to capacitance here, this is the semiconductor or depletion region capacitance. Therefore the capacitance of the MOS capacitor in depletion is a series combination of these two between this point and this point which is the same as this point. Now with this we have come to the end of this discussion on MOS capacitor. Let us quickly summarize what we have achieved in the last few lectures.

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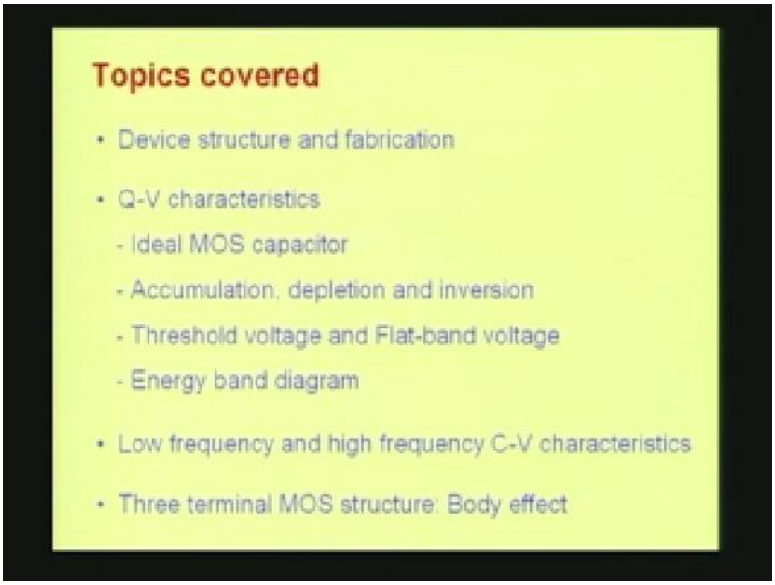

First we discussed the structure and fabrication of the MOS capacitor. Then we considered its DC characteristics charge versus voltage wherein we defined an ideal MOS capacitor and then we showed the meaning of a non-ideal MOS capacitor. We considered the accumulation, depletion and inversion regions of operation. We defined the threshold voltage and Flat-band voltage.

We also drew the energy band diagram because we showed that if you want to understand the work function difference contribution to the Flat-band voltage you have to understand the energy band diagram. The work function difference is nothing but a built-in voltage of the MOS junction. Then by differentiating the charge versus voltage or the Q - V characteristics we obtained the low frequency C - V characteristics. Then we explained why the high frequency C - V characteristics are little bit different than low frequency.

More specifically under high frequencies the capacitance in inversion saturates to the value of the capacitance at threshold. Then finally we considered the body effect where we saw the effect of introducing a third-terminal which makes contact with the inversion layer and biasing this third-terminal with respect to the substrate. In the next lecture we will start the discussion of the MOS field effect transistor.