Solid State Devices
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Lecture - 36
Metal-Oxide-Semiconductor (MOS) Junction
(Contd..)

In this lecture we will continue the discussion on the MOS junction or capacitor.

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Let me remind you the target shown on the slide which is the explanation of the C - V characteristics.

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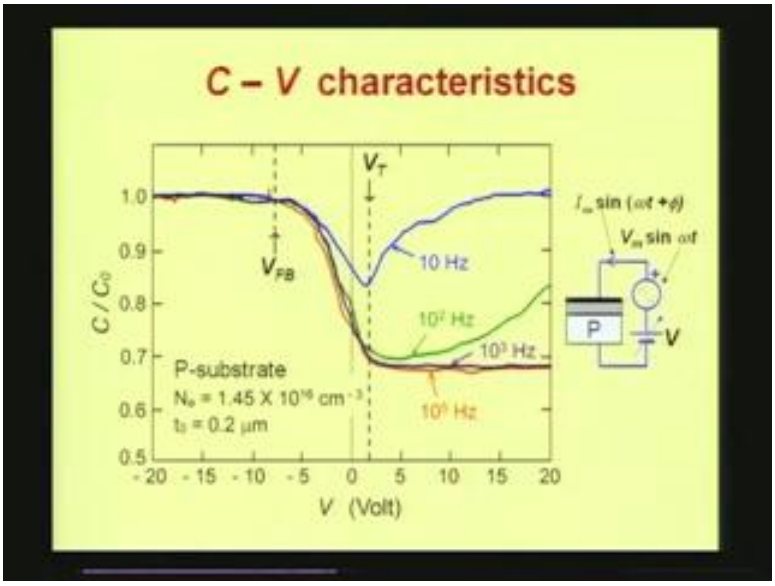

So far we have discussed a number of ideas and concepts which will help us to explain these characteristics. Let us summarize what we have achieved so far.

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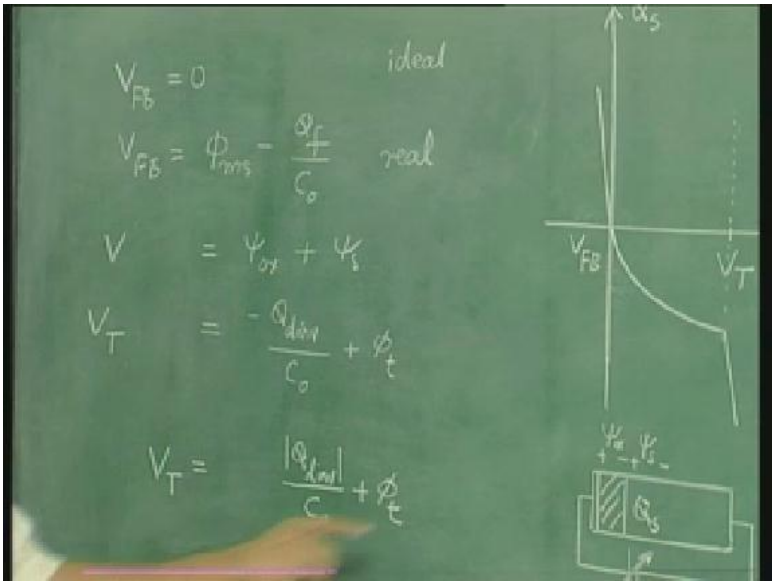

In the last class we explained that for ideal MOS capacitor Flat-band voltage is 0 but for the real MOS capacitor Flat-band voltage is given by phi_{ms} minus Q_f by C_0. Therefore for ideal MOS capacitor the basic equation for the applied voltage is V is equal to psi_{ox} plus psi_s as shown in this capacitor here.

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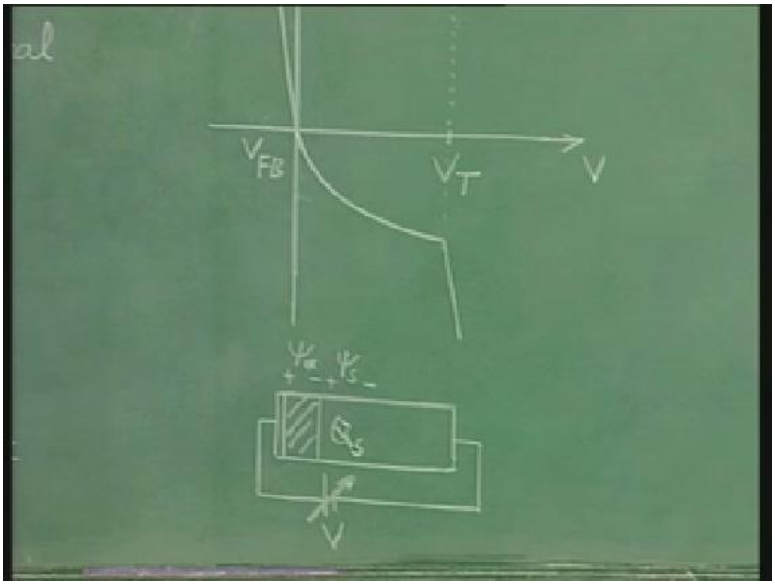

The psi_{ox} is the potential drop across the oxide and psi_s is a potential drop across silicon. Now this is the equation for ideal capacitor.

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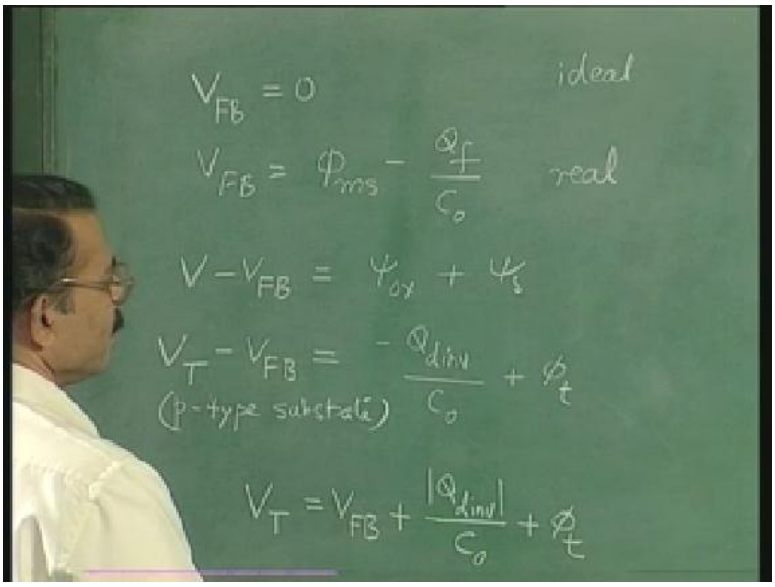

For a real capacitor all that you do is you replace V by V minus V_{FB}. Similarly, the ideal MOS capacitor equation for threshold voltage V_T is equal to minus Q_d inverse by C_0 plus phi_t is changed to V_T minus V_{FB} equal to the right hand side here. So, this is more of a general equation for threshold voltage. Now please recall that we are doing all our analysis for p-type substrate. So unless otherwise stated we are assuming a p-type substrate and the equations we show will be valid for p-type substrates. Therefore the expression for V_T can be written as V_T is equal to V_{FB} plus this quantity which is the quantity for ideal MOS capacitor. It is useful to write this charge in terms of the modulus because then we will find that we can write the equation very easily for n-type capacitor also and then show that just the signs change to negative signs here that accounts for a capacitor which has an n-type substrate. So here this is p-type substrate that we must note.

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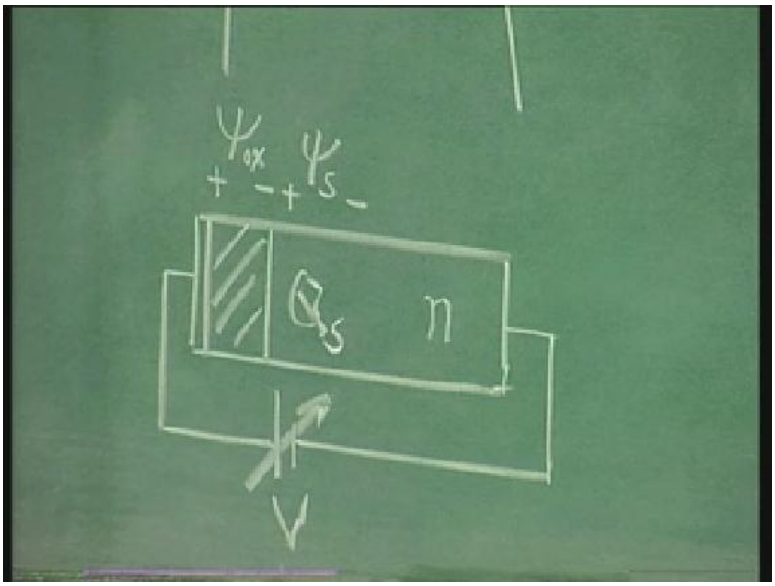

Now what will happen to an n-type substrate?

If the substrate is n-type then, please note here in terms of this diagram, for creating an inversion layer in an n-type substrate you will have to apply a negative voltage because inversion layer in n-type substrate means holes at the interface. To get positive charge in silicon you should apply negative voltage.

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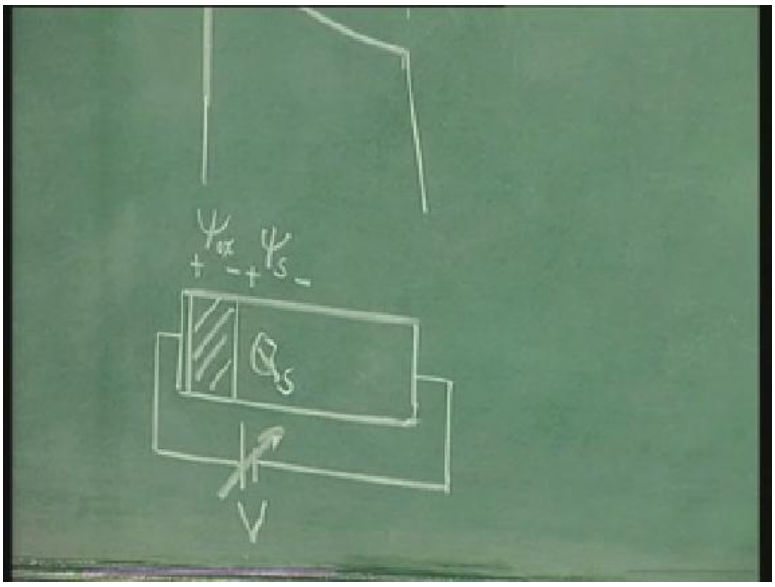

So, for n-type substrate what will happen is the psi_{ox} and psi_s will be negative because the applied voltage is also negative.

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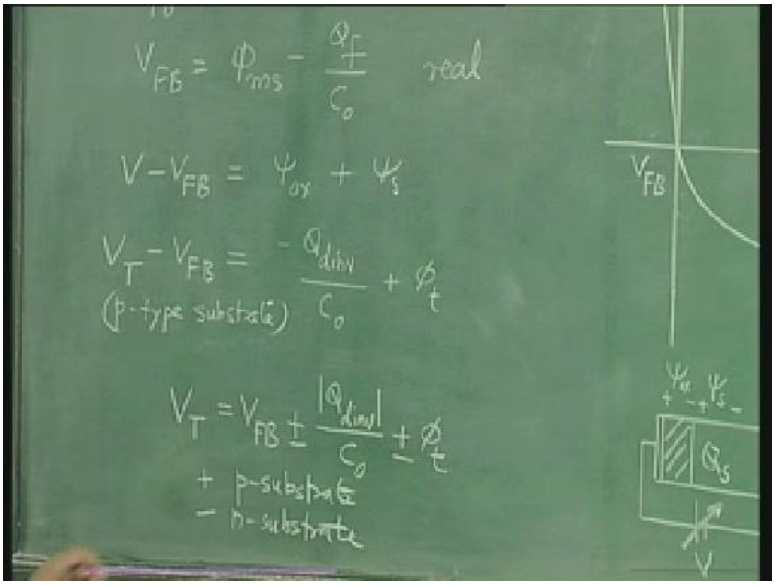

Therefore this equation just gets modified to V_{FB} minus Q_d inverse by C_0 minus phi_t. Here positive sign applies for p-substrate and negative sign for n-substrate. Notice that this is modulus of depletion charge at inversion for which you have written an equation already in terms of the doping.

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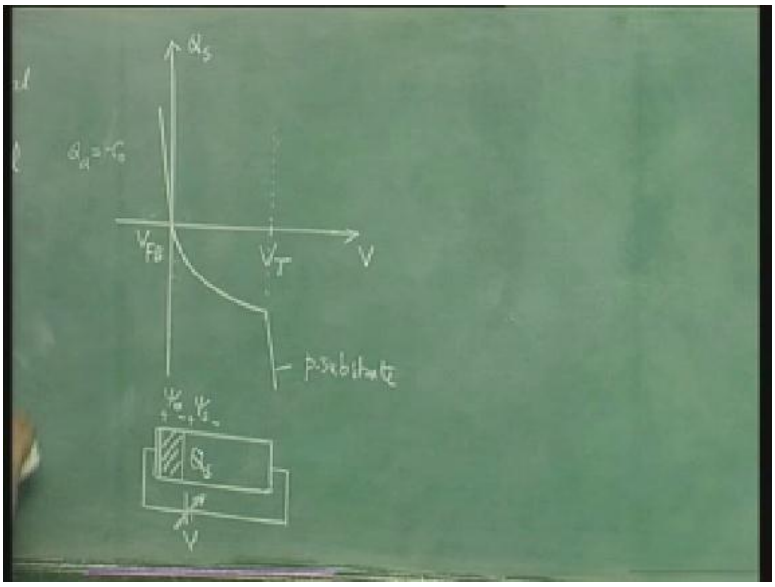

Now, coming to the Q - V relation this is the Q - V relation for p-type substrate where the charge is 0 for voltage is equal to V_{FB} and beyond threshold you have inversion. Please recall that the slope of this line which is an accumulation and the slope of this line which represents the inversion charge both these slopes are the same because the equation for this is Q accumulation is equal to minus C_0 into V minus V_{FB} whereas the equation for inversion is Q_i is equal to minus C_0 into V minus V_T.

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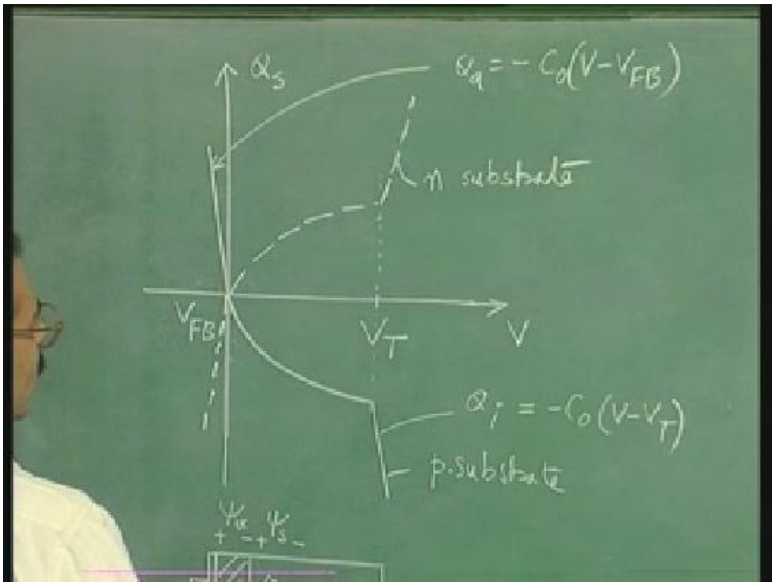

So please note that if you differentiate this expression with respect to voltage and you differentiate this expression with respect to voltage you will get the same slope and that would be the capacitance C_0. On this diagram if you want to draw the picture for n-type capacitor it would be the following. So, for the n-type capacitor the accumulation charge is negative because if substrate is n-type then accumulation means electrons. Therefore it is simply a reflection of this curve on this voltage axis like this the n-type substrate. So, that

summarizes our discussion so far. Now, before we take up the capacitance voltage characteristics based on this charge versus voltage characteristics let us explain why this term phi_t here in the threshold is also referred to as $2phi_f$. What is this $2phi_f$? To understand this we should look at energy band diagram.

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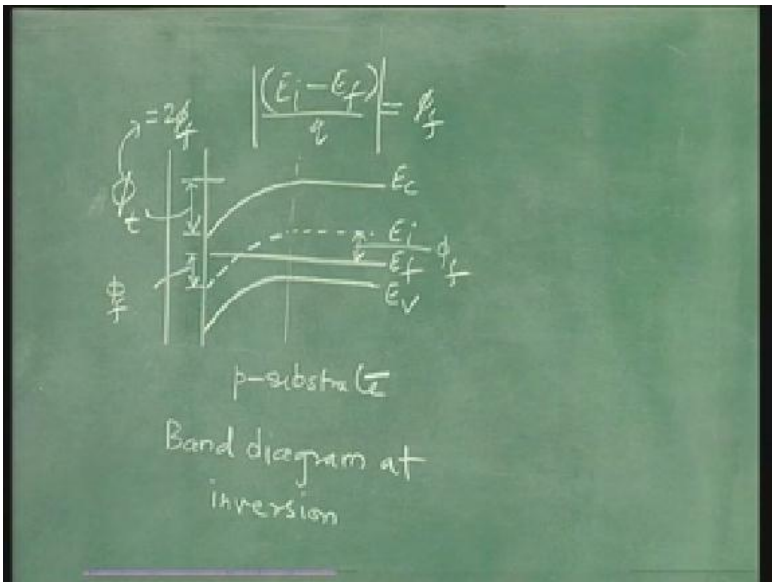

Look at energy band diagram at inversion. Supposing I assume a p-type substrate then at inversion the energy band diagram is as follows. You first draw the Fermi-level, in the bulk these are your bands. Now at the interface what you know is that the surface concentration of electrons is equal to the bulk concentration of holes. So let us draw the intrinsic level here in between. And now this difference indicates the bulk concentration of holes, the difference between E_i and E_f. So here your intrinsic level should cross this E_f and come down so that the surface becomes n-type to the same extent as it is p-type in the bulk. Therefore your band diagram at inversion would be something like this. So this is p-substrate band diagram at inversion. This distance is equal to this distance. It ensures that n_s is equal to p_0. Now this difference E_i minus E_f is referred to as the phi_f into Q. So E_i minus E_f the difference between Fermi-level and intrinsic level this difference is normally referred to as the Fermi-level the symbol phi_f. Therefore you see that if you want to know the total potential drop in silicon on the band diagram this is the total potential drop. So this is psi_s, this is phi_f and this is phi_f.

Now obviously this psi_s is nothing but this difference here between this intrinsic level and this point so this is equal to $2phi_f$ at inversion so this is phi_t. And this psi_s we can also call as phi_t and that is $2phi_f$. Now, in our nomenclature what we will do is we will take the modulus of this and call it as phi f because clearly if you take an n-type substrate the Fermi-level in the bulk would be above E_i and therefore this phi f according to the definition E_i minus E_f by Q would be negative. So, to avoid confusion we will use phi_f as the magnitude of the difference between E_i and E_f. So this is the reason why this phi_t is also written as $2phi_f$ where phi_f is V_T l_n doping by n_i. Now this doping could either be acceptor type or donor type. So we can write here suffix a or d because for both this formula is valid.

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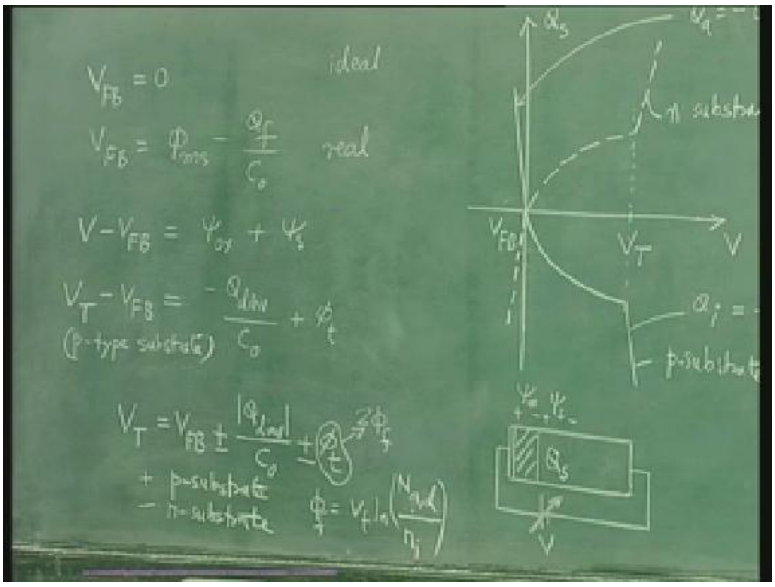

Now we are ready to discuss the capacitance voltage characteristics based on the Q - V characteristics. A simple way of deriving the capacitance voltage from the charge voltage is as follows:

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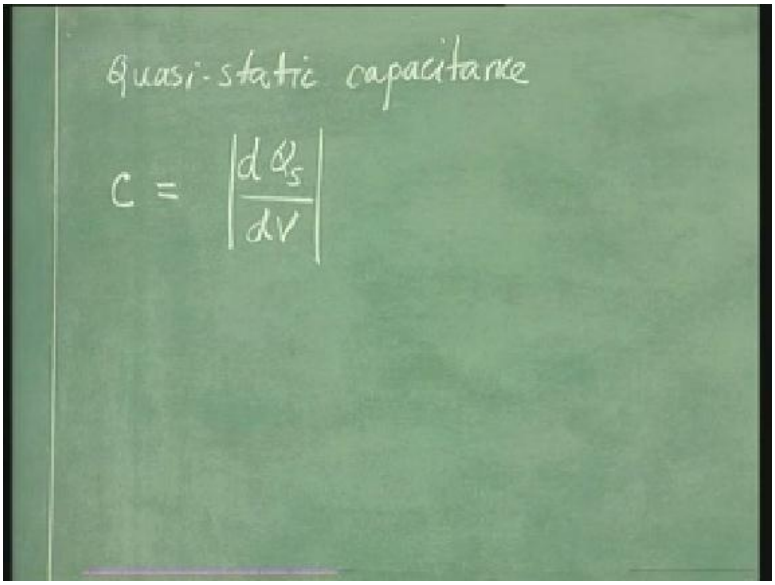

We can write the capacitance as dQ_s by dV with a modulus. So this is the so-called Quasi-static definition of small signal capacitance. The Quasi-static capacitance if you recall in the context of PN junctions was also the small signal capacitance. So Quasi-static also means a small signal capacitance at low frequencies because this Q versus V corresponds to DC conditions. So when you obtain a capacitance by differentiating DC conditions it is said to be a Quasi-static capacitance or it is equivalent to saying it is a low frequency capacitance. You are changing the voltage very slowly so that always almost steady state remains and then you are deriving the capacitance from the changes in the charge because of changes in the voltage.

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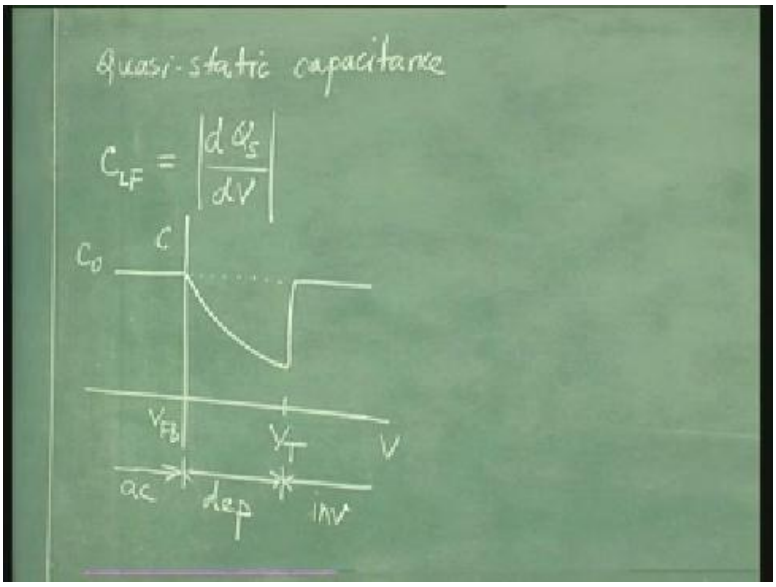

So this is also the low frequency capacitance. We will indicate it by putting a suffix LF. So, if you differentiate this curve let us take the p-type substrate. You take this curve and you differentiate this curve, now what kind of shape will you get? When you differentiate this you get the capacitance as C_0 which is clear from this equation and when you differentiate this you again get C_0 from this equation. So in between you have a variation. You find this slope here varies from C_0 and it decreases, as you can see the slope here is decreasing up to some point and then it abruptly changes to C_0. So we can plot this behaviour as follows: This is C_0, this is Flat-band voltage and this is the threshold voltage V_T then the capacitance falls so this is how the shape is and beyond this it will abruptly rises again back to C_0, so this is C versus V, the behaviour we get for low frequency capacitance from differentiating here like this.

Now, what is the meaning of this? The meaning of this capacitance is that when you make changes in the voltage initially the change in the charge because of change in voltage is coming from the interface that is why the capacitance is C_0. That is, in terms of this diagram here when you make a change in the voltage in the accumulation region the changes take place right at the interface. Now, when you move into the depletion region, this is the depletion region between V_{FB} and V_T and this is the accumulation. When you move to the depletion region you find that the capacitance is falling.

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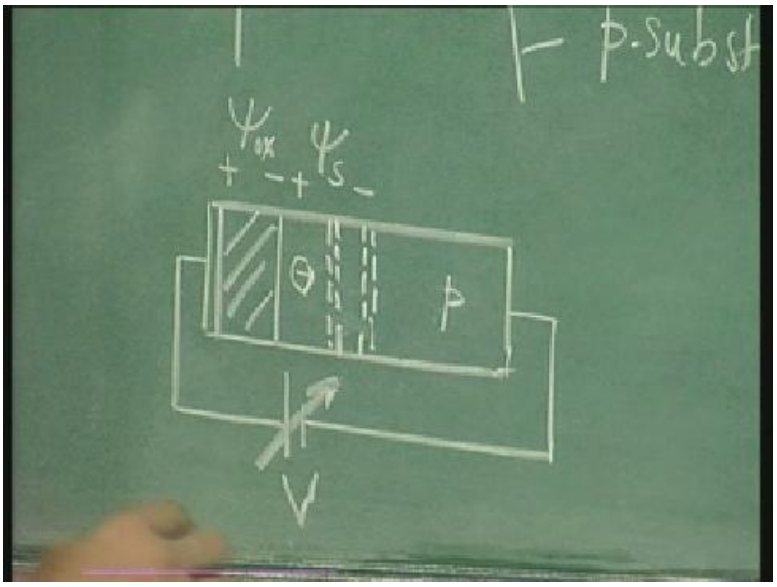

Now what is the reason? The reason is as follows: If you look at this MOS capacitor when the device is in depletion you are creating a depletion layer and this is the charge, you are taking a p-type substrate of ionized impurities. When you make a change in the voltage there is a change in the charge and that change occurs at the edge of the depletion layer. Therefore, if you take only the changes you find there is a change in positive at the gate located here and there is a change in negative charge in the semiconductor located at the edge of the depletion layer. So here evidently the capacitance is smaller than the oxide capacitance because this is the distance between the changes in the charge that is the incremental picture. Now let us draw the incremental charge picture for increment in the voltage.

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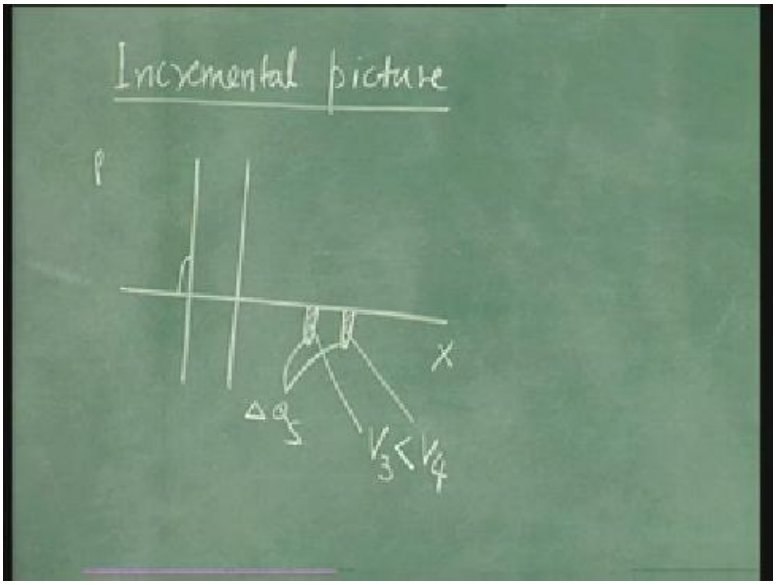

So this incremental picture is as follows: This is the oxide layer and what we are showing is the space charge versus distance but in the incremental picture. So, when the device is in depletion you have positive charge here at the gate and a negative charge here at the edge of

the depletion layer so this is for depletion as we explained based on this diagram. Now, as your voltage increases you find that the capacitance keeps falling until you come to the edge of the depletion layer or when you come to threshold. So what is happening here in terms of this diagram is that the depletion width is expanding and the increment therefore takes place at the edge of this depletion layer. So, for a higher voltage when you make a change delta V in the voltage the change delta Q_s in the charge takes place at a farther distance from the interface. This is what is shown here.

The increment in the positive charge is always at the gate here, so this is delta Q_s in response to delta V. This is again another delta Q_s and this is for one voltage and this is for another voltage. Supposing you call this voltage V_3 and this voltage V_4 this V_4 is on the verge of just below threshold so we are following our nomenclature 4 was always supposed to be near the threshold so it is V_3 less than V_4 is the increment in the charge. This explains why the capacitance goes on falling because this distance between the incremental charges is falling and this is what the capacitance is.

Now, what happens beyond this threshold is you get inversion. Now in inversion the capacitance is rising up to C_0. This means that the incremental charges are now coming from the interface. So let us look at this diagram here, what this means is that though you have the depletion layer, let us say this is the depletion layer edge at inversion, so when you make an increment the increment is coming from the mobile charges here rather than by the increment in depletion layer or from ionized impurities, because beyond V_T you are getting a large number of mobile charges at the interface and it is easier to get the increment from these charges.

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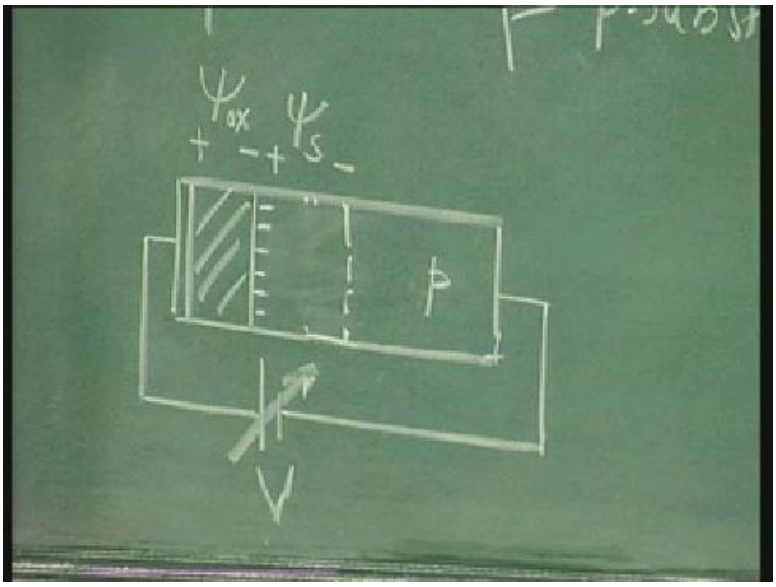

Now since the increment is coming from these charges your capacitance is again corresponding to C_0. This is what we will show here. This whole thing is for depletion, for inversion the incremental picture is this.

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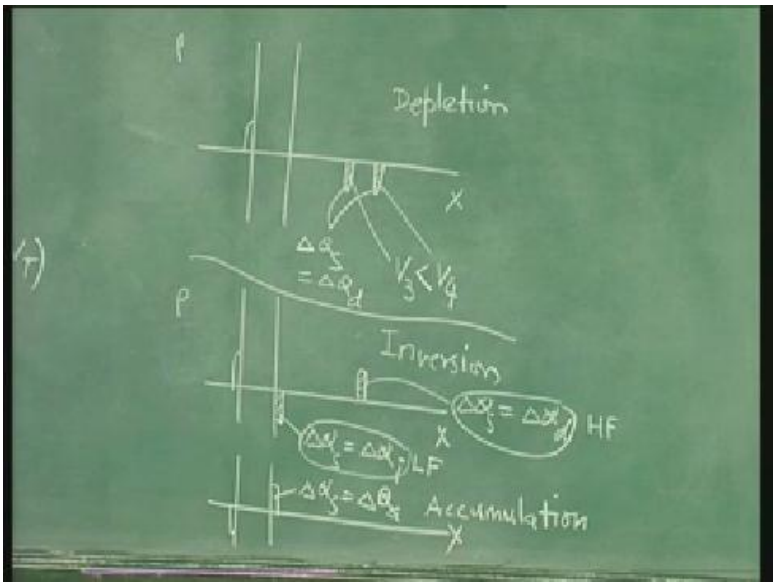

So this is your delta Q_s and this delta Q_s is equal to delta Q_d whereas this delta Q_s is equal to delta Q_i change in the inversion charge. So you are not having any change in the depletion charge here so this is for depletion and this is for inversion. Now for accumulation let us complete the picture. For accumulation it would be exactly similar to this except the polarities reversed. For accumulation you have negative charge in the gate and positive charge in the semiconductor so this is delta Q_s is equal to delta Q_a. This explains the qualitative behaviour of capacitance as a function of voltage at low frequencies.

Now if you look at the capacitance voltage diagram here the experimental characteristics, you will find that the behaviour of the capacitance shown by the blue line corresponds to low frequencies. Here you do not see very abrupt change of the capacitance this is gradual. Now this is because the frequency is not low enough. Quasi-static means the frequency is very low 1 hertz or even less because the frequency should tend to 0 for quasi-static operation. So such a capacitance versus voltage curve is difficult to measure at such low frequencies. That is why you are not able to see this kind of abrupt change going up here but you see that the capacitance in inversion the maximum capacitance here is same as the capacitance at accumulation. Here we have plotted C by C_0. Since C is equal to C_0 separation C by C_0 is one in accumulation and in inversion. Now what we need to explain is, why is that for high frequencies the capacitance does not go back to C_0 but saturate at the point where it comes to the edge of depletion layer. Let us explain why this happens.

Once the capacitance is in inversion if the frequency is high then you cannot provide changes in the mobile carriers at the interface very easily. This is because the mobile carriers at the interface in inversion are minority carriers. And you recall our discussion of majority and minority carriers we had said that minority carriers are thermally generated. The majority carriers are derived from the ionized impurities but minority carriers are obtained by thermal generation. Therefore to generate the required number of minority carriers it takes time. If you change the voltage very fast then you are not providing sufficient time for the minority carriers to be generated. Therefore if you make a rapid change in the voltage in inversion then your change in charge cannot come from this inversion layer. But the change in charge has to be there because when you change the voltage there will be change in charge on the gate.

Now that change in charge which is required to compensate the change in charge in the gate in the semiconductor that compensating charge in the semiconductor comes from the edge of depletion layer because you can change the majority carrier charge very quickly so you can easily get charges by moving the mobile majority carriers away. It is difficult to get change in charge by moving the mobile minority carriers but mobile majority carriers can be very quickly change in concentration. Therefore at high frequencies the change in the charge in response to change in the charge in the gate comes from the edge of the depletion layer. In inversion this is the picture at low frequencies delta Q_s is equal to delta Q_i. This happens at low frequencies but at high frequencies it is not this, it is here delta Q_s is equal to delta Q_d at high frequencies.

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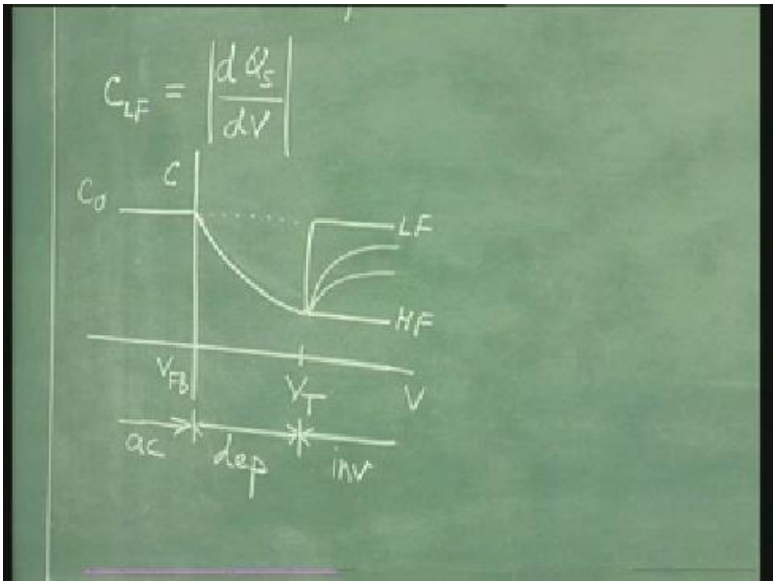

That is why if you see the capacitance voltage curve as shown here the capacitance voltage curve will just stop changing beyond threshold because the incremental charges are coming from the edge of depletion layer which means the capacitance therefore saturates to the value at this point because the edge of the depletion layer is not changing much in inversion. The width of the depletion layer is saturating so here we can therefore put, this is low frequencies and this is high frequencies. So, in between when you make a change from high to low frequency of course you will have a gradual change which is something like this. Now this is exactly what you find in the slide here. So you find that when you change your frequency from high value to low value progressively you are getting these curves.

Of course what you find is that the minimum here is not the same as this value so we will not bother about such details because to explain those you will have to go into more rigours theory. Here all that it means is, that if your capacitance is not really of low frequency your curve may actually come like this and go up.

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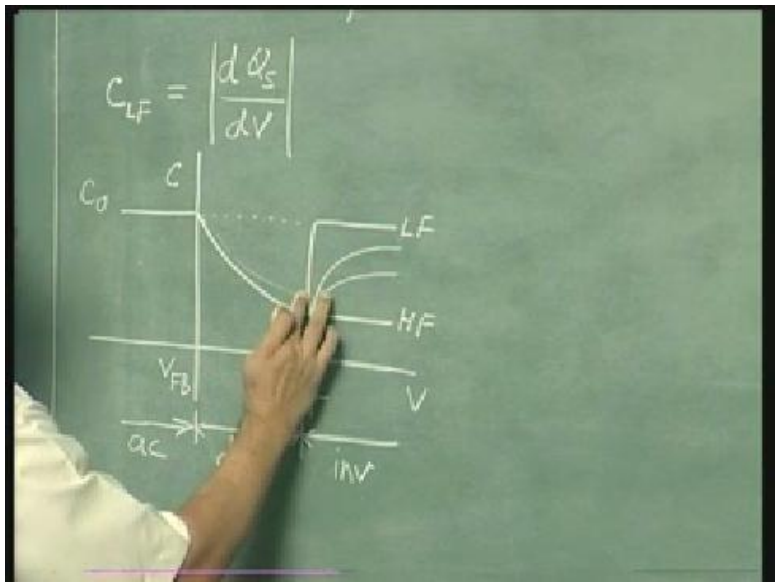

This is our capacitance versus voltage behaviour, qualitative terms, high frequency and low frequency. What is the expression for capacitance versus voltage in depletion because here the complete the picture if you want a quantitative analysis we must have equation for this curve C versus V then we can easily get all the parameters of this capacitance versus voltage curve. That is the next topic, derivation of the expression for capacitance as a function of voltage in depletion.

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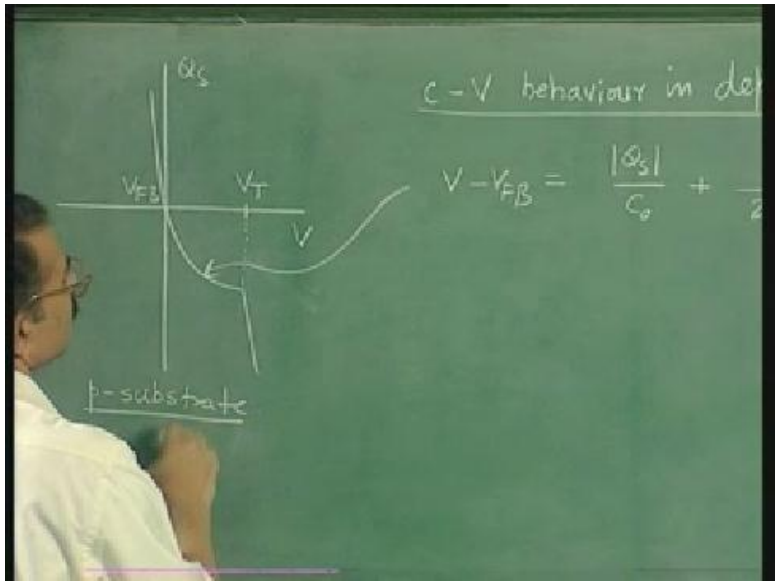

C - V behaviour in depletion:
We start with the equation for charge versus voltage in depletion that is here. This equation for charge as a function of voltage is V is equal to minus Q_s by C_0 plus Q_s square by 2q epsilon$_s$ N_a this is for an ideal capacitor and for a real capacitor you subtract Flat-band voltage from here. Now it is useful to write this formula in terms of the modulus. So when

you take the modulus you can remove this because you know that when you take a p-type substrate these two terms are both positive.

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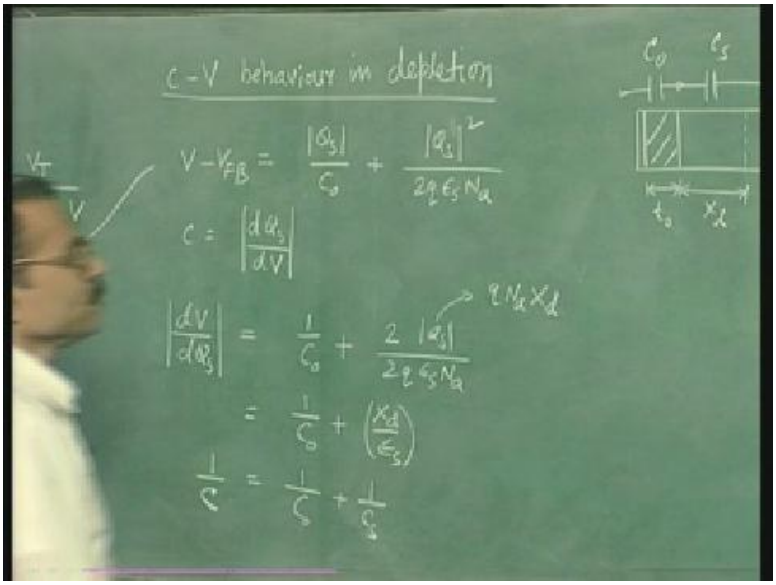

They represent the potential drop in the oxide and in silicon. Starting from here the capacitance is given by d[Q_s by dV] by a Quasi-static approach. Now here you will find that since the voltage is known in terms of the charge on this side a simple approach to derive this capacitance would be to differentiate this equation with respect to charge so that we get dV by dQ_s that is 1 by C. So when you do that differentiation you will get dV by dQ_s is given by with a modulus and that is why we are using a modulus here. You can use a modulus here also because it is a square it does not matter whether Qs is positive or negative. So when you differentiate you will get here 1 by C_0 plus differentiation of this would be $2Q_s$ by 2q epsilon$_s$ into N_a. Now you recognise the fact that this modulus of Q_s is nothing but q N_a into X_d where X_d is the width of the depletion layer in the MOS capacitor.

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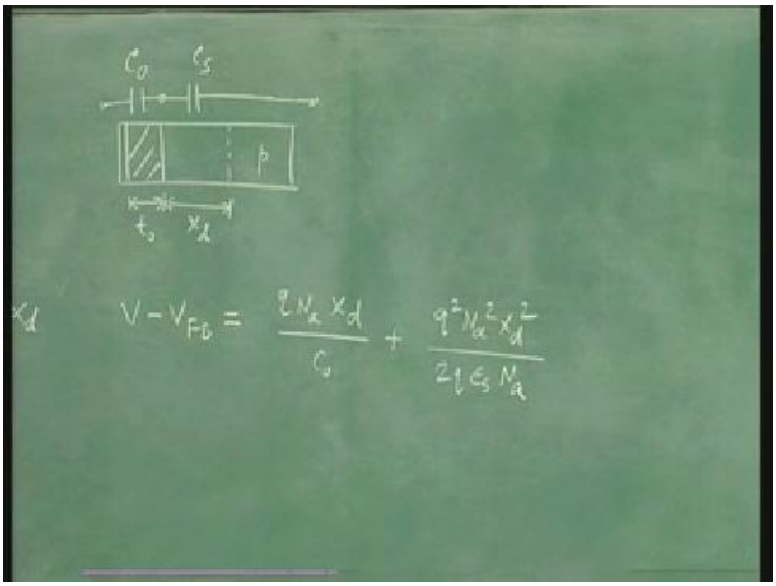

So this is your MOS capacitor, this is your depletion layer and this is your X_d. This is a p-type substrate so doping here is N_a. So q N_a X_d represents the depletion charge here. So you can interchange Q_s and Q_d because in depletion the charge in silicon is the depletion charge itself. This being the case you can write this as 1 by C_0 plus X_d by epsilon$_s$ because 2q N_a and 2q N_a will get cancelled and this is what you will get. Now you can identify this X_d by epsilon$_s$ as the capacitance associated with the depletion layer. So this is t_0 so you have a capacitance associated with this oxide layer and you have a capacitance associated with this depletion layer and both are in series. So this is C_0 and you can call this capacitance as C_s the capacitance associated with the semiconductor region. So we can write the same thing as 1 by C_0 plus 1 by C_s that is the overall capacitance. Now still we need to know this C_s as a function of voltage, C_0 is constant. To know this C_s as a function of voltage we need to know X_d as a function of voltage. Now X_d as a function of voltage is actually given by this formula where you can replace Q_s by q N_a X_d. So when you do that you will get V minus V_{FB} is equal to q N_a X_d by C_0 plus q square N_a square X_d square by 2q epsilon$_s$ N_a and here we can cancel q and N_a and then you divide both sides by q N_a.

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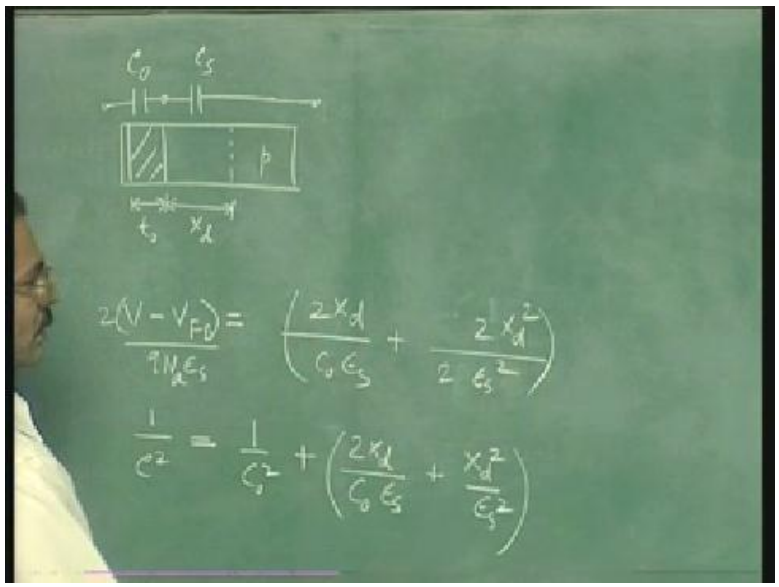

Now you get this equation. So this gives you X_d as a function of voltage. Now what you should do is, you look at this and then you can try to express C_s as a function of X_d in a simple was as follows. Supposing you square this equation which is the same as squaring this equation then you will get 1 by C square is equal to 1 by C_0 square plus $2X_d$ by C_0 epsilon$_s$ plus X_d square by epsilon$_s$ square. Now you have X_d and X_d square terms here like you have here, it does not take much time to see that if you multiply both sides by two and then you divide by epsilon$_s$ then this quantity ($2X_d$ by C_0 epsilon$_s$ plus X_d square by epsilon$_s$ square) is what you have here and here you can cancel the 2.

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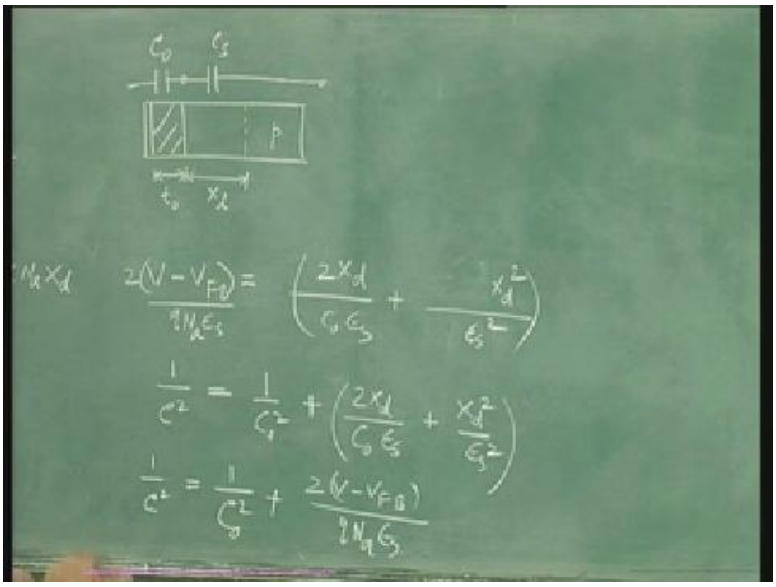

Since this quantity is this we can therefore get the equation 1 by C square is equal to 1 by C_0 square plus 2(V minus V_{FB}) by q N_a epsilon$_s$. So this is your equation for capacitance as a function of voltage. You can write this equation in a straight forward manner as C is equal to C_0 by square root of 1 minus 2(V minus V_{FB}) C_0 square by q epsilon$_s$ N_a this is the formula for capacitance as a function of voltage. According to this formula as your voltage increases this term increases.

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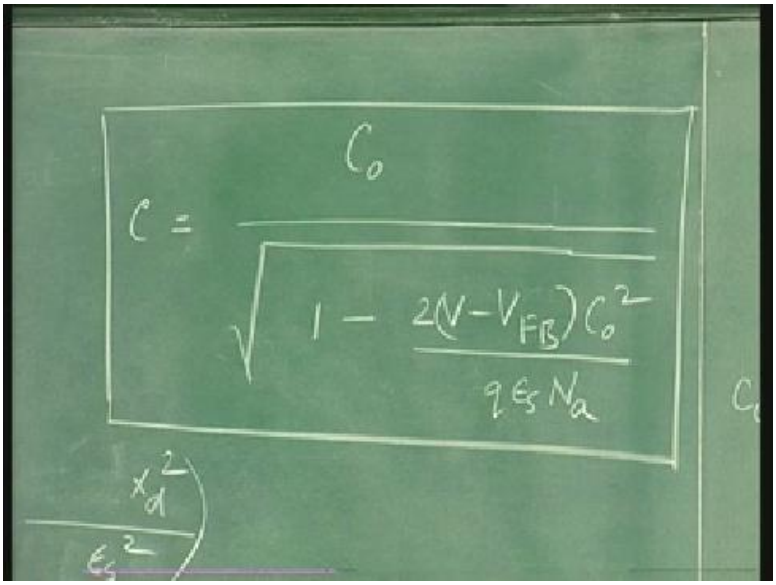

But then since there is a negative sign the whole quantity will decrease and capacitance will increase so this is not really correct but it should by a plus sign.

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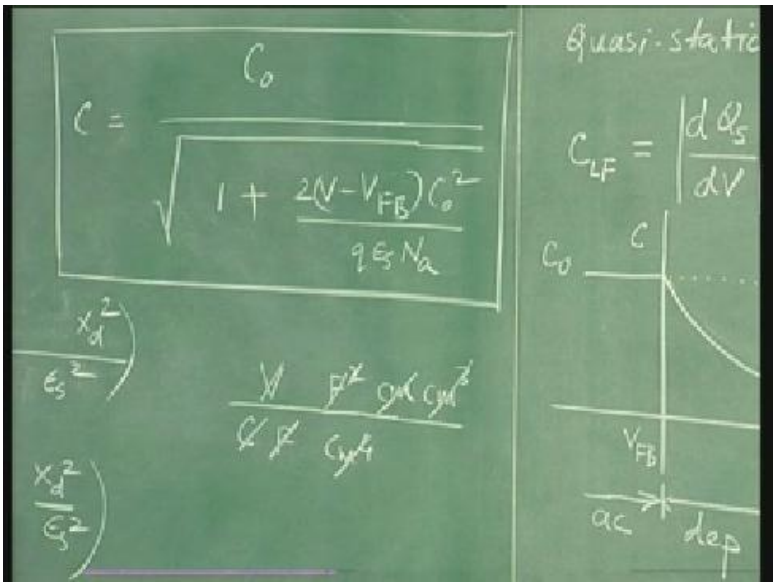

One must always check the formula by logical reasoning whether it shows the behaviour correctly and whether the positive and negative signs are correct. We must also check dimensionally. Let us make a dimensional check of this formula. So here this should not have any dimensions because you are adding 1 to this, then left hand side and right hand side will have the same dimensions. So here let us write the dimensions of these terms so V minus V_{FB} is volts. C_0 square is F square by cm power 4 because C_0 is F by cm square then q is Coulomb this epsilon is F by cm and this doping is per cm cube. So you have this cancelling here, this Farad cancels with one Farad there and Farad into volt is Coulomb so this cancels.

Now this means that this term is dimensionally correct. From here we can also get the value of the capacitance at threshold. At threshold all that you need to do is you must substitute V_T for this voltage V. Now this completes the capacitance versus voltage characteristics. Now let us do a solved example. Let us illustrate some of the ideas we developed.

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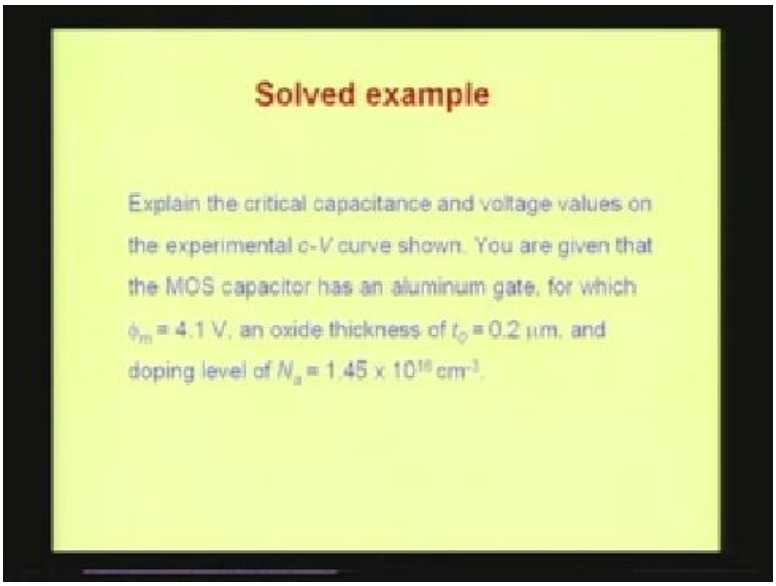

Explain critical capacitance and voltage values on the experimental C - V curve shown. You are given that the MOS capacitor has an aluminium gate for which phi m is equal to 4.1V and oxide thickness of 0.2 micrometer and doping level of 1.45 into 10 to the power 16 cm cube acceptance. So phi_m here is the work function. Let us take a close look at the capacitance voltage characteristics.

What are the critical values on this curve?
We will draw this curve on the board and mark the critical values from this slide and we will try to explain them.

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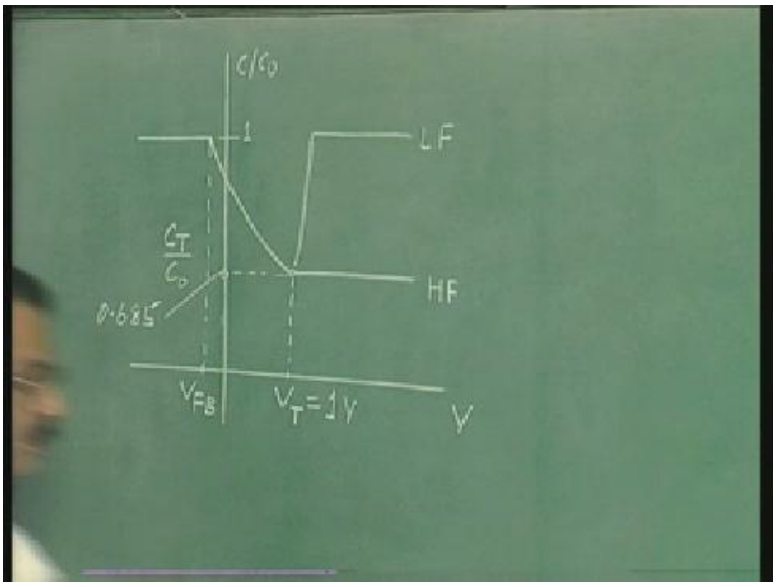

So the C - V curve is something like this if this is high frequency and for low frequency it goes up. So the critical values here will be, if you sketch C by C_0 versus V this value is 1, this is known then this is another critical value we have to explain. So let us call the capacitance at this point as C_T because the voltage here is the threshold voltage. So here this is C_T by C_0 so this is another critical value we need to note from our experimental characteristics. Then this is the Flat-band voltage. So the critical parameters we need to explain are: The value of the threshold voltage and the value of the capacitance at this point and then the value of the Flat-band voltage.

If you look at the C - V curve on this slide we obtain a value here to be close to about 0.68 or 0.69 or 0.685 this is the ratio of the capacitance to the oxide capacitance at the threshold voltage point. Now what you note is that the threshold voltage is more easily noted from the low frequency curve than from the high frequency curve. This is because it is difficult to know where exactly it has stopped changing or where exactly it is saturating. Whereas in the low frequency curve you have a sharp change here that enables you to locate the threshold voltage. Now, this threshold voltage is approximately about 1V. We want to explain why this is 1V and why this value which is C_T by C_0 is 0.685.

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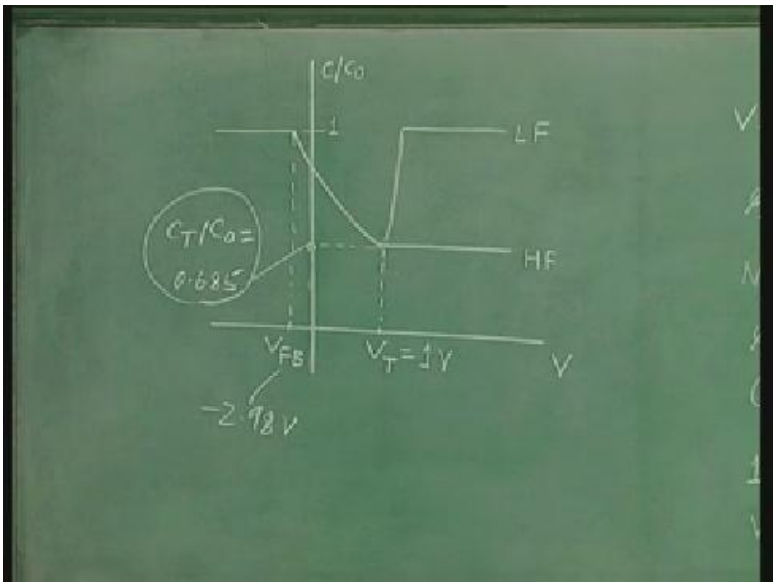

So we are able to locate this V_T from the low frequency curve rather than from the high frequency curve and that is the advantage of the low frequency curve that it enables you to locate the threshold voltage point rather precisely on a C - V plot. Now what about the Flat-band voltage? Let us look at this curve. Like it is difficult to locate the threshold voltage on the high frequency C - V curve it is difficult to locate the Flat-band voltage on the C - V curve.

Both low and high frequency C - V curves at Flat-band point and below Flat-band point are same. This is because you really do not know where the curve has started increasing. Though we have shown the Flat-band point to be somewhere here you really cannot locate it precisely. You can even move it to the right but we do not know exactly where the Flat-band point is. So let us try to see whether from these parameters we can extract the value of the Flat-band voltage from the other values that is the threshold voltage and the value of the capacitance at threshold. Let us start with the threshold voltage.

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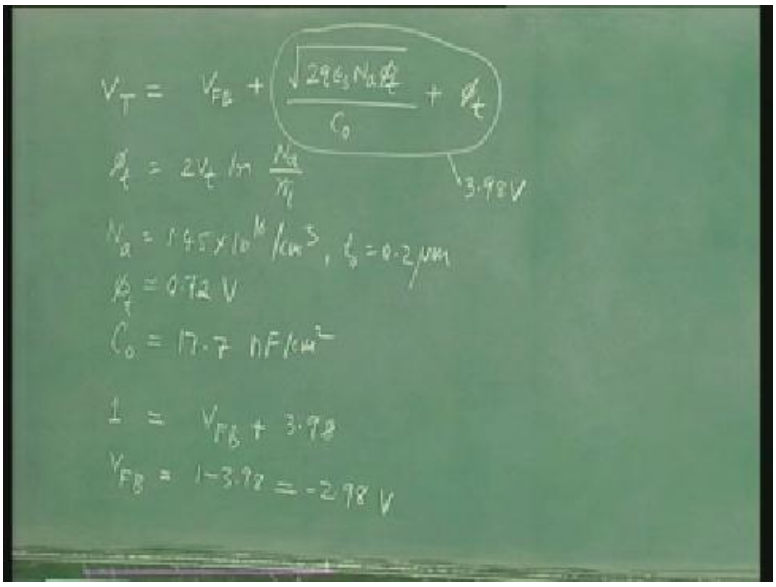

The expression for threshold voltage is V_T is equal to Flat-band voltage plus square root of 2q epsilon$_s$ N_a into phi$_t$ by C_0 plus phi$_t$. Now we are given the value of the doping level. From there we can also get phi$_t$ because phi$_t$ is equal to $2V_t$ l_n N_a by n_i. Now for N_a is equal to 1.45 into 10 to the power 16 cm cube we have already done the calculation of this quantity and this quantity. So we have obtained phi$_t$ to be about 0.72 V and C_0 we have already determined to be 17.7 N_f cm square for t_0 of 0.2 microns. And in fact this is the so called ideal threshold voltage, this we had shown to be 3.98 V.

Now we want to explain why the threshold voltage is 1V and that is the value on our experimental curve. So clearly this is because of the presence of the Flat-band voltage. So we have the relation 1V is equal to Flat-band voltage plus 3.98 from where we obtained Flat-band voltage equal to 1 minus 3.98 which is minus 2.98 V. Now we need to see how we can explain a Flat-band voltage of this value.

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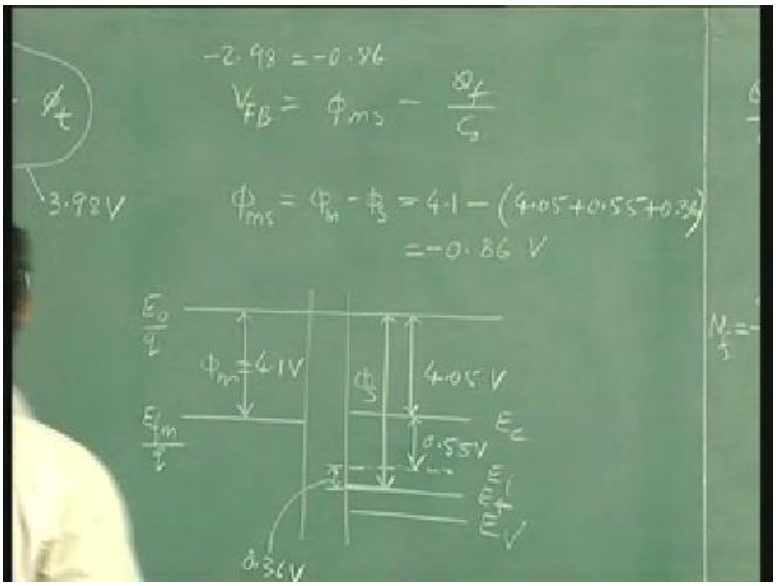

So the Flat-band voltage formula is given by phi_{ms} minus Q_f by C_0 of which we can determine phi_{ms} from the fact that the gate is made of aluminium. So, to determine phi_{ms} let us draw the band diagram. This is the Fermi-level in metal, this is the E_0 level, this quantity given to us is 4.1V so in terms of energy you will have to multiply it by Q. So what we are sketching is the potentials. Now suppose this is oxide layer on the semiconductor side you know that silicon has electron affinity of 4.05 electron volts so here it is in volts, this is K_i and this is E_c, this is your E_v and this is the intrinsic level and Fermi-level is here it is a p-type semiconductor.

Now this difference is phi_f which is half of phi_t. Now this phi_t is 0.72 V therefore this phi_f is 0.36 V. Now, to determine phi_{ms} this is phi_m and phi_s is this quantity. So to get this quantity we need this value because we know this value. Now this value is 0.55 V because it is half of energy gap of silicon. So now we can put this value, this value and this value together to get this phi_s and then we can get phi_{ms} so phi_{ms} is equal to phi_m minus phi_s that is 4.1 minus 4.05 plus 0.55 plus 0.36. Now this value turns out to be 0.86 V. So for phi_{ms} this quantity is 0.86 V. The Flat-band voltage we want to explain is minus 2.98 V. Now incidentally phi_{ms} is negative, phi_m is 4.1 this is actually negative so phi_m is less and phi_s is more. But still you cannot account for this 2.98 only from phi_{ms}. So, obviously there is a fixed charge Q_f.

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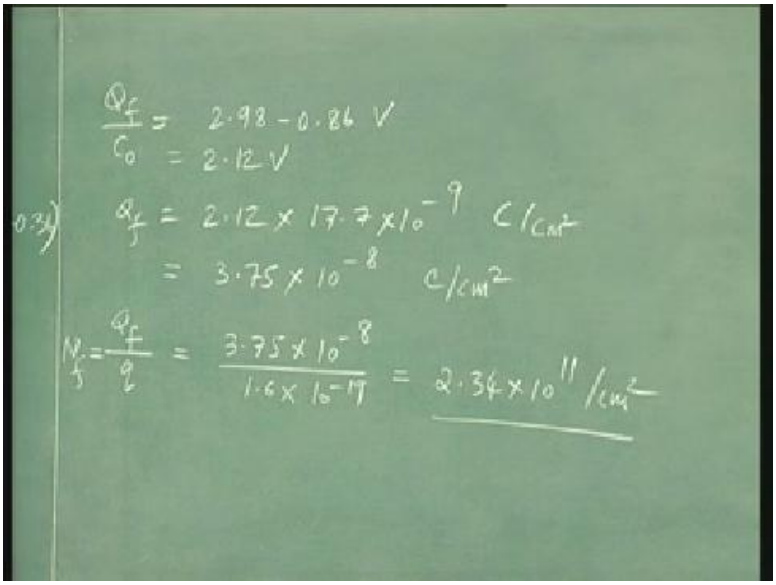

Now what is the value of the fixed charge?
We can write Q_f by C_0 is equal to 2.98 minus 0.86 V, this is 2.12 V. So Q_f is equal to 2.12 into 17.7 into 10 to the power minus 9 C by cm square because volts into Farad cm square is C by cm square. Now this is equal to 3.75 into 10 to the power minus 8 so this is the order of the fixed charge. It is customary to express this fixed charge in terms of the number of charges. So number of charges is obtained by dividing the fixed charge by the charge on an electron. So Q_f by q is the so-called N_f the number of fixed charges is equal to 3.75 into 10 to the power minus 8C by cm square by 1.6 into 10 to the power minus 19. Now this turns out to be 2.34 into 10 to the power 11 per cm square. That is the kind of N_f which is present. In the problem you are not giving the N_f because it is not very easy to determine N_f before you make the capacitor.

Unless your process is very standardized you do not know. You know the doping level of the starting semiconductor; you also know how much oxide you are growing, but this Q_f is very sensitive to the way you grow the oxide conditions, oxygen conditions during the oxidation and so on. That is why this N_f or Q_f has to be extracted by measurement. So, having explained the value of N_f now we can explain the Flat-band voltage. We have the Flat-band voltage equal to minus 2.98 here. So what we are left with now is this C_T by C_0. Let us see how we can get C_T by C_0. We can get it from the formula for capacitance as a function of voltage. So this is the formula for capacitance as a function of voltage, C_T is equal to C_0 by square root of 1 plus 2(V minus V_{FB})C_0 square by q N_a E_s.

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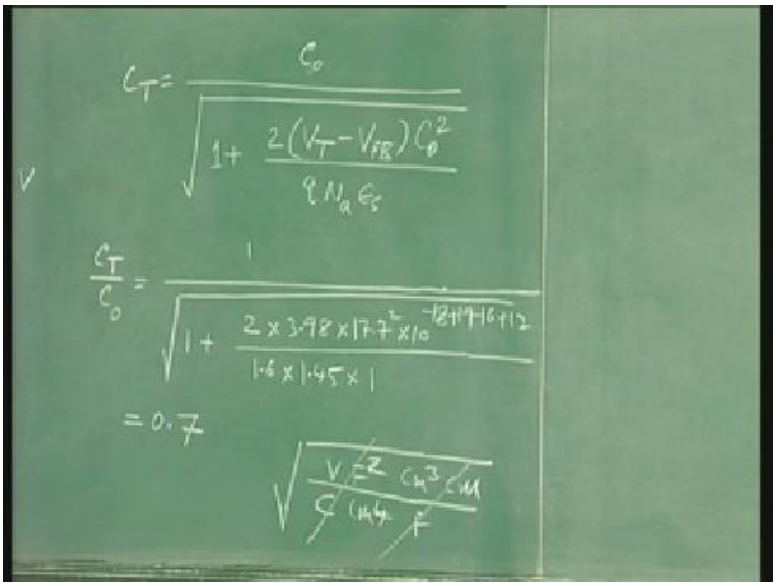

You want the capacitance at threshold so this is the formula. We have to substitute the various values here to get the ratio so we can write C_T by C_0 is equal to 1 by square root of 1 plus 2(V_T is 1V and V_{FB} is minus 2.98 V so this is 3.98 V, you must put the units here simultaneously)C_0 square that is 17.7 square into 10 to the power minus 18F per cm square so F per cm square by Q is 1.6 into 10 to the power minus 19 Coulombs so minus 19 goes here as plus 19 Coulombs into doping is 1.45 into 10 to the power 16 that goes as minus 16 over there cm cube.

And finally epsilon$_s$ is 10 to the power minus 12F by cm so that goes as 10 to the power 12 over there F by cm. So the formula is: C_T by C_0 is equal to 1 by square root of 1 plus 2 into 3.98 into 17.7 square into 10 to the power minus 18 plus 19 minus 16 plus 12 by 1.6 into 1.45 into 1. You check that all these cancel and you get a dimensionless quantity. Now you evaluate that quantity and you will get the value to be 0.7. Therefore here this value we get approximately 0.7 from calculations. So this is how we can explain the critical parameters on the capacitance voltage curve. There are some more aspects of this capacitance voltage curve that we will discuss in the next class.