

Solid State Devices
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Lecture - 35
Metal-Oxide-Semiconductor (MOS) Junction
(Contd...)

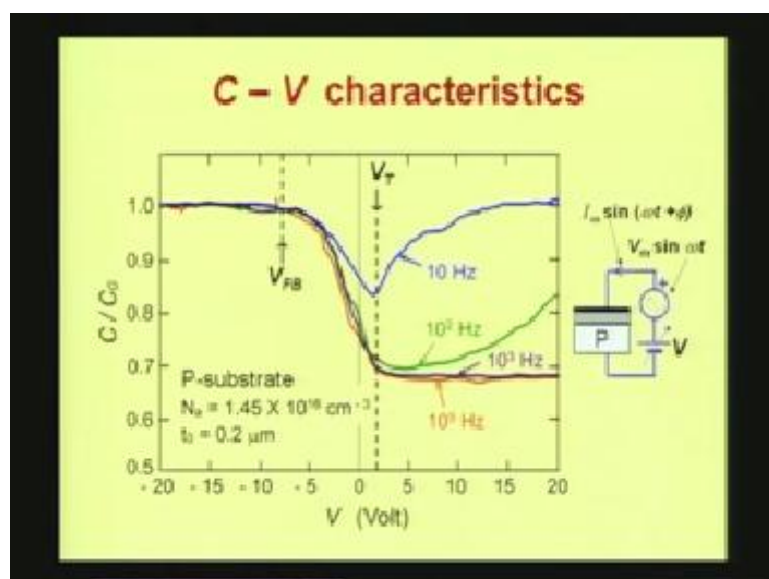
In the last few lectures we have been discussing about the Metal-Oxide-Semiconductor junction or capacitor.

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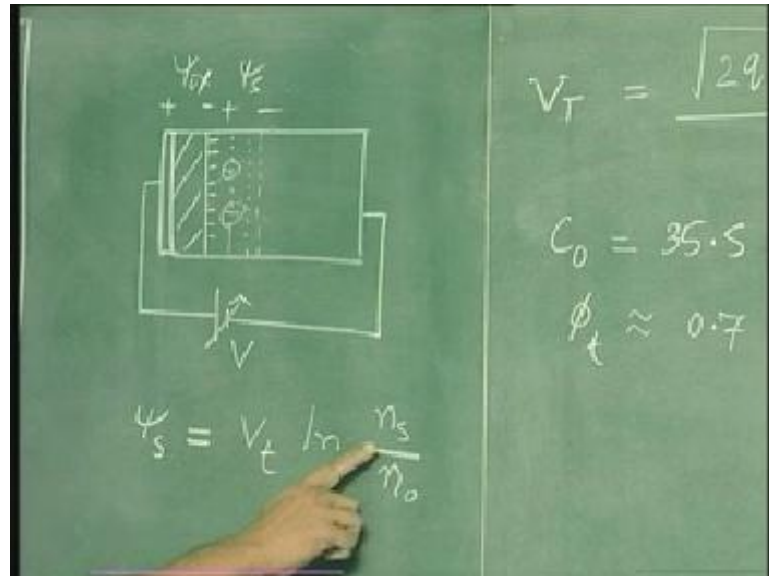
We shall continue this discussion in this lecture. Let me remind you that our goal of these discussions on these topics is to explain the C - V characteristics shown on the slide.

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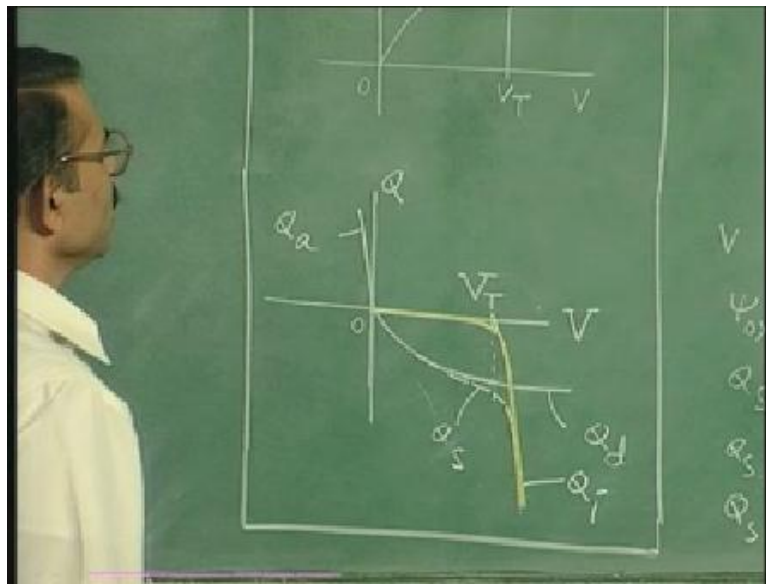
We are coming closer to this explanation. As a first step we said we will explain the charge conditions in the MOS capacitor as a function of the DC applied voltage and from there we will derive the C - V characteristics.

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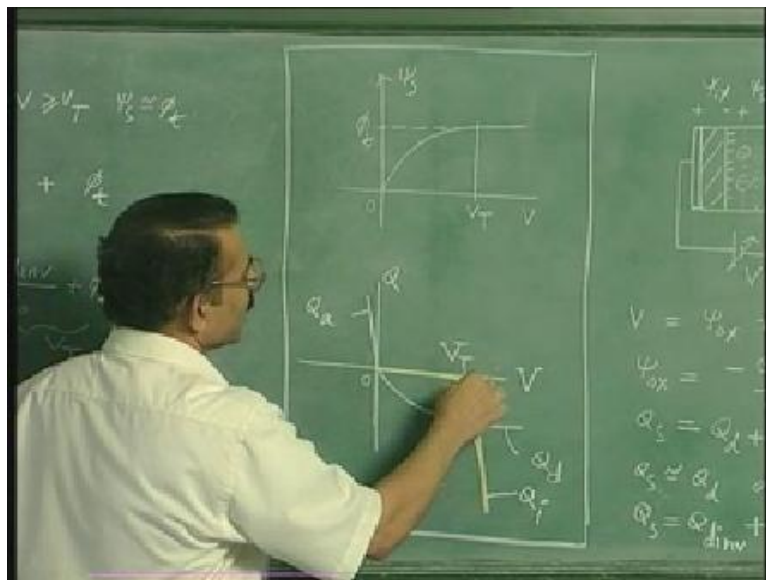
In the last class what we explained was the following: In a MOS capacitor when your voltage is greater than 0, then you have depletion and inversion, conditions. We discussed these conditions in detail and said the following: When you increase the voltage from 0 first the depletion region starts expanding, the charge in the semiconductor required to sustain this applied voltage comes from the depletion region because of ionized impurity atoms. Now this proceeds until you reach the threshold. Beyond threshold what happens is this depletion stops expanding and instead you have mobile electrons being attracted to the surface in large numbers. And beyond threshold it is this mobile electron concentration or inversion layer charge concentration that goes on increasing and the depletion layer concentration saturates. This was shown on a graph like this.

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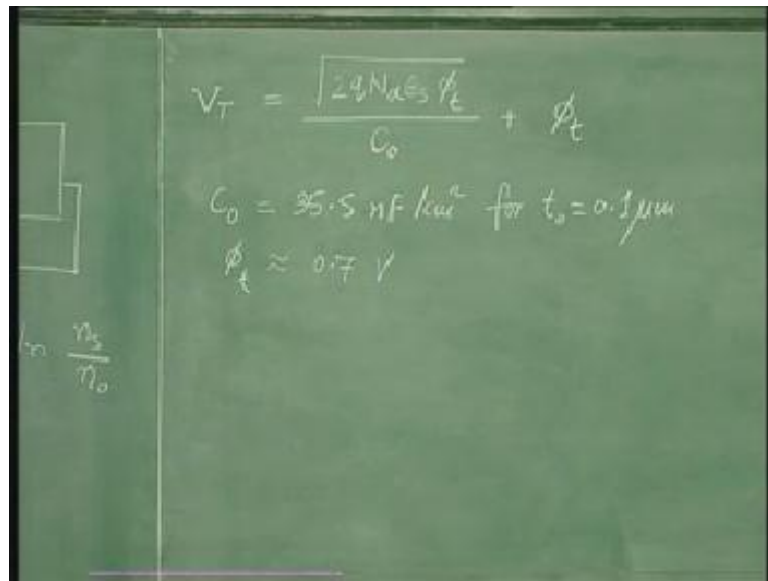
So here the depletion charge is saturating and the inversion charge Q_i is rapidly expanding beyond the threshold point. We also said that if you look at the voltages ψ_{ox} and ψ_s that is the potential drop across oxide and silicon as two components of the applied voltage then when you increase the voltage from 0 ψ_{ox} keeps monotonically increasing. Now ψ_s also increases in the beginning but beyond threshold voltage when the depletion layer almost saturates the ψ_s also saturates. This is what we said about ψ_s the surface potential.

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Beyond threshold it saturates to a value ϕ_i . This saturation is approximate of course whereas this ψ_{ox} keeps increasing continuously because the silicon charge as a whole which is the sum of the inversion charge and depletion charge keeps increasing though the depletion charge saturates beyond threshold. Now we also derived an expression for V_T as well as this ϕ_i .

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$$V_T = \frac{\sqrt{2qN_a\epsilon_s\phi_t}}{C_0} + \phi_t$$

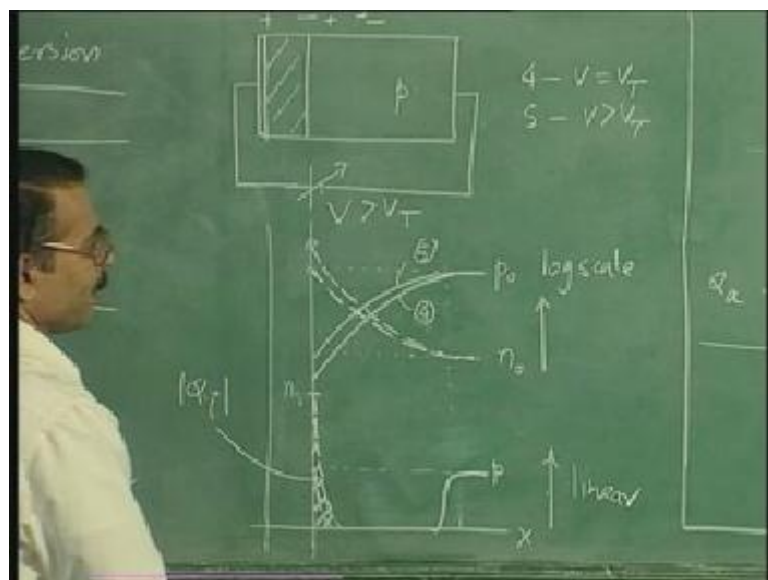
$$C_0 = 35.5 \text{ nF/cm}^2 \text{ for } t_{ox} = 0.1 \mu\text{m}$$

$$\phi_t \approx 0.7 \text{ V}$$

$$\ln \frac{n_s}{n_0}$$

Now this expression was V_T is equal to square root of $2q N_a \epsilon_s \phi_t$ by C_0 which is oxide capacitance plus ϕ_t . This is the ψ_{ox} and this is ψ_s at inversion. You must remember two numerical values for any calculation related to MOS capacitors. One is the oxide capacitance for 0.1 micron oxide thickness which is about 35.5 nF by cm square and the ϕ_t is approximately 0.7V. It would be useful to remember these two values. Now, in this lecture we would like to derive expressions for Q_d as a function of voltage and Q_i as a function of voltage that is our first exercise in this lecture. Before we take that up let me explain one doubt. That is, how ψ_s almost saturates when your inversion charge is increasing?

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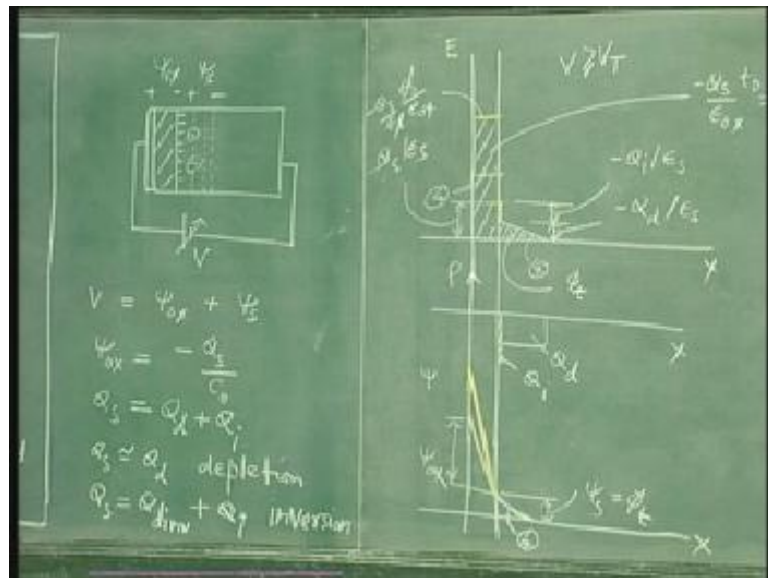


The doubt is, when you increase the voltage beyond threshold this electron concentration is going on increasing so n_s is going on increasing. Now if n_s is going increasing how can ψ_s be constant?

Here ψ_s and n_s are related by the Boltzmann relation ψ_s is equal to $V_t \ln n_s$ by n_0 . That is, if you look at this diagram ψ_s is given by the ratio of this surface concentration to n_0 and logarithm of this ratio multiplied by the threshold voltage. So, if n_s increases ψ_s should also increase but we are saying ψ_s is almost becoming constant how is this possible?

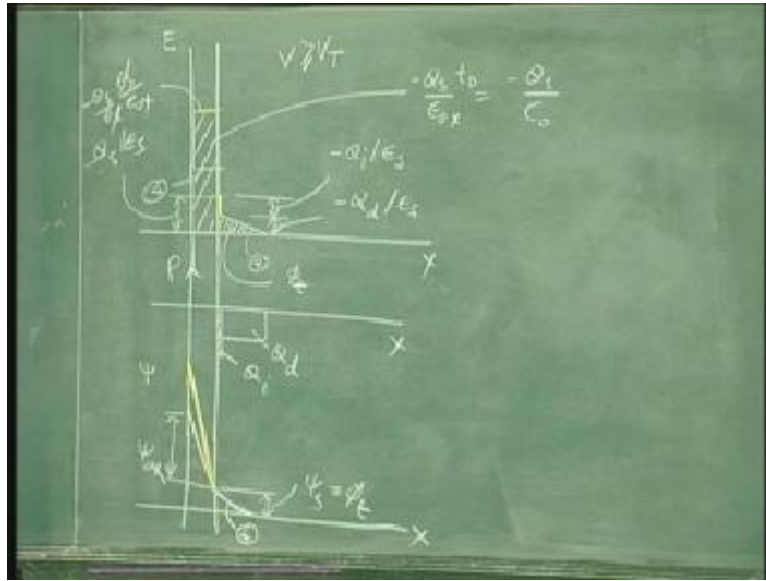
Well what we are saying is the following that ψ_s depends logarithmically on n_s . So even if n_s increases the increase in ψ_s will be very small because the ψ_s is logarithmic function of n_s . On the other hand, if you look at the inversion charge Q_i it increases almost linearly with n_s . The function is not exactly linear but approximately we can say. If this function ψ_s of n_s is logarithmic this is almost linear, Q_i is a linear function of this n_s . So when n_s increases Q_i increases directly with n_s whereas ψ_s increases logarithmically with n_s . That is why even though the inversion charge increases rapidly the surface potential increases very slowly therefore we are treating it as a constant. Now let us return to our discussion related to derivation of equations for Q_d and Q_i . Now the starting point for this is the same as that we used for deriving the special voltage expression.

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We can write V is equal to ψ_{ox} plus ψ_s , ψ_{ox} is given by minus the silicon charge by the oxide capacitance, this is from the field picture. Please note that Q_s by C_0 is with a minus sign because when the applied voltage is positive the charge in the silicon is negative, the charge in the silicon is of opposite polarity to the voltage applied to the gate and that is why you have minus. So, this is generally true, depletion as well as inversion. So, in the expression for Q_s you will have Q_d as well as Q_i . Look at this graph; we said that Q silicon the silicon charge is obtained by summing up Q_i and Q_d . So let us understand this with the help of a field versus distance diagram. So we draw the E versus X in the oxide and semiconductor.

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So at threshold suppose this is the field distribution, this is 4 in our nomenclature. Now, beyond threshold what happens is, you have a step in the electric field here because you have an inversion charge which is almost like a sheet. And then your oxide electric field will be three times this electric field. So in inversion this step is Q_i by ϵ_{ox} with a modulus or you can put a negative sign because the charge is negative, this is by Gauss's law. So the inversion charge contributes to a step in the electric field so we can draw the charge picture here underneath. This is depletion charge under depletion approximation and this is the inversion charge.

We are not showing the charge in the metal this is always positive whenever this charge is negative. So corresponding to this sheet charge you have this step. On the other hand, this distance is minus Q_d by E_s . So this total thing is Q_s by ϵ_{ox} with a negative sign, the silicon charge per ϵ_{ox} . As you go on increasing your voltage and since depletion layer does not expand beyond threshold, we are talking of V greater than or equal to threshold because the depletion width does not expand and this triangle will almost remain the same whereas this step will appear here and this will go on increasing as your V increases beyond V_T . But now what we are interested in is to know what the oxide and the silicon drop is. The oxide drop is given by this shaded area.

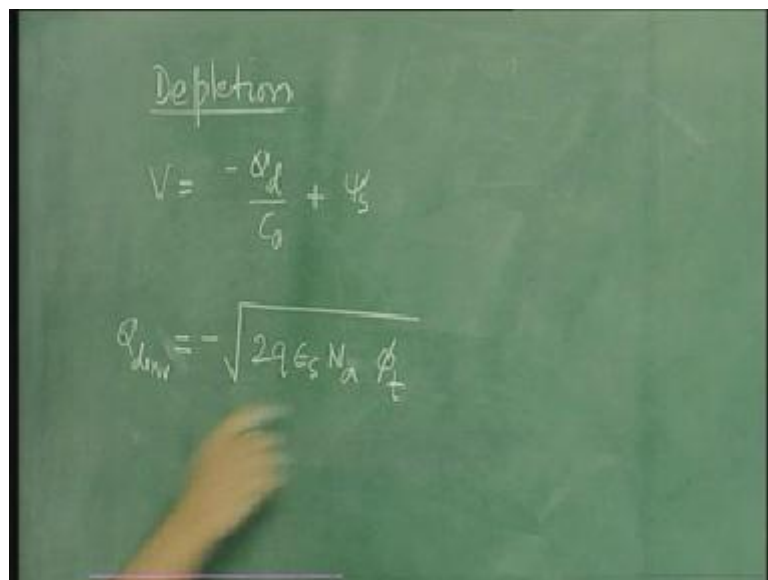
So what you find is this electric field is nothing but this electric field into ϵ_{ox} because you are shifting from silicon to silicon dioxide so this value is minus Q_s into minus Q_s by ϵ_{ox} into ϵ_{ox} by ϵ_{ox} which is nothing but Q_s by ϵ_{ox} and this area therefore is Q_s by ϵ_{ox} into t_0 because t_0 is this width. Now this is how we had derived the threshold voltage expression also. So that is the same thing. What we wanted to show here is that even when inversion charge is present the relation for the oxide potential drop is the same so this is nothing but minus Q_s by C_0 .

So, if we show this potential on potential variation with C diagram this is how it will be. So, in depletion suppose this is your potential at threshold so let us draw this to scale. For the particular calculation we did we found that this is about 0.7 potential drop whereas the remaining one is about 3.2 which means this is almost 4.5 times this so this is approximately

to scale. This is your ψ_s and this is ψ_{ox} , this is 4 at threshold, this ψ will be ϕ_t it is this area ϕ_t . That is the link between this diagram and this diagram and this diagram. So, from charge you get the electric field by Gauss's law and by integrating the electric field or taking the areas in the electric field you get the potential versus X. This ψ_{ox} is this area and that is minus Q_s by C_0 . Now, in inversion what will happen is, this part will almost remain the same but only your oxide potential drop is going to change.

Now coming back to the equation here therefore your conditions are; ψ_{ox} is equal to minus Q_s by C_0 where Q_s is Q_d plus Q_i . In depletion Q_s is approximately equal to Q_d whereas in inversion Q_s is equal to the value of Q_d at inversion plus Q_i . Now, starting from here from these two equations and substituting these into this and then this back into this we can get the charge versus voltage regulation. First let us take the depletion region Q - V relationship. So we can write V is equal to minus Q_d by C_0 plus ψ_s .

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Depletion

$$V = -\frac{Q_d}{C_0} + \psi_s$$

$$Q_{dinv} = -\sqrt{2q\epsilon_s N_a \phi_t}$$

Now we want Q_d as a function of V so to do that we must express ψ_s also as a function of Q_d . Now if you recall when we wrote down the threshold voltage expression we wrote down the depletion charge at threshold as follows: Q_d is equal to minus square root of $2q\epsilon_s N_a$ into ϕ_t this was at inversion. Please look at the derivation. So basically this derivation is related to this. So we must relate this area Q_d and this electric field here and then this electric field is related to the area under this which is the potential ψ_s . Following the same approach if you try to derive the Q_d as a function of ψ_s all that you need to do is replace ϕ_t by ψ_s .

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Depletion $0 \leq V \leq V_T$
 $0 \leq \psi_s \leq \psi_t$

$$V = -\frac{Q_d}{C_0} + \psi_s$$

$$Q_d = -\sqrt{2q\epsilon_s N_a \psi_s}$$

$$\psi_s = \frac{Q_d^2}{2q\epsilon_s N_a}$$

$$V = -\left(\frac{Q_d}{C_0} - \frac{Q_d^2}{2q\epsilon_s N_a}\right)$$

Here this is generally valid until threshold which is in the depletion region. So once you know this you know that ψ_s is given by Q_d square by $2q\epsilon_s N_a$ by squaring both sides. We can substitute this here and you get an equation between V and Q_d so this is a quadratic equation. So your relation is V is equal to minus Q_d by C_0 plus Q_d square by $2q\epsilon_s N_a$ this is the equation for depletion region. Now how do you know that this equation is valid? It depends on what is your value of ψ_s or V . So depletion region means V less than or equal to V_T but greater than or equal to 0 or ψ_s is less than or equal to ψ_t greater than or equal to 0. Let us write this here and this is the depletion.

Now, similarly let us take the inversion condition. What is the charge voltage regulation under inversion? Now incidentally this quadratic equation represents this particular curve. Please note how do we get this shape from here? The first term is a linear term and then the second term is a quadratic term basically subtracting from the first term if you take the brackets. So in brackets you can write you can write this as follows. Now this whole quantity will be on the negative axis so a linear term increasing. But then you have a quadratic term subtracting from the linear term as seen here. So you have a linear increase but then since the quadratic term is present and by subtracting the magnitude goes on falling and that is how you get this kind of a shape. Now let us return to the inversion charge.

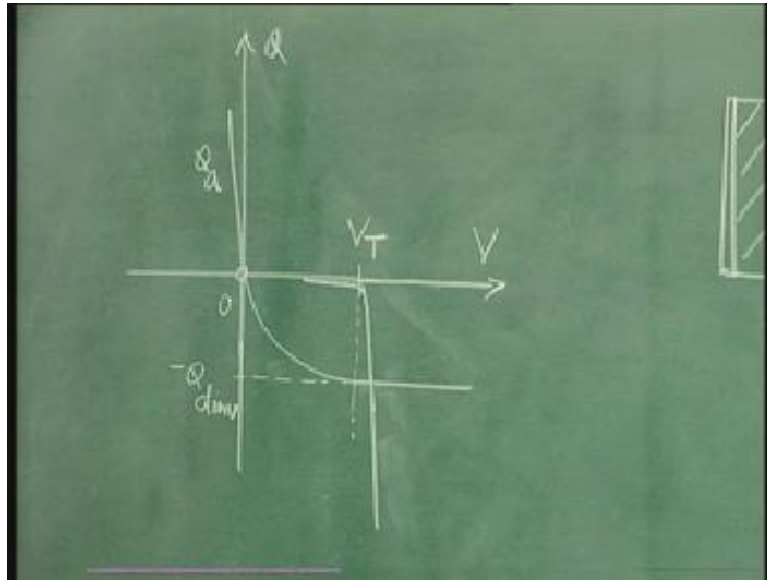
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The image shows a chalkboard with handwritten equations for the inversion region of a MOSFET. At the top, it says "Inversion" and " $V \geq V_T$ $\psi_s \sim \phi_t$ ". The main derivation starts with the equation $V = -\frac{(Q_{dinv} + Q_i)}{C_o} + \phi_t$. This is then rearranged to $V = -\frac{Q_i}{C_o} + \left(\frac{-Q_{dinv}}{C_o} + \phi_t \right)$. A bracket under the term in parentheses is labeled V_T . This leads to $V - V_T = -\frac{Q_i}{C_o}$. Finally, the equation $Q_i = -C_o(V - V_T)$ is boxed. To the right, there are two small graphs: the top one shows ϕ_t vs V with a horizontal line at ϕ_t and a vertical line at V_T ; the bottom one shows Q_i vs V with a line starting at V_T and increasing linearly with a negative slope.

In inversion we can write V is equal to Q_d inversion plus Q_i with a negative sign by C_0 plus ϕ_t because inversion is characterized by V greater than or equal to V_T or ψ_s is equal to ϕ_t . So we must replace ψ_s by ϕ_t which we can write as minus Q_i by C_0 plus minus Q_d Inversion by C_0 plus ϕ_t . Now this sum is nothing but the threshold voltage V_T . Therefore you write this as V minus V_T is equal to minus Q_i by C_0 . Or transforming this equation you get Q_i is equal to minus C_0 into V minus V_T . So Q_i is linearly increasing with voltage. But please note that this formula is only valid for V greater than V_T . So one must not say if V is less than V_T then Q_i will be positive. There is no positive Q_i for V less than V_T . This formula itself is valid only for V greater than V_T .

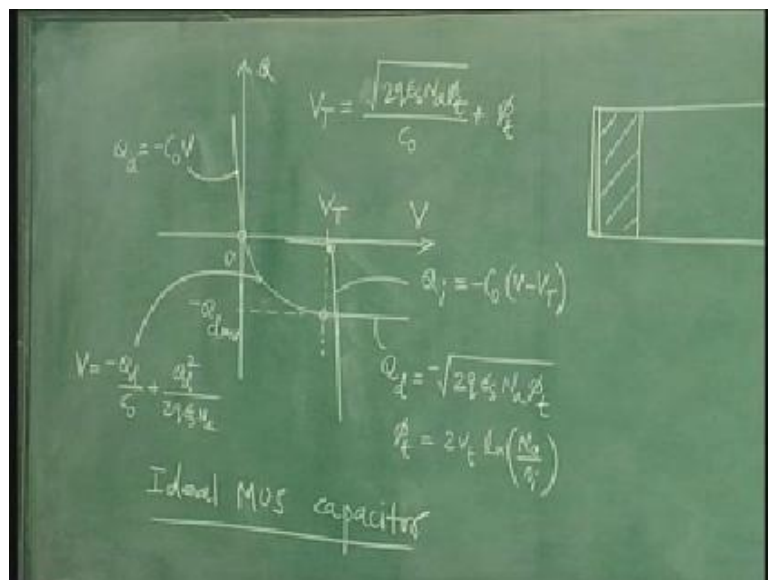
Now you can see that this particular shape is a straight line starting from V_T which is the shape for Q_i . So, what we derive is that the inversion charge increases linearly with the difference between the applied voltage and threshold voltage. Now with this we have completed the Q minus V characteristics of an ideal MOS capacitor. **So let us summarize what we have obtained so far.**

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This is the Q versus V curve. For the various segments the equations are as follows. For this accumulation segment that is this segment here you can write Q_a is equal to minus C_0 into V that is this segment. Then for the depletion segment that is between 0 and V_T you can write V is equal to minus Q_d by C_0 plus Q_d square by $2q \epsilon_{\text{silicon}} N_a$.

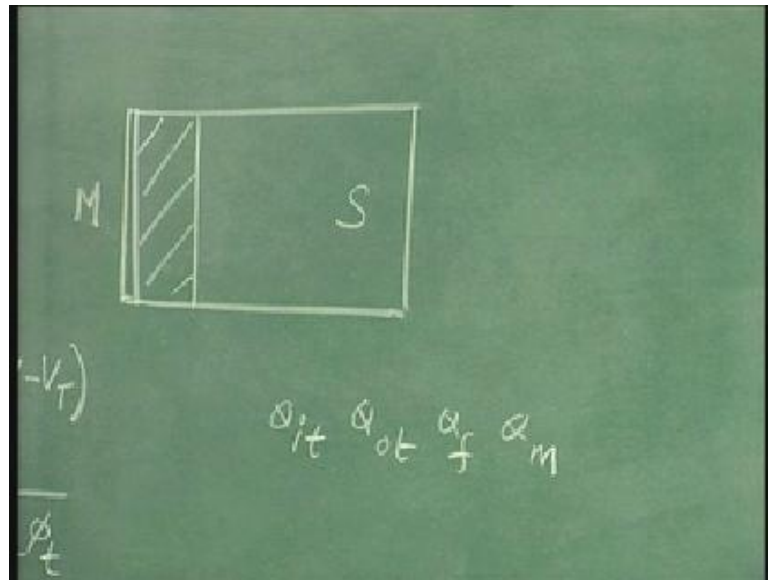
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Now for this particular depletion charge segment beyond threshold this value is minus Q_d inverse. So Q_d is equal to Q_d inverse which is nothing but minus square root of $2q \epsilon_{\text{silicon}} N_a$ into ϕ_t where ϕ_t is equal to $2V_T \ln N_a$ by n_i . Then you have the inversion charge segment which is this and for this segment your equation is Q_i is equal to minus C_0 into V minus V_T . The threshold voltage expression V_T is given by minus Q_d inverse by C_0 which is the oxide potential drop that is square root of $2q \epsilon_{\text{silicon}} N_a$ into ϕ_t by C_0 plus silicon drop that is ϕ_t . So these are the results for an ideal MOS capacitor. Now we must see what happens when the capacitor is not ideal or when it is real.

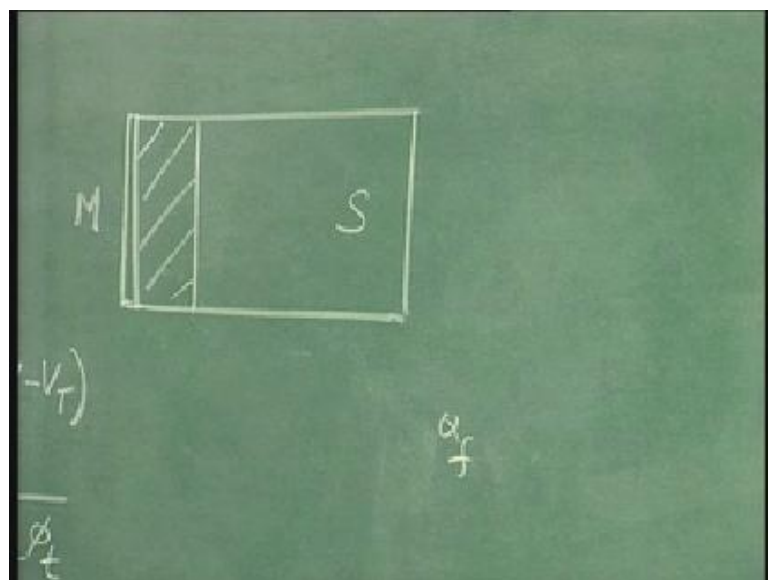
As we explained, in a real capacitor the extra things we must take into account are firstly this metal or poly silicon gate and semiconductor between them there is a contact potential which we have not taken into account and also in addition you have a number of charges in oxide as well as at the interface.

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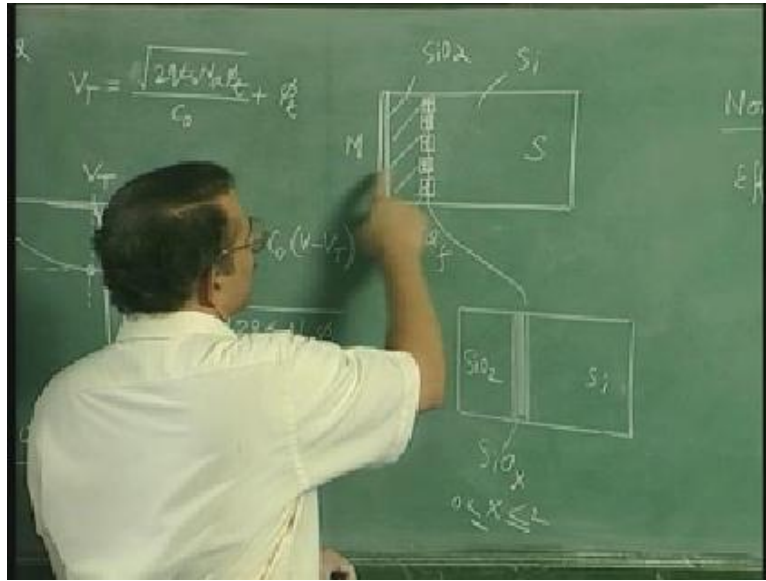


So the charges we listed were Q_{it} that is interface trap charge, Q_{ot} that is oxide trap charge, Q_f that is the fixed charge at the interface and Q_m that is the mobile charge in oxide. Let us concentrate on the charge Q_f alone.

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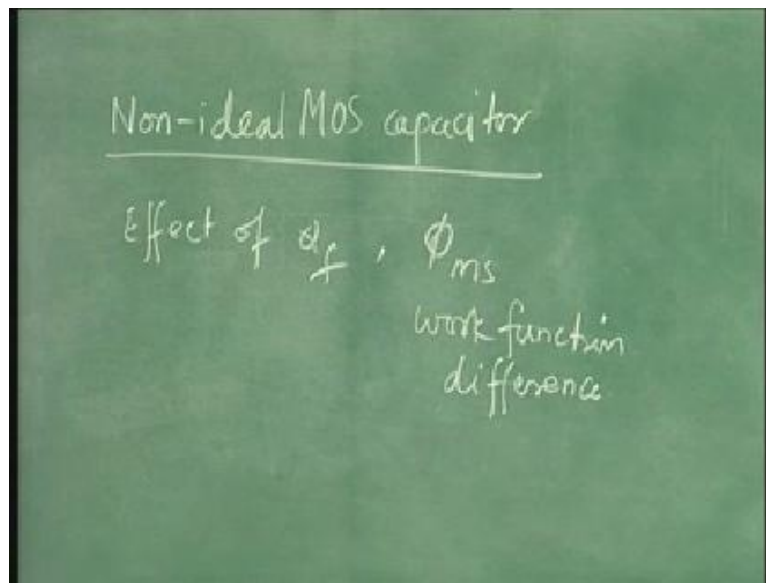
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Now it turns out that at silicon dioxide interface you have a positive charge which is said to be fixed because the value of this charge does not change with voltage and it is always present whenever you create silicon dioxide interface. So right here at the interface you have this charge. Usually this charge is shown in a box because this is a fixed charge so it cannot move nor can it vary with voltage. Now very briefly the origin of this Q_f is as follows: The chemical composition of the oxide layer or the silicon dioxide layer is SiO_2 so this SiO_2 whereas this is Si . Now you cannot have an abrupt transition from Si to SiO_2 in practice.

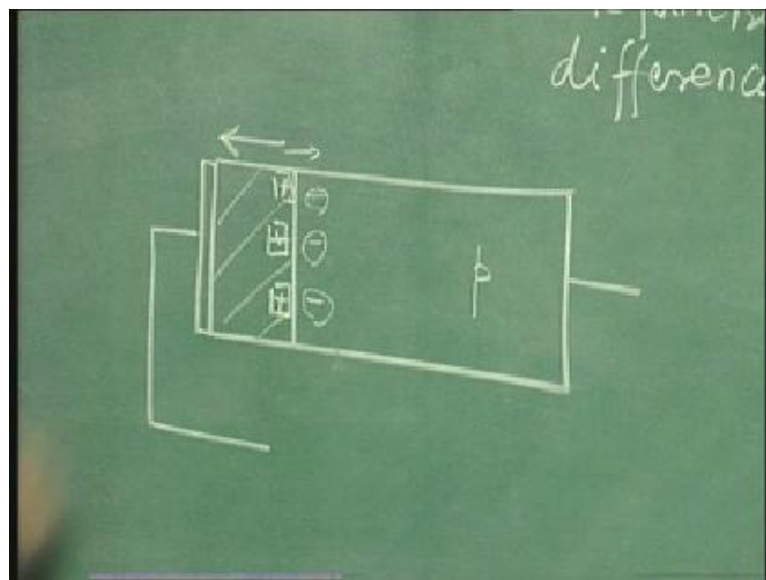
So what is going to happen is that if you expand this interface you have silicon and on this side you have silicon dioxide so there will be a region in which the composition will gradually change from Si to SiO_2 so here it is SiO_2 and this region it is SiO_x where x varies from 0 to 2. So here x is 0 and here it is 2 so there is this transition layer. Now because you do not have two oxide oxygen atoms for one silicon so all the silicon atoms are not satisfied by bonding and therefore there is a positive charge that is created. And this positive charge is the charge that is called Q_f .

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So in our non-ideal MOS capacitor which is the next topic we will try to take into account the effect of Q_f and what is called the contact potential or as we show that contact potential is nothing but work function difference denoted ϕ_{ms} is called work function difference. Now the question is how we take both of these into account. Let us start with the effect of Q_f .

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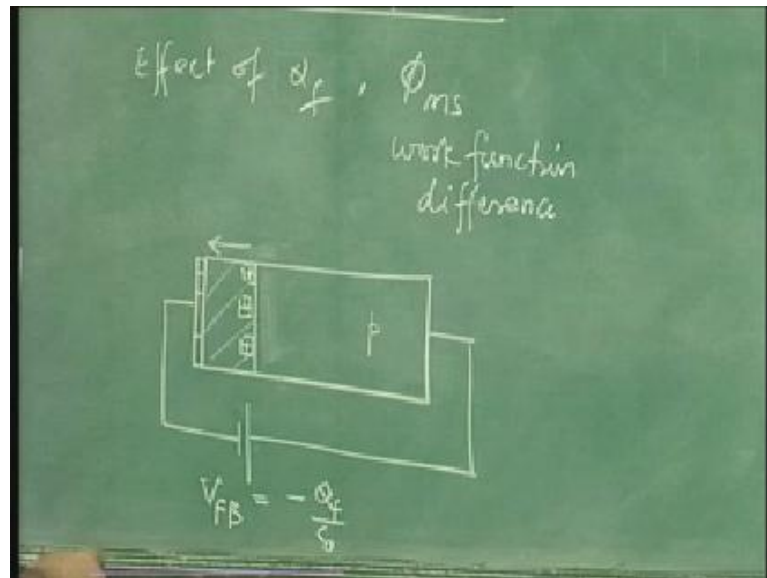


What effect will Q_f have?

Now you can see that this positive charge Q_f will tend to find negative charge here in the nearest silicon substrate. So what does this mean is that if you have a p-type substrate here then even when you do not apply any voltage because of this fixed charge you will already have a depletion layer. So you have charge in silicon even when there is no applied voltage. Recall that in ideal MOS capacitor for no applied voltage there was no charge in silicon whereas here you have a negative charge. Now if the Q_f is very large you can even have inversion charge here in addition to depletion charge.

So, if you want to create a condition of zero charge in silicon what you will have to do is you will have to apply a voltage to the gate so that these charges instead of terminating on this side with an electric field like this they terminate on the gate with an electric field directed in the opposite way. So you need an electric field like this so that these positive charges will not look for negative charges in silicon.

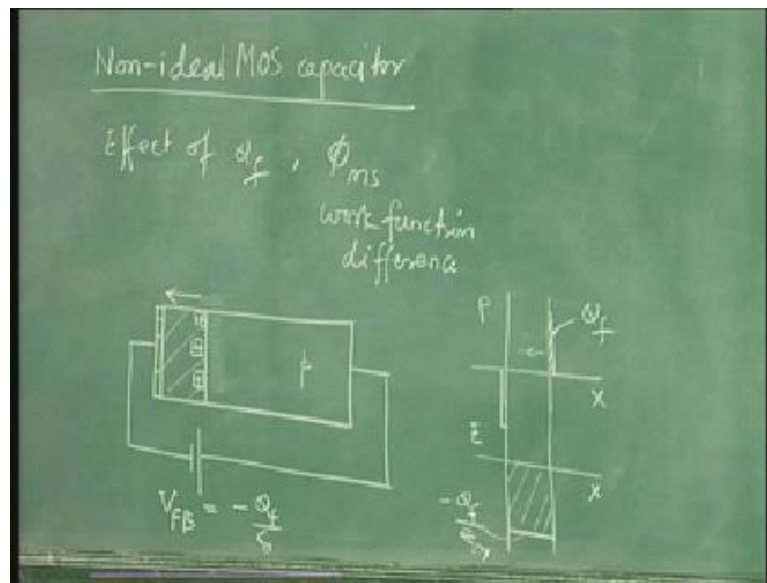
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In other words, you have to put a negative charge equal in magnitude to the positive charge in the gate which means you must apply a negative voltage to the gate to create zero charge in silicon. Now zero charge in silicon corresponds to Flat-band conditions in semiconductor if the semiconductor is uniformly doped because then the conduction and valance band are constant with distance when there is no charge. Therefore to create Flat-band conditions in silicon you will have to apply a voltage in a non-ideal MOS capacitor. And if you want to take into account only the effect of Q_f then you will have apply a Flat-band voltage which is negative. And what is the value of this Flat-band voltage? We can even determine that.

Since the charge is Q_f the voltage to be applied from the field and charged picture is V_{FB} is equal to minus Q_f by C_0 . This is the simple parallel plate capacitor relation. That is the charge is equal to voltage into capacitance.

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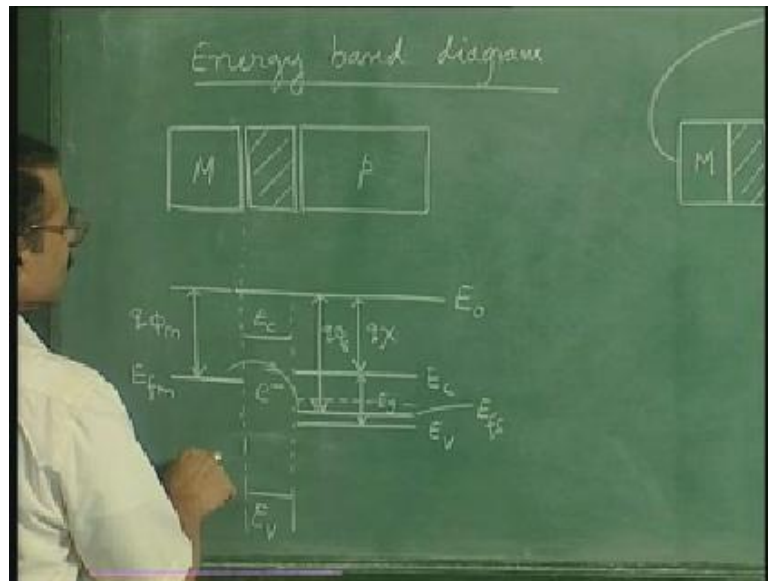
Therefore one can draw the charge and field picture which would be like this. So you have the fixed semiconductor and equal negative charge on the gate so this is the charged condition and both are sheet charges. And now you have an electric field directed from this positive charge to negative charge so this is your E versus X . And the value of the electric field is nothing but Q_f by ϵ_{ox} . You recall that when we wrote the electric field in oxide because of a certain silicon charge Q_s we wrote the oxide field as minus Q_s by ϵ_{ox} so similarly here it is minus Q_f by ϵ_{ox} . Q_f is this charge area under this so now the area under this is the applied voltage. Following this approach you get Flat-band voltage equal to minus Q_f by C_0 . So the effect of fixed charge is to shift the Flat-band voltage of an ideal MOS capacitor which is 0 to a negative value. So the Flat-band voltage is shifted from 0 to a negative value in a non-ideal MOS capacitor because of Q_f .

Now how do you take into account the effect of ϕ_{ms} ?

To take into account the effect of ϕ_{ms} we will have to go to the energy band diagram. Now this is an important point we arrive at here that whenever you want to discuss a junction between dissimilar materials then you will have to use the energy band diagram, you cannot avoid energy band diagram. If you recall when we discussed the PN junction we said that when you have a PN junction made in silicon that is in the same material one can do a great deal of analysis of this junction and derive the current voltage characteristics without the aid of energy band diagram.

Although energy band diagram approach gives you some additional insights but without energy band diagram one can go quite far in understanding a PN junction which is a homo junction. So we can generally say to understand a homo junction we can avoid the use of energy band diagram to a great extent. But while understanding a hetero junction or a junction between dissimilar materials which is what a MOS junction is because material here is different from the material here and of course material here is also different so in such cases we need to use energy band diagram to derive the effects of the contact potential or the work function difference between one material and another material. So the next topic that we need to discuss in the context of non-ideal MOS capacitors is the energy band diagram.

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Now let us look at the energy band diagram when all the components of the MOS capacitor are isolated. That means you have the metal then you have the oxide and you have the semiconductor and suppose these are all isolated now without any loss of generality we will assume that the metal is also sufficiently thick, this is just to enable us to draw the energy band diagram.

Now how do we draw the energy band diagram?

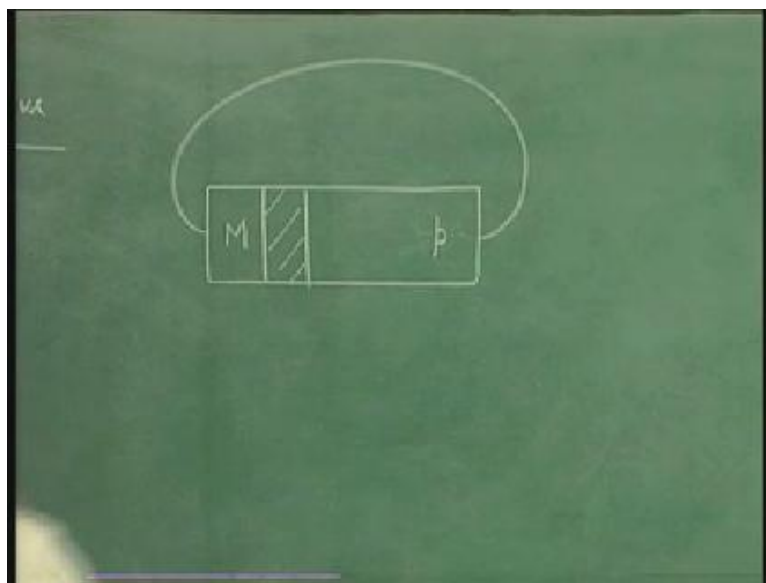
Showing the bands in all the three we must choose a reference. We know that the reference is normally the vacuum level. So we first draw E_0 . The various steps in the drawing of energy band diagram were given in the context of PN junction and we are following the same steps. Now, in the metal you cannot have conduction or valence bands but you only have the Fermi-level. So this is E_{fm} and this difference is normally referred to as the work function, the difference between the vacuum level and the Fermi-level. So this is q times ϕ_m where ϕ is the work function in volts, E is energy. Energy band in the oxide, the oxide is an insulator it has a very wide band gap so energy band diagram is something like this, this is the conduction and valence band.

Please remember that these three are isolated right now when we draw the band diagram so there is no connection between them. So, we are drawing the structure individually in each of these three. So this is E_c and this is E_v . Now we come to the semiconductor. In the semiconductor you will first locate the E_c and then E_v . The band gap of semiconductor is obviously much less than that of the oxide. This E_c is located at a distance given by q times the electron affinity. Then this E_v located below E_c and this is energy gap.

Since we are considering p-type silicon your Fermi-level will be below the intrinsic level which is in the middle here. So this is intrinsic level and your Fermi-level is somewhere here. This is E_f in the semiconductor where s stands for semiconductor. Here we have shown a metal whose work function is more than the electron affinity in the semiconductor. It is not necessary that this should always be the case but you can have the Fermi-level above this level here or even below the valence band level, it depends on the metal.

In analogy to the work function in the metal you can define a work function in semiconductor also so that would be this difference $q(\phi_s)$. Although the work function in semiconductor does not have that much real meaning as it has in a metal because you can remove an electron from the Fermi-level out of a metal. So when you remove an electron out of a metal it is most likely to be at the Fermi-level whereas when you remove an electron in the semiconductor it is unlikely to be at the Fermi-level because Fermi-level is in the forbidden gap and you do not have any allowed states in the forbidden gap in the electrons. But still it may help us in writing the equations that is why we are introducing this work function in semiconductor. So Fermi in the metal is above the Fermi-level in the semiconductor as we have drawn here. Now from this starting point we proceed to the situation when you put all these three components together and join them by a wire which means now we draw the band diagram which is like this, so you are joining them together.

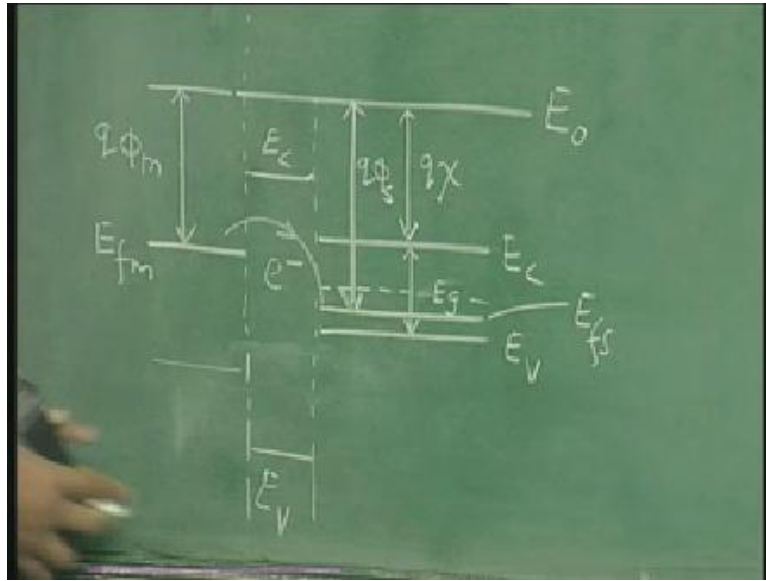
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Please note that if we join them together like this the band diagram will be no different from this diagram. That is because since there is an insulator here it prevents any interaction between the metal and this semiconductor so no exchange of charges can happen. So even when these three components are stuck to each other they are still as isolated as this case when they are separate. So when we talk of the energy band diagram of a MOS capacitor under equilibrium it is necessary to note that the metal here is joined to the semiconductor here by a wire. Only then the MOS is said to be in equilibrium that is all these three form a system because in a system the various should be able to interact with each other otherwise it is not a system at all. So in this case what is the energy band diagram?

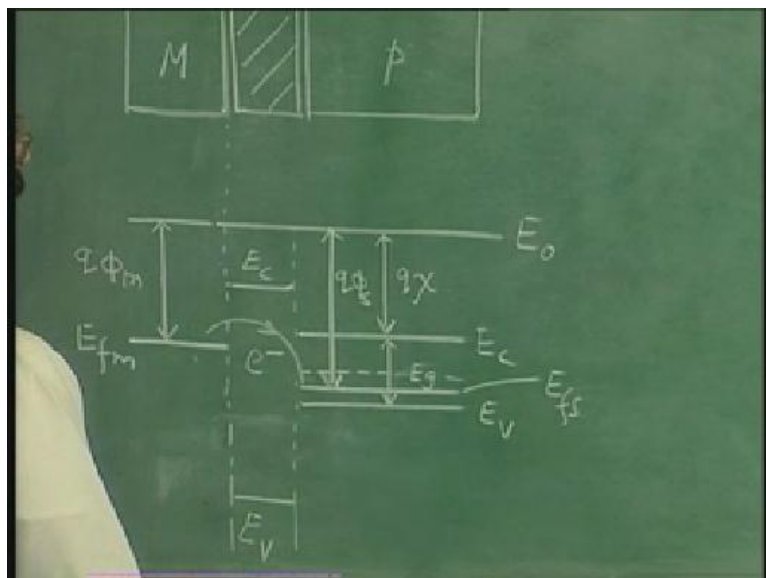
We can start from here and we will note that since Fermi-level is higher here than in this semiconductor the electrons will tend to be transferred in this direction so electrons are transferred from metal to semiconductor. Now, please note that electrons are being transferred from metal to semiconductor because Fermi-level in metal is higher than that in semiconductor. One must not think that because the electrons are in higher concentration in metal than in semiconductor therefore they are being transferred. So, because electrons concentration is higher in metal than in semiconductor you will always have transfer of electrons from metal to semiconductor which is not correct.

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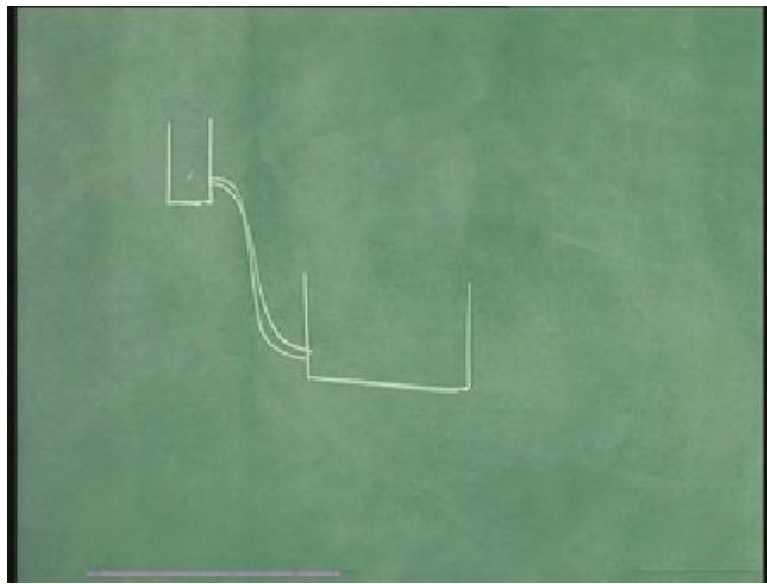


For example, in this case if the Fermi-level was below this Fermi-level somewhere here like this then even if this is a p-type semiconductor which has a very small number of electrons when you join the metal and semiconductor by a wire the electrons would get transferred from semiconductor to metal because the Fermi-level here is higher than here. So it is a Fermi-level difference that decides because Fermi-level represents the average energy of electrons and electrons always move from regions of higher energy to regions of lower energy just as water goes from a point which is at a greater height to a point which is at a lower height.

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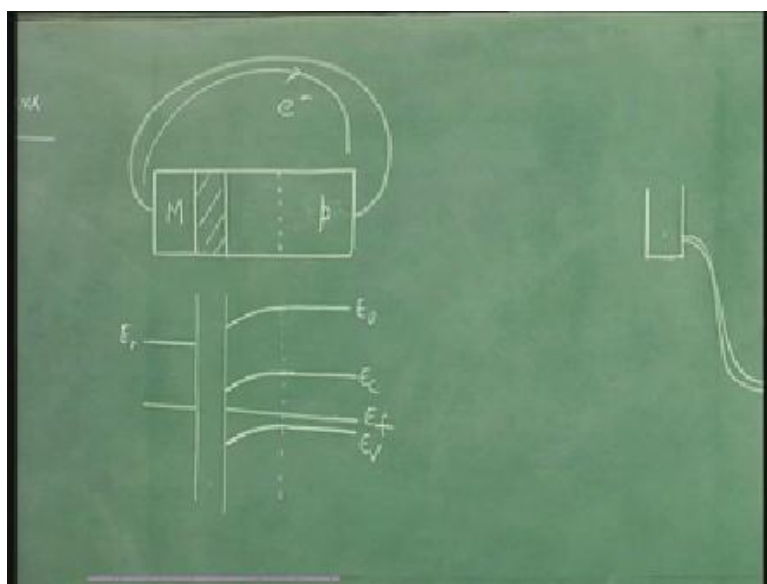


So even if you have a container like this which is small and you have big container here at a lower height than this and when you join these two by a tube the water will flow from this to this even though the container is small because it is at a greater height than here. So it is the height that decides the transfer of water. Similarly here it is a Fermi-level that decides the direction of transfer of electrons.

How are the electrons transferred?

Well, even though the electrons have been shown to be transferred like this it does not mean they are going through the oxide because the oxide would not allow any electrons. So basically this transfer is taking place through the wire here. So this is how the electrons are transferred.

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Now after the transfer takes place and equilibrium is established both these Fermi-levels should be aligned because in equilibrium the Fermi-level should be a constant. Therefore the band diagram would look something like this. We should draw constant Fermi-level. Now please note that we are not drawing a Fermi-level in oxide because oxide is an insulator and really speaking there is no Fermi-level. Having drawn the Fermi-level now you identify a space charge region. You are following the same sequence of steps which we followed for PN junction.

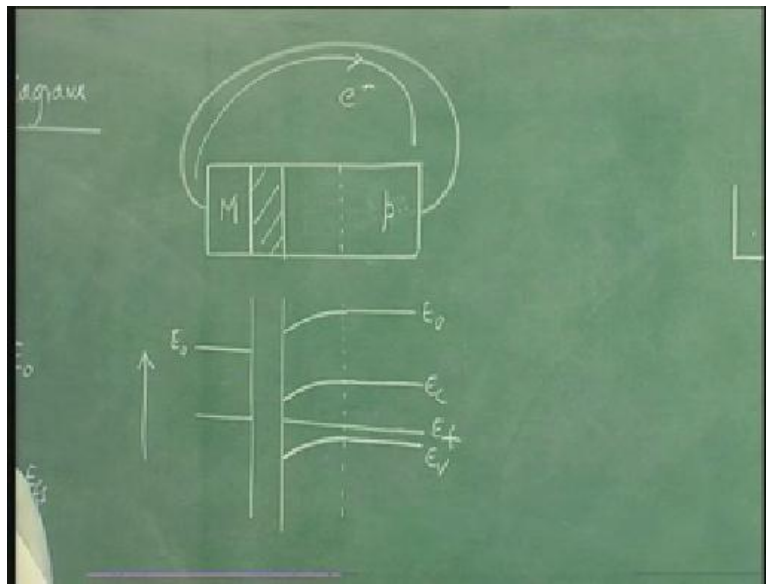
Now we ignore the width of the space charge region in the metal because that is really very thin. Now here if electrons are transferred they would recombine with holes on the p-side and in effect what we are having is therefore depletion of holes. So you are creating a depletion layer. Therefore the extent of this region would be much more than a sheet charge because you are having a depletion layer. So hole concentration is going to decrease as compared to bulk. Now you draw the energy band diagram in the bulk. Bulk means away from the space charge region so this is what the energy band diagram is in the semiconductor away from the bulk.

Now you must complete the picture, the hole concentration is reducing as you come to the surface so it is something like this. And you can complete the picture for vacuum level. This is E_0 , this is E_c , this is E_v and this is E_f something like this and this is your E_0 . Now what about the vacuum level in the metal? Vacuum level in the metal will be at the same distance from the Fermi-level as it was here. One way of understanding how this bending occurs in the energy band diagram is to build up this diagram as follows. So here you find that the electrons will move into the semiconductor and therefore the Fermi-level here will come down. So we assume that the Fermi-level is coming down here and it is aligning with this metal. Actually this is coming down and that is going up but for simplicity we will take this as the reference and say that this is coming down. So along with this the E_0 also will come down, so you have E_0 somewhere here. That is how the diagram looks.

Note that we have not drawn the diagram in the oxide, we can draw it in the oxide also but that adds to the complexity. In fact whatever effects we are going to discuss those effects do not depend on the energy band diagram in the oxide and they depend only the diagram in the metal and semiconductor. So this is the picture under equilibrium. So you see what has happened is because of the contact potential even when the applied voltage is 0 you have a charge in the semiconductor and in this case it is a negative charge. So this is the effect of the contact potential. Even when the applied voltage is 0 you have a charge in the semiconductor because of charge transfer between metal and semiconductor originating from the difference in the Fermi-levels in the two regions. That is the effect of non-ideality which means if you want to create a zero charge condition in the semiconductor you will have to apply a voltage to the gate.

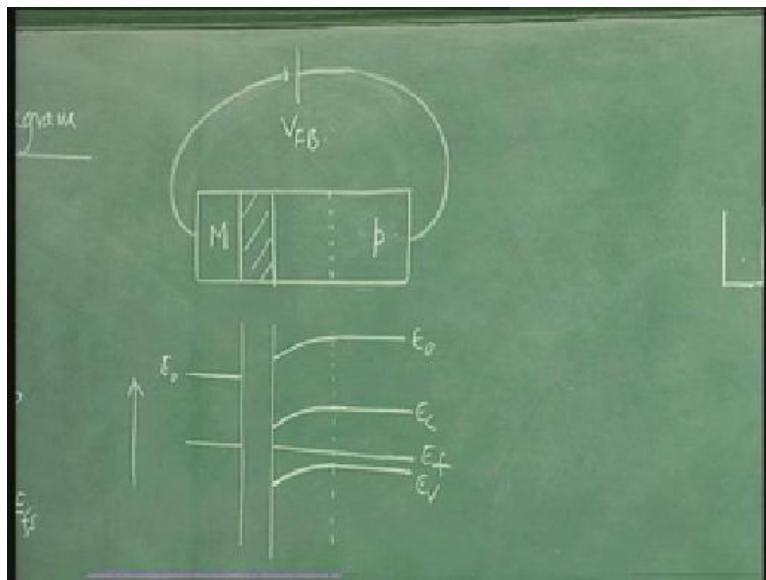
In other words, the Flat-band voltage will not be 0 that is the effect of the work function difference. Now how much voltage should we apply so that the charge conditions are 0? When you have zero charge here the energy band diagram would be the same as this and that is the Flat-band condition. So, to achieve this Flat-band condition you will have to remove the negative charges which are there in p-type. So from here we start and we have to remove the charges which are there in the p-type. So to remove the negative charges in p-type semiconductor you must apply a negative voltage to the metal which means you must lift this Fermi-level up because increase in energy is here these are electronic energies.

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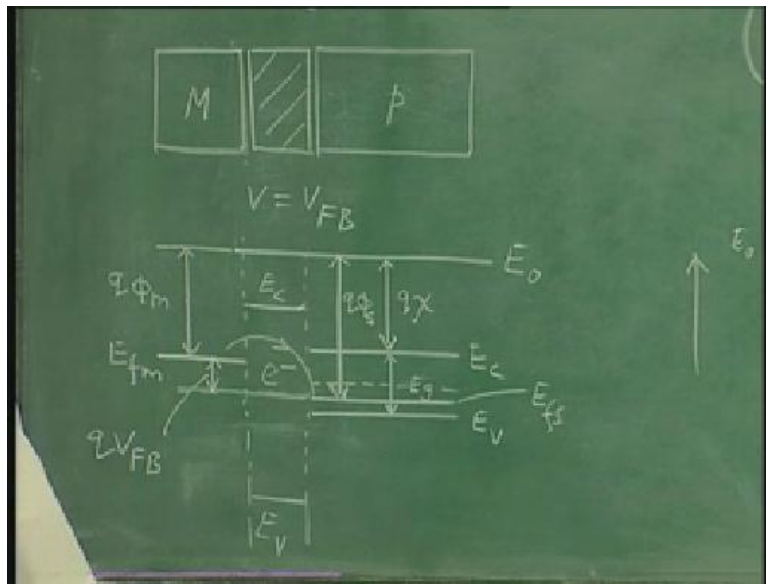
So when a Fermi-level moves up it means that you are applying a negative voltage. So in order to get Flat-band condition what you will have to do is, you have to introduce a power supply here with a negative polarity because in this particular case you have negative charge in the semiconductor.

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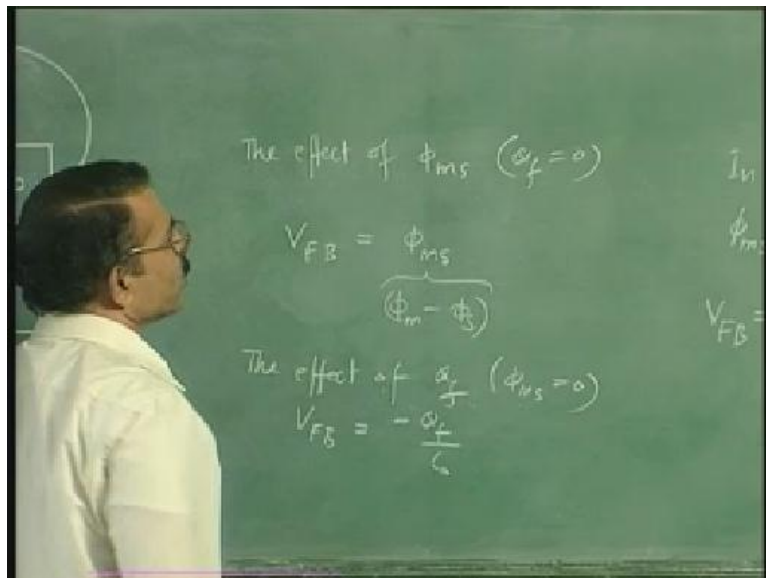
Once you do that provided the power supplies of copper magnitude all these negative charges will be repelled. We will shortly see what the magnitude is. This is interesting that you have zero charge condition in the metal for a given applied voltage so this is the Flat-band voltage. Now V is equal to V_{FB} is the condition.

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So the band diagram for V is equal to V_{FB} is the same as the band diagram when the three regions are isolated or not joined by a wire. Then this difference between the Fermi-levels indicates the amount of applied voltage because under equilibrium the Fermi-levels are aligned and this is the Flat-band voltage or voltage you have to apply to the gate. Now evidently this voltage is equal to the difference in the work function of this semiconductor and the metal. Therefore we can say that the effect of the work function difference ϕ_{ms} is that the Flat-band voltage equal to ϕ_{ms} should be applied to create Flat-band conditions.

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So we write V_{FB} the effect of ϕ_{ms} to create a Flat-band voltage equal to ϕ_{ms} and ϕ_{ms} is nothing but ϕ_m minus ϕ_s . Notice here that this voltage is the difference of these two but in magnitude it is negative. So this voltage is obtained as this minus this. Now we have already seen that the effect of Q_f was to create a Flat-band voltage equal to minus Q_f by C_0 assuming there was no ϕ_{ms} . So effect of Q_s when ϕ_{ms} is 0 is this. And effect of ϕ_{ms} when Q_f is 0 is

this and we considered no Q_f in this case. So whenever you want understand the effect of two parameters you must understand them one at a time and that is what we are doing here. So from these two we can easily get the effect of ϕ_{ms} and Q_f as follows:

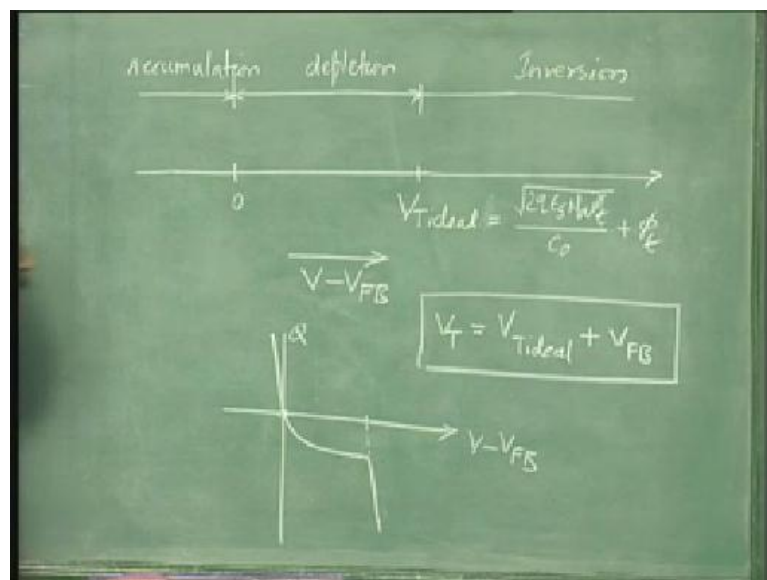
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In presence of ϕ_{ms} and Q_f

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_o}$$

In presence of ϕ_{ms} and Q_f you can simply write the Flat-band voltage is equal to the superposition of these two ϕ_{ms} minus Q_f by C_o . So we are simply summing up these two to get the effect when both ϕ_{ms} and Q_f are present. We can summarize all these discussions on the effect of Q_f and ϕ_{ms} in a non-ideal capacitor as follows:

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This is the picture we had for ideal capacitor. Here we find zero charge condition in the silicon at 0V and then threshold at a voltage given by this formula. Now the zero charge condition occurs at Flat-band voltage. In other words if you simply change this V to V minus V_{FB} then this whole picture is valid. Same thing you do here also, the charge was 0 for

voltage equal to 0 but now the charge is 0 when voltage is equal to V_{FB} . In other words, if you change this to V minus V_{FB} this whole diagram becomes and it becomes applicable to a real capacitor. Therefore we can say that the effect of non-idealities of Q_f and ϕ_{ms} is to simply change this zero charge condition to Flat-band voltage and the threshold voltage to the following formula. So threshold voltage is now given by V_T is equal to the threshold corresponding to ideal capacitor plus V_{FB} because V minus V_{FB} is this. Therefore V is V_{FB} plus this so V_T of a real capacitor is V_T of an ideal capacitor plus V_{FB} .