Solid State Devices
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Lecture - 25
PN Junction (Contd…)

This is the 25th lecture of this course and the 7th lecture on PN junction. In the previous lecture we have seen the reverse current voltage characteristics of a diode. In this lecture we will see the equivalent circuit of the diode under small signal conditions. So let us look at the slide which is related to this particular topic.

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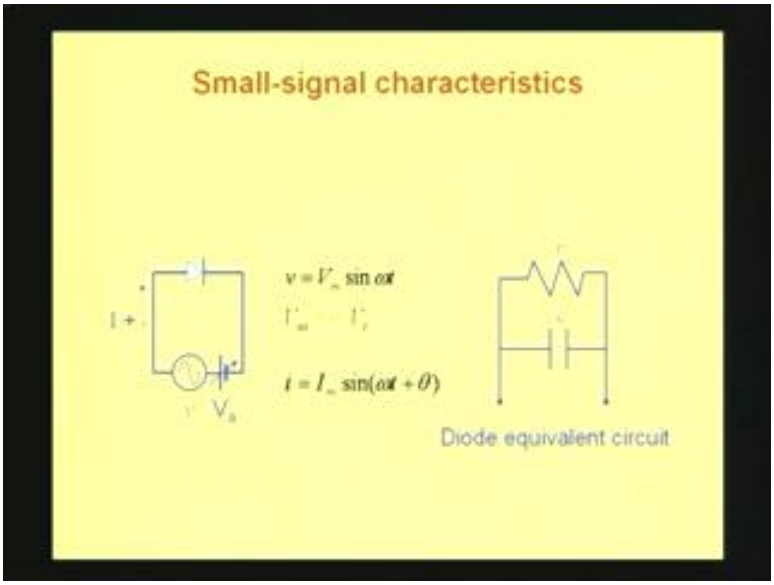

This is the biasing arrangement in which we measure the characteristics. You have a DC voltage applied across a diode. Although the circuit shows a forward bias the DC voltage V_a could as well be a reverse bias. Over and above this DC voltage is an AC voltage which is super imposed so this is the AC voltage. The magnitude of this voltage is small and that is why the term V_m is set to be very small compared to the thermal voltage V_t. Now why the V_n should be much less than V_t? At this point this is not clear but it will become clear when we take up the details.

The frequency of the signal is omega as shown by the equation v is equal to V suffix m into sin of omega t. If this is the applied voltage we will find that there will be a small signal current I as shown here in addition to the DC current capital I. And this small signal current I will have amplitude and also there may be a phase difference between the current and the voltage. We would like to find out what kind of an equivalent circuit will explain this phase difference and will also help us to calculate the amplitude of the current for a given voltage. So the equivalent circuit of the diode will look like this. So

we would like to explain how you obtain the diode equivalent circuit as a parallel combination of a resistance and capacitance.

Now, the approach for this is called the quasi-static approach. This means we will try to derive the formulae for AC conditions from the DC characteristics or static characteristics. This is an important point to remember that this approach gives you only approximate estimates of the capacitance and resistance of the equivalent circuit. To see the difference between the quasi-static approach or non-quasi-static approach in detail I would suggest that you look into the reference material that is given in this particular slide. This is an article published in IEEE transaction on education in November 1999.

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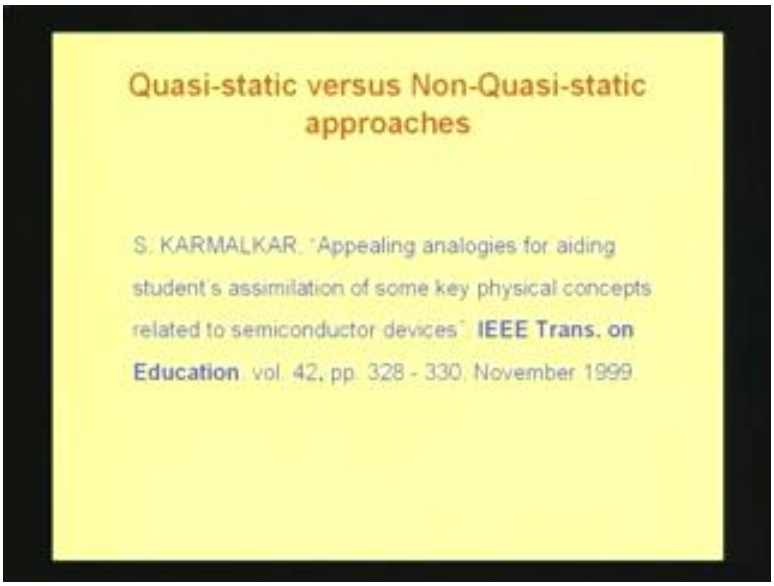

The page numbers are 328 to 330. The title of the article is "Appealing analogies for aiding student's assimilation of some key physical concepts related to semiconductor devices". Here with the help of an analogy the difference between the quasi-static and the rigorous approach of estimating the capacitance has been given. In this course we will only do the quasi-static approach. Now let us understand what is meant by the quasi-static approach in a little bit detail. This is a PN junction across which a bias has been applied, let us assume a forward bias. We will derive the family of a forward bias and we will show that the formulae will also enable us to get the parameters for the reverse bias.

Now what we do is we change the voltage V by a small amount as a result of which the current I will also change by small amount. Now when we make the change we wait until in the new voltage the conditions in the diode has stabilized and you are getting a new current. That is to say: for voltage V you get a current I then you change the voltage to v plus dV and then you give sufficient time so that the current stabilizes at I plus dI. So, just as I is a DC current corresponding to the voltage V, I plus dI is the steady state or DC current corresponding to the voltage V plus dV. Now, when the current changes from I to

I plus dI the charges inside the device also will change. For example, you find that a certain charge Q is stored in the device for a voltage V.

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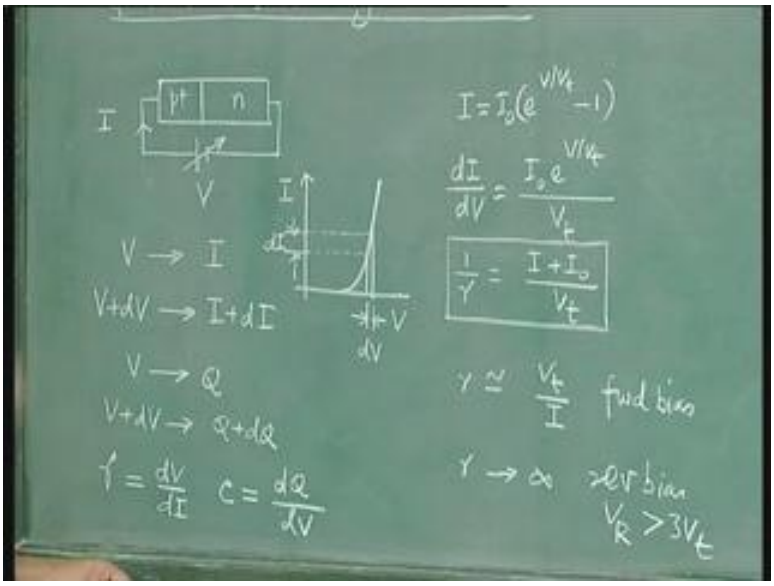

We will shortly see what is it that is responsible for storing a charge Q. As of now let us just assume that if a charge Q is stored for v and when you change the voltage to v plus dV this charge increases to Q plus dQ. Then from these conditions now one can obtain the resistance and capacitance as follows. So you can get a resistance r is equal to dV by dI. So dV is increment in voltage and corresponding increment in the DC or static current is dI so it is dV by dI. And you can define the capacitance C as this change dQ in the charge because of the change dV in the voltage. So this is the meaning of the quasi-static approach.

We are making a change in the voltage and we are estimating the changes in the current and charges because of the change in voltage but we give sufficient time for the effects of the change to stabilize. For example this resistance equal to dV by dI you can represent drastically as follows. This is your forward current voltage characteristics where I is on a linear scale and voltage is also on a linear scale. At some voltage V you make a change dV so this is the change dV and the corresponding change in current is dI. So you note this change in current dI and this dV by dI is the resistance. So basically it is a slope of this DC curve at any point.

Similarly, one can sketch this charge Q as a function of voltage V and then one can take the slope of that and one can obtain the capacitance dQ by dV. This is the quasi-static approach of determining the resistance and capacitance. Now we can quickly estimate the resistance using this formula because we know that the ideal diode equation is given by I is equal to I_0 exponential of V by V_t minus 1. So, differentiating this we get dI by dV is equal to I_0 exponential V by V_t by V_t which we can write as the numerator I_0 exponential V by V_t is I plus I_0 from this equation. So this is I plus I_0 by V_t. So dI by dV is nothing

but one by small signal resistance r. This is the formula for small signal resistance. Now for forward bias generally the current I is much greater than I_0 so we can write r is approximately equal to V_t by I for forward bias. On the other hand, what you see is that for reverse bias the current I will saturate to minus I_0 which is more than $3V_t$. And therefore you find from the formula that the small signal resistance of the diode for reverse bias more than $3V_t$ would be infinity because the numerator is 0.

So we can write r tends to infinity for reverse bias VR greater than $3V_t$. Now this is true for an ideal diode, please note that we are deriving this for an ideal diode. In a real diode you will find that this r will not be infinity because the reverse current increases with voltage because the reverse current in practical silicon diodes is because of generation within the depletion layer which goes on increasing because of the increase in depletion width with voltage. So in that case you will have a finite non-zero conductance or non-zero dI by dV on the reverse side therefore resistance will not be infinity but it will be of the order of hundreds of kilo ohms or higher.

What we are doing here is for ideal diode characteristics. Now how do we determine the capacitance of this particular diode under small signal conditions?
Before doing this let me explain why the capacitance and the resistance both should be regarded as in parallel. Please note that the voltage V that is responsible for the current I and the charge Q is the same. Since the resistance and the capacitance are due to a common voltage V that is the voltage across both the resistance and capacitance is the same and therefore it follows that the resistance and capacitance should be shown to be in parallel.

Now, determining the estimation of the capacitance we need to derive a relation for charge Q as a function of voltage V in the same way as we have a relation between the current I in response to V. Let us see how we determine the charge Q. Here we have shown the conditions in a PN junction under forward bias. This is the space charge region and these are the conditions in the neutral region. This is the first time we have shown both the electron and hole concentrations in the neutral regions on a linear scale and that is why you will find a cut shown here.

If we use the same scale we cannot show both majority and minority carriers. The reason we have shown both electrons and holes in a given-region on linear scale is that we must recognize that the excess hole concentration which is shown by this shaded area in the n-region is exactly compensated by the excess electron concentration which is the area under this portion. So, when the p-region injects holes into n-region these are the injected holes the negative terminal injects electrons to compensate for the holes so that charge neutrality is maintained. So this equality in the holes and electrons is clearly seen when you plot it on a linear scale and similar conditions exist here also. These are the injected electrons from the p-side and to compensate for this you have holes injected from the positive contact. We will be shading the positive charges in the device, these are the extra positive chargers, excess holes on the p-side. The dotted lines here show the equilibrium condition.

Now, come back to the space charge region. Here corresponding to the equilibrium condition the space charge region would look like this. The width of the space charge region would have been longer. So the distance between this dotted line and this dotted line shows the space charge region width under equilibrium and the solid line shows the conditions for the applied voltage V which is the forward voltage. Here this is for V and this is for V is equal to 0.

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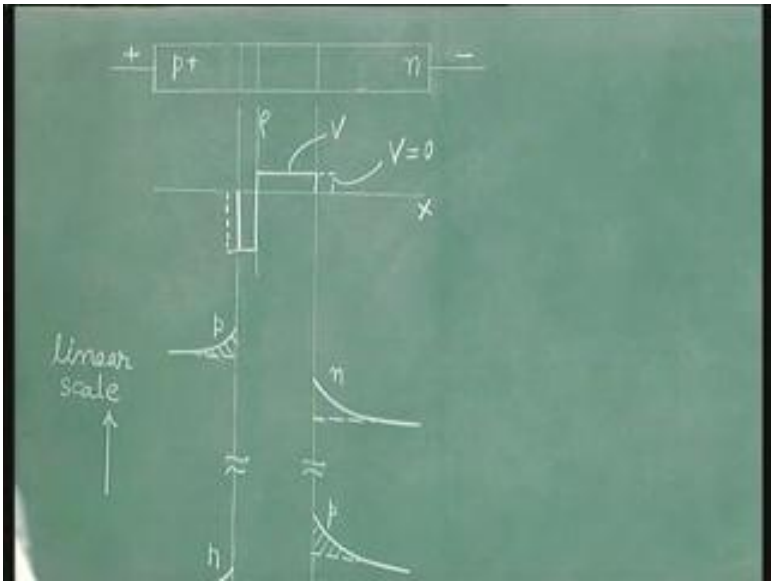

We find that the depletion-region has shrunk for the forward bias V. Or in other words, the width of the quasi-neutral region has increased on either side. This is the shrunk wing of the depletion-region which represents also the extension of the quasi-neutral n-region. So equilibrium quasi-neutral region was between this dotted line and this end whereas for applied bias it is between the solid line and this end. So we can say that the swing in of the depletion layer has cost expansion of the quasi-neutral regions and in other words therefore what has happened is that extra electrons have been introduced in this n-region and extra holes have been introduced in this p-region. So as to compensate for the ionized impurities here and as well as there to create charge neutrality.

When you have extra electrons in the quasi-neutral regions obviously some holes will be there which are minority carriers and similarly some electrons will also be there. But we neglect the effect of the electrons on the p-side and holes and the n-side because they are minority carriers as far as the depletion layers are concerned. So we can say the expansion of the quasi-neutral region has been because of injection of electrons from the negative terminal. And exactly equal number of holes has been injected from the positive terminal so as to extend the quasi-neutral region on the p-side. So this area represents the extra holes which have come in at the forward bias voltage V as compared to the equilibrium condition. And obviously this area is equal to this area and this represents the extra electrons. These are the extra electrons.

What one can say is that, as compared to the equilibrium condition because of forward bias there has been a change in the concentration of holes and concentration of electrons. So we can write it down as follows. In the PN junction you have charges which are because of impurities which are bound charges and you have free charges which are electrons or holes. And now the electrons and holes change when a voltage is applied so the free carrier chargers change due to change in this space charge width and due to change in the excess charge in the neutral regions or quasi-neutral region.

Therefore the electrons and holes change in the number. But these impurities the bound charges do not change so we need not take the effect of this into account because we are defining the capacitance as dQ by dV. So, only the change in the charge is of interest to us because of dV and not the absolute magnitude of charges. Since a bound charger or impurities do not change with voltage we do not consider the effect of the impurities in estimation of the capacitance.

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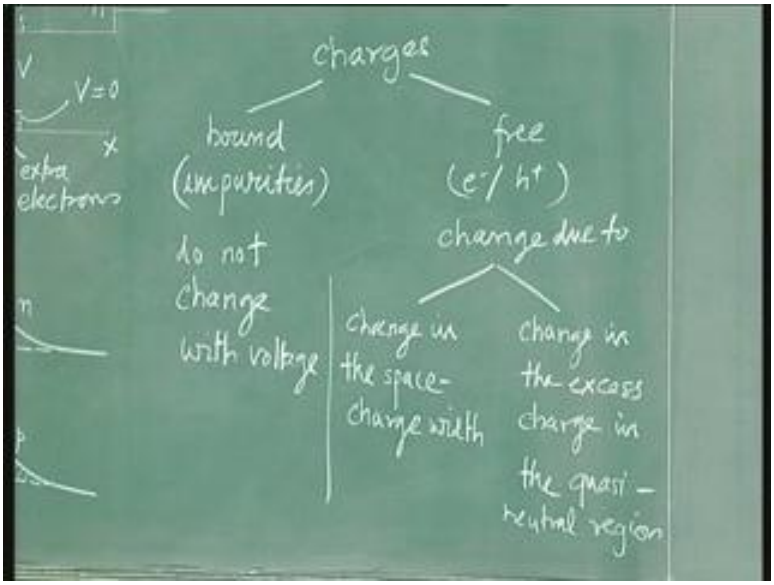

The changes in the free carrier charge are indicated here in the diagram. The shaded area shows the excess holes which are coming because of the applied voltage V as compared to the equilibrium conditions. Now we can estimate the capacitance by taking the some of these hole concentrations and then dividing by the incremental voltage. So in this case the incremental voltage is v itself because we are comparing it with respect to equilibrium condition. Alternately we could write down an expression for these excess holes and we could differentiate this expression with respect to voltage. Now there is one point you must remember that while estimating the capacitance you can either take the change in the positive charge or the change in the negative charge so the term dQ here represents either the positive or the negative component. That is why we normally put a modulus on this particular term to represent the capacitance.

The capacitance is always positive so you can either take the positive component or the negative component. If you take the negative component this term will be negative so you have to take the magnitude to take the capacitance. So we will take the positive component of this charge for estimating the capacitance. And for any capacitance the positive and negative component will always be equal because the device as a whole is charge neutral.

Now let us write down the expressions for this excess hole charge. We will take the space charge region and the quasi-neutral region separately. Let us take this space charge region first. What is the formula for these excess holes as compared to the equilibrium condition can be written as follows. Let us represent the excess hole concentration in the space charge region as Q_p suffix d where d stands for depletion. So we are calling this either space charge or depletion-region. So Q_p is excess hole concentration that has come in at voltage V because of change in the depletion-region.

So Q_p d is this particular shaded area and we can write that as the depletion-region width on the p-side that is X_p minus X_{p0} the change in the depletion-region into Q into the acceptor impurity concentration there N_a into the area of the junction. So this area of the junction is a cross-sectional area in direction perpendicular to the board. In this case here this width is X_p and this width is X_{p0}. In fact this formula should be written X_{p0} minus X_p because X_{p0} is more than X_p and this is the Q_p hole charge. Now what one can do is one can differentiate this with respective tp voltage. The voltage dependence comes because of the dependence of X_p on voltage the depletion width on the p-side on the voltage. So you can differentiate dQ_{pd} by dV and we can write this as q times and we have to take a modulus so q N_a into a into d Xp by dV, there is a negative sign here because this is minus X_p. So this would represent the capacitance contribution due to the space charge region.

Normally this contribution is shown using a symbol C suffix depletion because this is a capacitance due to changes in the depletion layer. So, one can evaluate this by substituting the expression for X_p. I will leave it an exercise for you to derive the expression for the capacitance C depletion by substituting the expression for X_p and differentiating with respect to the applied voltage. What I will do here is I will derive the final expression by a different method which is much simpler and which is more physical rather than mathematical.

Now this method can be understood as follows: You take only the increments and let us see how the incremental picture of this charge looks like. The incremental picture can be drawn as follows. This is the p plus side and this is the n plus side and this is the PN junction, this is incremental hole charge and this is incremental electron charge so this is the so called Q_pd. Now, if you take this increment between any two voltages that is this edge corresponds to voltage V and this edge corresponds to V plus dV. Therefore this is the increment dQ_{pd} because of increment dV then this thickness of these regions will be very small. So here we have shown these changes with reference to the equilibrium condition. So this is v and this is equilibrium.

Supposing this V is very small as compared to equilibrium then this V is nothing but the incremental voltage dV. Or alternately we can draw the picture for any two voltages which are different only by an incremental voltage dV and that is what we have done here. So, for one voltage V this is the picture and for another voltage V plus dV depletion has shrunk and this is the picture, dV is very small so this thickness is very small. And this is the corresponding picture on the p-side.

Now this picture corresponds to that of a parallelepiped capacitor, you can very easily see this like a parallel plate capacitor whose distance is between the charges which is nothing but the depletion-region X_d and the charges around this side. This is an incremental picture and we are interested in the incremental capacitance which is dQ by dV. So, the incremental picture of the changes of in charges at the edges of the depletion layer is similar to that of a parallel plate capacitor, the distance between the plates being X_d.

We can very simply write this particular capacitance that is the depletion capacitance. We can show that this will be equal to epsilon into A by X_d. This is a capacitance because of a parallel plate capacitor plate separation X_d. This is the physical approach to determine the equation. You can mathematically do this expression, work out and then show that this is nothing but epsilon A by X_d. Oone clarification is, this is the change in the depletion layer charge so it is shown on a negative side because on the p-side the space charge is negative and on the n-side the space charge is positive.

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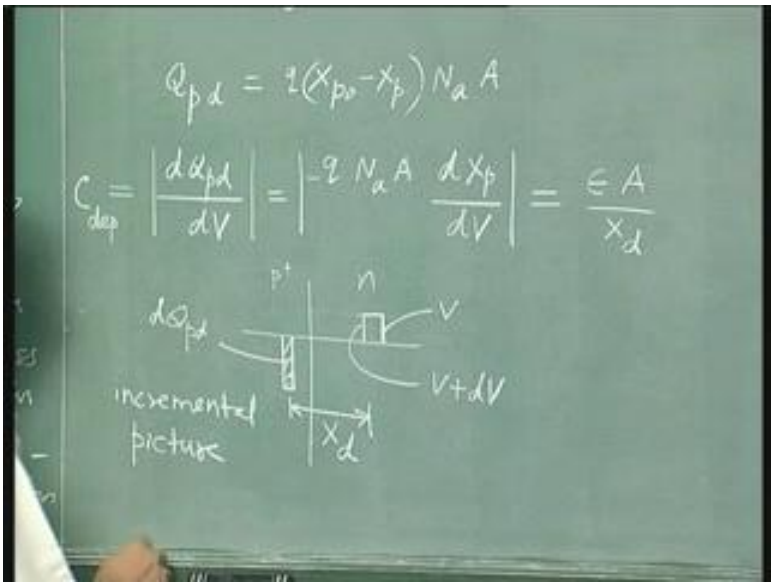

Now one might wonder that how the change in the negative side has been shown as the hole dQ_{pd} change in the positive charge. Here what you are seeing is the magnitude of the change in the positive charge so the negative charge is decreasing in magnitude. In this previous figure this is the negative charge and when you apply more and more forward voltage the negative charge decreases so what is shown is the change in the negative charge. So the decrease in negative charge means increase in positive charge so if you

want to show that more accurately then you must show the dQ_{pd} as a rectangle on this side. And dQ_n is the change in electron charge on this side as a rectangle here.

Here we are discussing about the magnitude of dQ_{pd}. So this shaded area is the magnitude and we do not care about the sign when you are talking of the magnitudes. This is how one can estimate what is called the depletion component of the incremental capacitance of a diode. Now we should see how we can determine the diffusion component of the capacitance. That is, the capacitance or incremental capacitance because of charges in the quasi-neutral regions. This particular capacitance is called diffusion capacitance because these chargers in the neutral region contribute to the diffusion current of the diode.

Now you might have a doubt, how does this charge contribute to diffusion current? This is the majority carrier charge. This is an important point you must note that this charge is equal to this charge because this region should be quasi-neutral. So, the sum of these two charges which are the excess holes in the neutral regions is equal to the sum of these two charges which are these areas. And you know that the excess minority carrier charge contributes to the diffusion current on the p-sides just as the excess minority carrier charger or hole charge contributes to the diffusion current on the n-side. That is why we can estimate the capacitance by summing up these two areas. And therefore this capacitance is referred to as the diffusion capacitance.

Now let us discuss the estimation of the diffusion capacitance. The diffusion capacitance can be written as differential of the sum Q_p plus Q_n by dV where Q_p is this charge which is the excess charge due to minority carrier stored on the n-side and Q_n is this charge the area under this excess carrier concentration stored on the p-side and this is excess electron charge stored on the p-side. Here we want to find out the total number of excess holes because of voltage V which is this plus this. But since this area is equal to this area and we know that distribution of minority carriers can be solved very simply using the continuity equation so instead of summing up these two we are summing up these two.

One should not think why are we summing up the electron charge and the hole charge. Electrons are negatively charged and holes are positively charged. So we are not summing up negative and positive charges but we are summing up magnitudes. Actually we are summing up the hole charges on the two sides of the quasi-neutral region. But since the magnitude of excess hole charge on the p-side is same as the magnitude of the excess electron charge on the p-side we are summing up these two and these two can be written down easily. This is where you must understand the quasi-static approach and why the word quasi-static is being used is because this distribution which I have drawn here is known for this static or steady state condition and they are exponentials, therefore the area can be easily determined once you know the distribution.

In steady state conditions the distribution is exponential because you take the continuity equation for the minority carriers and then you set the rate of change of the minority carrier concentration as 0. For example, if you want to get this exponential distribution then you take the continuity equation for holes and you are going to set dow p by dow t in the continuity equation to be 0. Let me write that equation here to show this.

So dow p by dow t is equal to minus 1 by q dow Jp by dow x minus delta p by tau.
This is the continuity equation for holes on the n-side. To get the distribution of holes you are going to set this equal to 0 under steady state conditions. Now you are going to use this exponential distribution update under steady state conditions to estimate the changes in the charges also under non steady state or time varying conditions or the voltage varying with time conditions. This means you are setting this dow p by dow t not exactly equal to 0 but approximately equal to 0 so that you can still use the continuity equation setting these terms equal to 0 and get the exponential distribution and then work with that. So approximately equal to 0 means quasi-static. And for dow p by dow t when the conditions are varying with time it is not equal to 0. That is why strictly speaking the distribution of the holes will not be exponential.

So, coming back to the estimation of Q_p and Q_n we can easily write the expressions for Q_p and Q_n by looking at this diagram and our knowledge of the distribution of holes and electrons. So we write Q_p is equal to Q(delta p) into diffusion length L_p into the area A of the cross section of the diode. This is your excess carrier distribution delta p, this is diffusion length L_p and here the area under this rectangle is same as the area under this exponential. Here this is the area that we are interested in. Now similarly one can write down the expression for Q_n also. Now what we will do is since we are considering a one sided junction the p-side doping is much more than n-side therefore we will neglect Q_n compared to Q_p which will help as to get a simple equation for the diffusion capacitance.
So we assume Q_n less than Q_p since p to the power plus n junction. With this approximation and this equation you get the equation for C diffusion as d by dV of Delta p into q L_p into A.

Now we know the expression for delta p as a function of v that is delta p is equal to p_{n0} exponential of V by V_t minus 1. So, if you differentiate this with respect to V you will get p_{n0} exponential of V by V_t by V_t which you can write as delta p plus p_{n0} by V_t. This term is nothing but p_{n0} exponential V by V_t so you shift this minus 1 on this side and that is how you get this equal to this from this equation. So we can write this here as this is equal to qA L_p into delta p plus p_{n0} by V_t. Now, when you are talking about forward voltages this delta p is much greater than p_{n0}.

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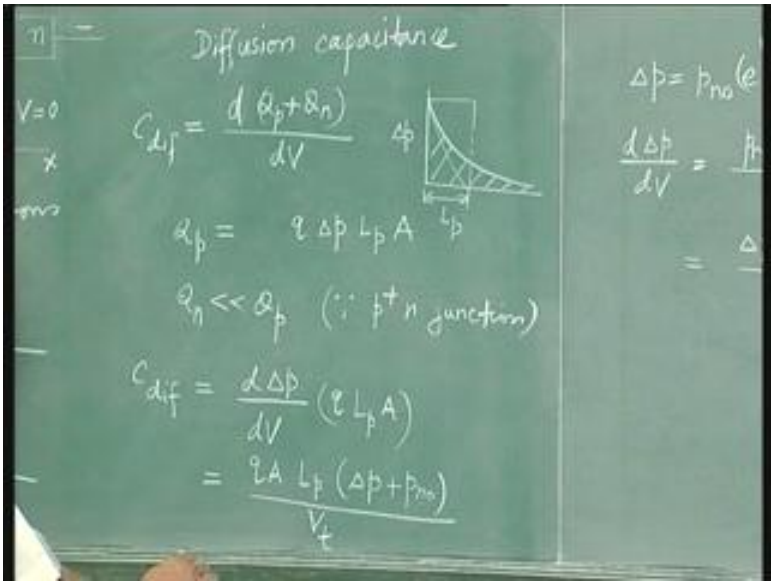

So we can approximate for forward voltage conditions or for forward bias the diffusion capacitance C dif approximately equal to qA L_p delta p by V_t since we have neglected p_{n0}. Now, we can write this term very simply in terms of the current. We know from our diode theory that for p to the power plus n junction the forward current I is approximately equal to qA delta p into Dp by L_p. This is the diffusion current and we are neglecting the diffusion current because of electrons.

So look back into the forward diode equation which we have derived and you will find this equation. We can write this equation by multiplying by lifetime tau and divide by lifetime tau and then we can identify this term as L_p square. Now this L_p square will cancel with L_p, one of this L_p terms will cancel and so this is equal to qA delta p L_p by tau. So from this equation of a forward current it is clear that you can write the numerator qA L_p delta p as I into tau. So this is equal to I tau by V_t. This is the formula for the diffusion capacitance. This is very easy to remember because current into time is charge and charge by voltage is the capacitance. So the characteristic voltage is the thermal voltage and here this is the characteristic time that is that the lifetime.

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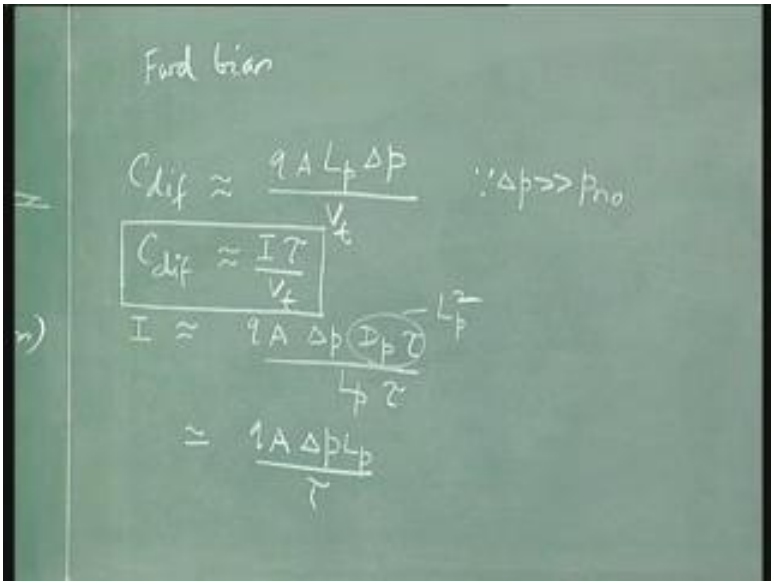

So this enables you to write down an expression for the diffusion capacitance very simply in terms of the forward current. Please note that this is derived under the condition that it is a one sided junction when we neglect the electron charge on the p-side. Now what happens under the reverse bias?

In the reverse bias this excess carrier concentration Delta p is negative of p_{n0} because you have depletion of carriers in the neutral regions. So delta p is minus (p_{n0}) so these two terms cancel and the diffusion capacitance goes to 0. Now this will happen for reverse bias voltages more than $3V_t$. For reverse bias voltages less than $3V_t$ there will be some small diffusion capacitance. But generally we operate in reverse bias voltages more than $3V_t$ therefore diffusion capacitance is taken to be negligible under these conditions. Now we can summarize the results of our small signal analysis as follows. From the DC current voltage characteristics where in the current is proportional to exponential V by V_t minus 1 we get the small signal resistance r of the diode that is shown here. So this is the equivalent circuit under forward bias. This r is V_t by I where the I_0 term has been neglected as compared to I.

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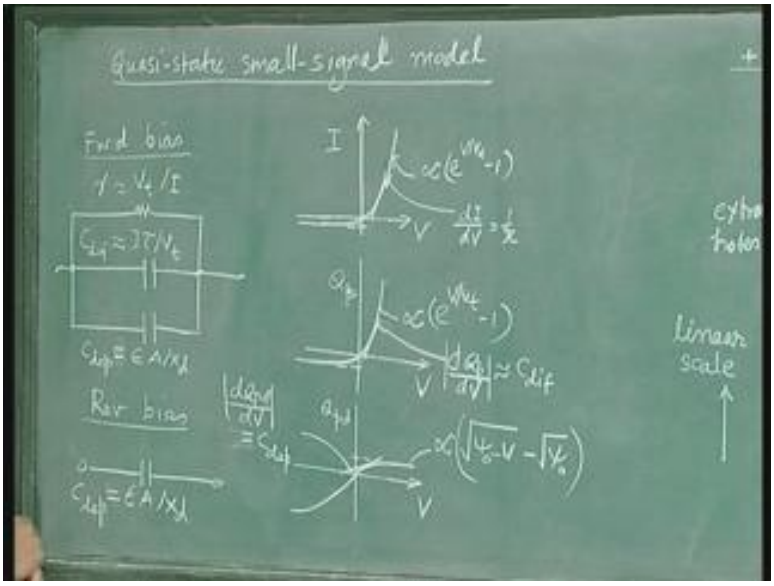

Now this is obtained as the slope of this particular curve so it is dI by dV is equal to 1 by r. Now consider this stored charge in the neutral regions taking only the store charge in the lightly doped region for a p to the power plus n junction. This Q_p varies with V in the same way as the current so this is also exponential behavior and this is also an exponential behavior. You can check this from the formula that we have derived for Q_p which was Q_p is equal to Q Delta p L_p into A. So you can write expression for Delta p and you can show that the Q_p will be proportional to exponential of V by V_t minus 1. Then you take the slope of this curve and this gives you the diffusion capacitance. So dQ_p by dV is the diffusion capacitance.

Similarly, you take the hole charge that is injected into the device because of shrinking of the depletion layer in the forward bias and that follows this particular behavior as shown in this graph. Here this particular quantity is proportion to square root of psi_0 minus V minus square root of psi_0. This is because of the change in the depletion layer width. Here Q_pd is negative for reverse bias because here when you apply a reverse bias this is positive with respect to this and then the depletion-region expands so the quasi-neutral region shrinks and therefore you are extracting holes from this side and electrons from the other side. So the extracted holes are what are represented here for reverse bias. So you take the slope of this and then you get the depletion capacitance.

The depletion and diffusion capacitances are shown here. The results are that C diffusion is current into lifetime by thermal voltage and depletion capacitance equal to epsilon A by X_d where X_d is the depletion width. The depletion capacitance can be seen physically as a parallel plate capacitor. This is an incremental capacitance and it is like a parallel plate capacitor so the incremental charges are separated by the distance X_d. For reverse bias you should put equal to sign exactly and the depletion capacitance is again given by epsilon A by X_d and here X_d goes on expanding so depletion capacitance falls. We do not show any diffusion capacitance or resistance in reverse bias because as we have said the

diffusion capacitance is negligible and resistance is very high so those two elements do not exist for reverse bias.

For moderate forward bias where the devices are operated generally the diffusion capacitance dominates over the depletion capacitance. So this quantity is negligible for moderate forward biases. Now it is of interest to look at the reverse bias capacitance or depletion capacitance for reverse bias in a little bit detail as this quantity is useful in several applications. Since the reverse bias diode is almost like a pure capacitor without any parallel resistive component or loss component and this capacitance varies with voltage an important application of a reverse bias diode is that of a voltage Variable capacitor.

Now, another application of diode in reverse bias is, we can show that we can extract the doping level in the lighted dope region from the measurement of the reverse bias diode capacitance. To see this let us expand the formula; C depletion is equal to epsilon A by X_d. We write X_d is equal to 2 epsilon V_R plus psi_0 where V_R is the reverse bias upon q into 1 by N_d plus 1 by N_a. Then here we recognize that, since N_a is much greater than N_d this quantity can be neglected the one sided junction. We should put a square root here. Now, for the one sided junction we can substitute for X_d here and then we can simplify and you can show that 1 by C depletion square can be written as 2 by epsilon A square q into 1 by N_d approximately equal to this quantity. Here we are assuming that N_d is much less than N_a.

Of course we should write the V_R plus psi_0. And what we find from here is 1 by C depletion square versus the reverse bias V_R is a straight line whose slope gives you N_d. So slope of 1 by C depletion square versus V_R is equal to 2 by epsilon A square Q_nd. So, if you know the area A and you measure 1 by C depletion square and plot it on the function of V_R then you can get the N_d. Let us look at the measured characteristics of reverse bias capacitance. This is shown in this slide.

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You can see that it is almost a straight line. Here CJ indicates the junction capacitance, this is another symbol used normally for the capacitance. This is a function of applied bias and that is why it is shown on the negative access so these are reverse voltages. These are the values for a typical silicon diode of area 0.32 mm by 0.32 mm.

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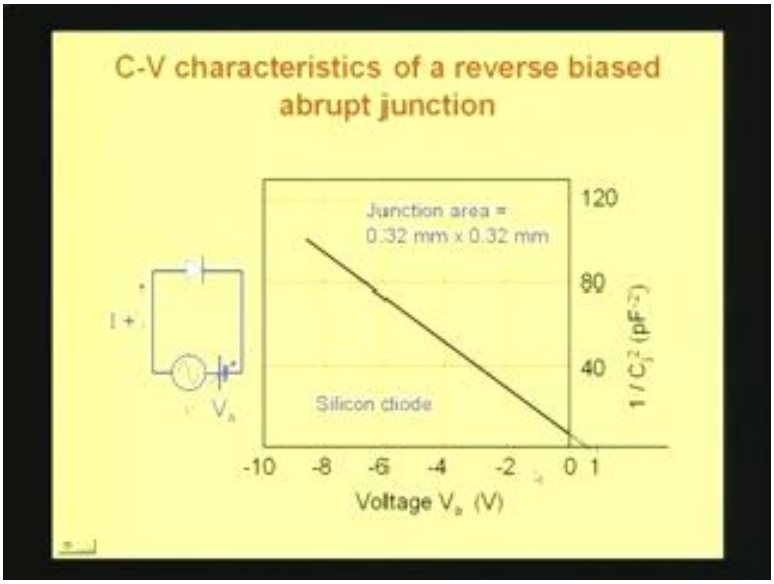

Now the intercept here if you extend this solid line and then allow it to intersect the voltage access the intercept gives you the quantity psi_0 and this can be seen from this particular equation. So V_R is minus psi_0 or if you are writing instead of V_R minus V if you write V_R plus psi_0 as psi_0 minus V then v is equal to psi_0 when the 1 by C depletion is

0. So the intercept this quantity here on this slide shows psi_0 which is this distance so you can extract an approximate value of psi_0 also. The slide also shows the typical values of the capacitances for the area considered. So the capacitances are of the order of Pico farads.

What you see here is square of Pico farads but you can always estimate these values from here and you can see that they are of the order of Pico farads. Now for information if you take the equivalent circuit for the forward bias here since these capacitances are of the order of Pico farads for areas of 0.3 mm by 0.32 mm we have considered the moderate forward bias the diffusion capacitance will be of the order of Nano farads. It can go up to micro facts for larger forward bias.

What about the small signal resistance?
For the small signal resistance see if the currents are in the mA range since V_t at room temperature is of the order of 25 or 26 mV this is of the order of ohms so for 10 mA current 26 mV by 10 mA about 2.6 ohms is the kind of small signal resistance that you get for the diode. Now, before summarizing our discussion on the PN junction if there are any questions I would like to take them.

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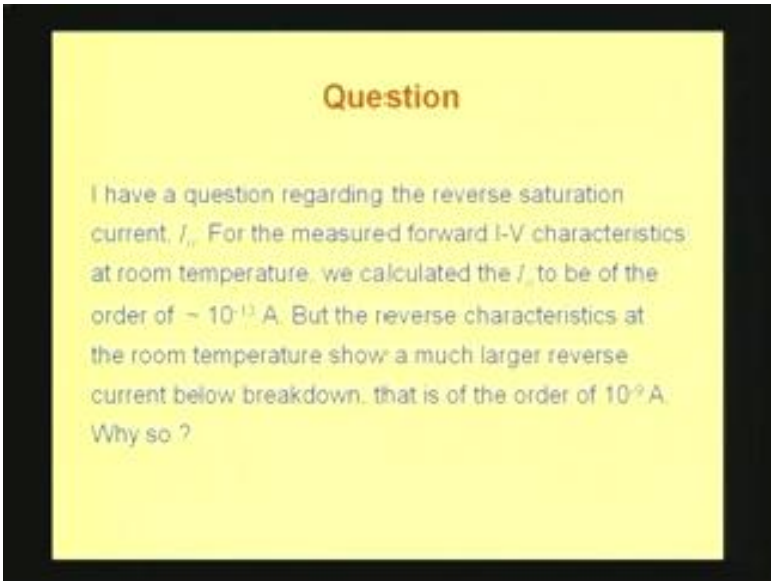

Here is a question regarding the reverse saturation current I_0. For the measured I-V characteristics at room temperature we calculated I_0 to be of the order of 10 to the power minus 13 amperes but the reverse characteristics at the room temperature show a much larger reverse current below breakdown that is of the order of 10 to the power minus 9 amperes, why it is so?
To explain this forward characteristic we found that the I_0 was of the order of 10 to the power minus 13 amperes. But if you see the reverse characteristics here what you are saying is this current is of the order of 10 to the power minus 9 at room temperature

somewhere around this. Now this is because the forward characteristics where explained using the diffusion current and I_0 calculated there was the diffusion current.

As we have pointed out in silicon diode the generation current dominates on the reverse side as compared to the diffusion current. So, though the diffusion current saturates the generation current within the depletion layer dominates the diffusion current which goes on increasing with voltage. Now this generation current within the depletion layer is of the order of 10 to the power minus 9 and that is why you are getting the reverse current of the order of 10 to the power minus 9 amperes instead of the 10 to the power minus 13 ampere current we used for calculating the forward characteristics. Since you have asked a question about the reverse characteristics let me tell you another important aspect of the reverse saturation current. It is found that the reverse saturation current in a silicon diode doubles for every 10 degree C raise in temperature. And for germanium diodes in which the energy gap of the germanium material is less than silicon in fact it doubles for as small as about 4 to 5 degree C change in temperature.

Now how to get this behavior that the current doubles for 10 degree C raise in temperature in a silicon diode?
What you should do is, write the expression for generation current and then for diffusion current and you sum it up. The total reverse current is because of generation in the depletion layer plus diffusion. Now, around room temperature generation current will dominate over diffusion current and the generation current is proportional to n_i. If you take the ratio of n_i at two temperatures differing by 10 degree C around room temperature you will find it is close to 2. At higher temperatures diffusion current dominates over the generation current and the diffusion current is proportional to n_i square at higher temperatures around 100 degree C for example. If you take the ratio of n_i square for two different temperatures differing by 10 degree C for silicon you will find that this quantity will again turn out to be close to about two. This is how the combination of generation and diffusion currents gives rise to this kind of a behavior of doubling the reverse current for every 10 degree C rise in temperature.

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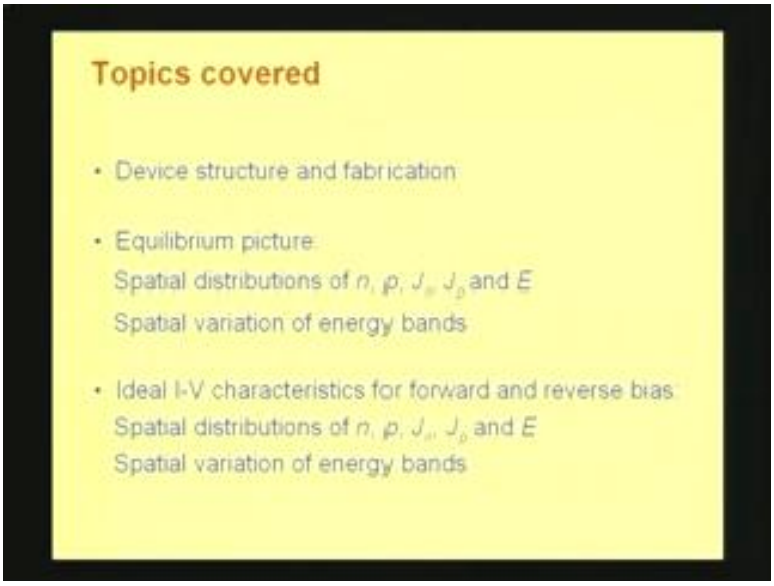

Now I would like to summarize the discussion on the PN junctions:

We covered the following topics in the last seven lectures. First we discussed device structure and fabrication. Then we idealized this structure and used the approximate in the structure for analysis. First we discussed the equilibrium picture in which we gave the distributions of n, p, J_n, J_p and E and we also considered the variation of energy bands. Then we considered the ideal current voltage characteristics for forward and reverse bias. We derived the characteristics based on spatial distribution of n, p, J_n, J_p and E. We showed how the analysis can be done without the aid of energy bands using the five basic equations.

We also drew the energy band diagram for forward and reverse bias to show the advantage you gain in terms of getting information and details using the energy band diagram. Then we explained the non-idealities in real current voltage characteristics namely the ideality factors, series resistance, depletion layer generation current and breakdown. Finally we considered the small signal characteristics where we gave the equivalent circuit of the diode consisting of resistance and capacitance for forward and reverse bias.