Solid State Devices
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Lecture - 23
PN Junction (Contd...)

This is the 23rd lecture of this course and the 5th lecture on the topic of PN junctions. In the previous lecture we derived an equation for the ideal forward diode characteristics which is this equation. Now, this equation was derived in the following steps: When you apply a forward bias of volts we assume that the entire bias is appearing across a depletion layer. The depletion layer shrinks as compared to the equilibrium condition. And then what happens is that the positive terminal injects holes into the n-region and the negative terminal injects electrons into the p-region.

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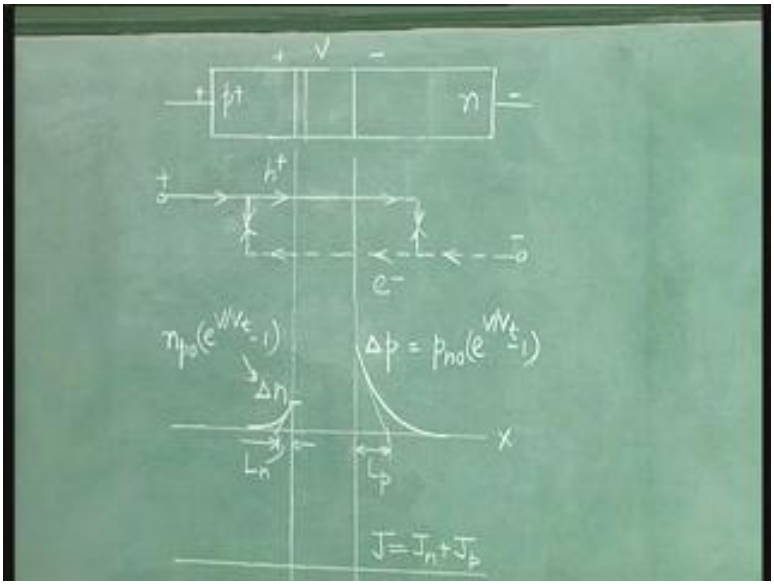

The negative terminal also injects electrons to provide for recombination of holes which are injected from the p-region. And the positive terminal injects holes which supply the recombination associated with the electrons which are injected from the n-region. This is the flow diagram showing the movement of holes and electrons. Next we showed that the concentration of excess carriers at the depletion edge can be obtained using the quasi equilibrium approximation and applying this approximation to the Boltzmann relation. And the result is that the excess hole concentration at the depletion edge on the n-side is given by P_{n0} that is equilibrium hole concentration multiplied by exponential V by V_t minus 1. And a similar relation applies for excess electrons on the depletion edge on the p-side. Then by using the diffusion approximation for minority carriers we showed that the excess minority carrier concentration can be assumed to decay exponentially in the quasi neutral regions.

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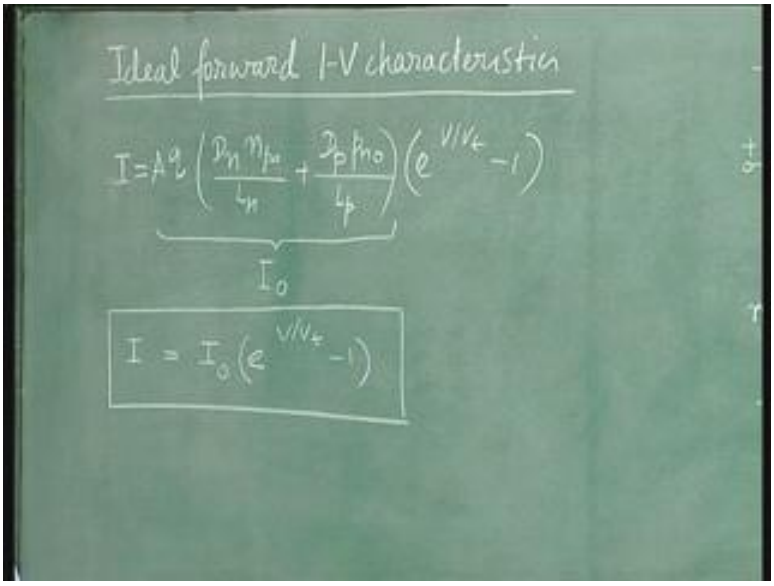

So this is exponential decay and this is the other exponential decay in the n and p-regions. Then we said that based on these excess carrier concentrations we can sketch the hole current for the n-region and the electron current for the p-region because this is based on diffusion approximations. To get the total current we need to know the electron current and hole current both at any one point. This is because under steady state conditions the J is a constant with x. Now, to get the electron and hole currents at any point what we have done is that we have assumed that in the depletion layer the hole currents and electron currents remain constant that is there is no recombination in the depletion layer.

Once we assume that then we can extend this electron current from this depletion edge to the other depletion edge and we can extend the hole current from this depletion edge to the other depletion edge here. And once we do that now we have both electron and hole currents at points within the depletion layer. Therefore we can use this and obtain this particular relation.

Now let us write this relation in a compact form. The first step is to recognize that the current I can be written by multiplying this equation by the area. So we multiply this by area and change the left hand side from J to I. Now we can recognize that this hole term is a constant that we will represent by the symbol I_0. And we obtain the ideal diode characteristics I is equal to I_0 exponential V by V_t minus 1 this is the well known diode equation. Now we have derived this for forward bias and we will be doing a similar exercise for reverse bias a little later. Now let us understand what we should do to complete this picture for electron current on this side and the hole current here and what information do we derive from this. Since we know the total current J we can get the electron current as total current minus the hole current. The whole current is known so from there we can get information about the electron current. So this electron current is simply this constant line minus this line. And similarly we can get the hole current on this

side as this total current minus this electron current. So that completes the current density as a function of X.

Now what are the mechanisms of current flow involved here?
Now this J_p is because of diffusion because this is the current of minority carriers so this can be called as J_p diffusion. Similarly this current is again because of diffusion because these are electrons in the p-region so this is J_n diffusion. Now what about the hole current here? This is the hole current. Now clearly the hole current cannot be because of diffusion because if you assume the whole current to be because of diffusion then the direction of the current will be opposite to the direction of flow that we have shown here. This is because excess holes are equally in concentration with excess electrons. And since excess electron concentration is like this the excess hole concentration also would be given by a similar function. So this kind of a shape indicates the flow of carriers in this direction because of diffusion. This means, if this is the concentration of excess holes then the holes will move in this direction which is opposite to the direction that is shown here.

So evidently the hole current in p-region is not because of diffusion. Similar comments apply to the electron current which is this particular current in the n-region. So majority carrier currents cannot be because of diffusion. This is very clear from this analysis. This means the majority carrier currents must be flowing because of drift. This is quite logical because when you are applying a voltage like this small electric fields will be present in the neutral regions which we have neglected. And these electric fields cause the voltage drops in p-region and n-region. So this small electric fields are sufficient to provide the required hole current in this direction. And in this direction what is shown here is the flow of electrons and not the electron current because for the electrons the current is in the opposite direction to the direction of their flow.

Now returning to this diagram here we can say that this represents the whole current because of drift and this is much greater than the diffusion current of holes for majority carriers so this is mostly the drift current. Similarly this is also the drift current of electrons. So J_n drift is much greater than J_n diffusion. The picture is as following. This terminal injects electrons and these electrons move by drift and they provide for recombination with the holes which are injected from p-region. Then electrons come to the edge and they get injected to the p-side. We have neglected the recombination of electrons during their transit in the depletion layer. Now these electrons when move by diffusion because they are minority carriers here. And as they diffuse they recombine. Similar arguments apply for holes.

The positive terminal injects holes and these holes move by drift in this direction and during the drift they also recombine since they provide for recombination with electrons which are injected from the n-side and then they get injected at this depletion edge on to the other side. But since we are neglecting the recombination in the depletion layer the holes are shown to simply move without any recombination in this edge. Then as they get injected in the n-region they move by diffusion because they are minority carriers in the

n-region and as they diffuse they recombine. This is the picture of the electron and hole flow within the PN junction. Now let us do a solved example.
Explain the important features of these observed forward current voltage characteristics based on the ideal diode theory. The important things we will try to explain on this slide is about how the current of about 1 mA can be accounted for at 0.06 V and also about how beyond this point within a very small voltage range the current rises very rapidly.

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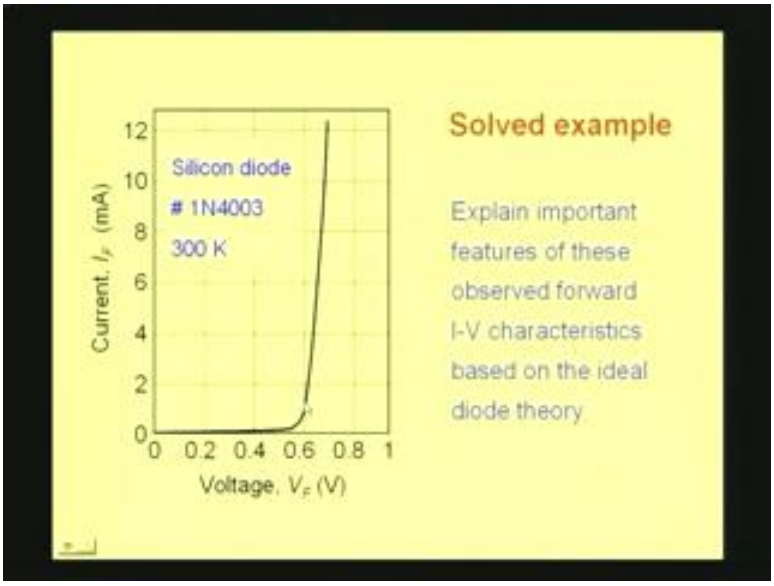

You can see then the current rises from 1 mA to 10 mA within a few tens of mV and that is what is seen here. So let us try to explain this particular feature. Now, this is the equation I is equal to I_0 exponential V by V_t minus 1. Now we have in our observed characteristics this I is 1 mA and this V is 600 mV. Now let us find out how much I_0 is there. Let us try to evaluate I_0 which accounts for this. Now V_t is 0.026 V or 26 mV because we are considering room temperature. So if we substitute these values we get I_0 I by exponential V by V_t minus 1 is equal to 1 mA by exponential of 600 by 26 minus 1. And if you evaluate this value you will get this equal to 9.5 into 10 to the power minus 14 amperes. So this is the value of I_0. This means that for real silicon diodes the current I_0 is of the order of 10 to the power minus 13 amperes which is 1 by 10th of a picoampere.

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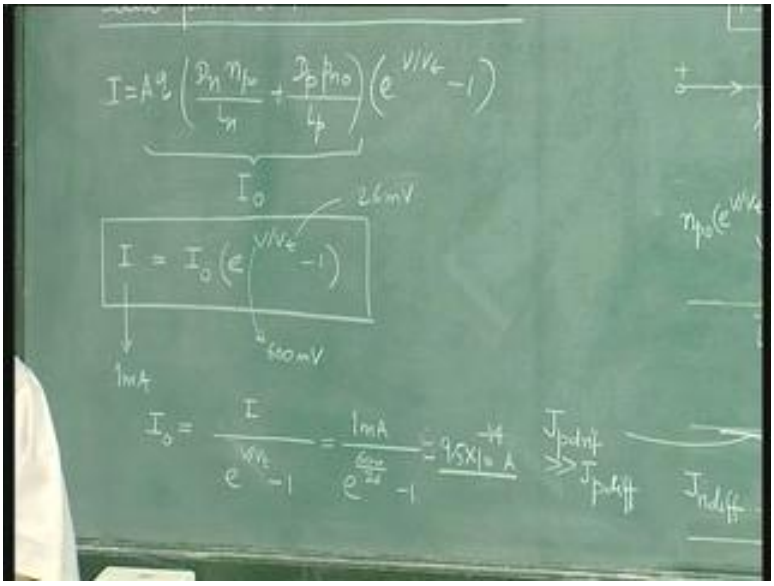

Now if you want to increase the current from 1 mA to 10 mA what should be the change in voltage?

For this purpose we will write this equation in terms of I_1 by I_2 is equal to exponential of V_1 by V_t minus 1 by exponential of V_2 by V_t minus 1. Now we have seen that this V_1 is much more than V_t and V_2 also is much more than V_t in the forward direction for the currents I_1 and I_2 involved. Therefore we can neglect this 1 and from here we obtain V_1 minus V_2 is equal to V_t into ln I_1 by I_2. So, if you want the difference in voltage for a change in current at ten times then we can write I_1 is equal to ten times I_2 and therefore your V_1 minus V_2 is equal to deltaV is equal to V_t l_n 10 which is of the order of 60 mV. So within 60 mV change in voltage you will get a factor of 10 change in current. That is why on this diagram the current changes from 1 mA here to 10 mAs here within an interval of about 60 mV. Suppose this is 1 mA and this is 10 mAs this difference is about 60 mV. Now it is of interest to know what will be the cutting voltage for a diode made in a different material such as gallium arsenide.

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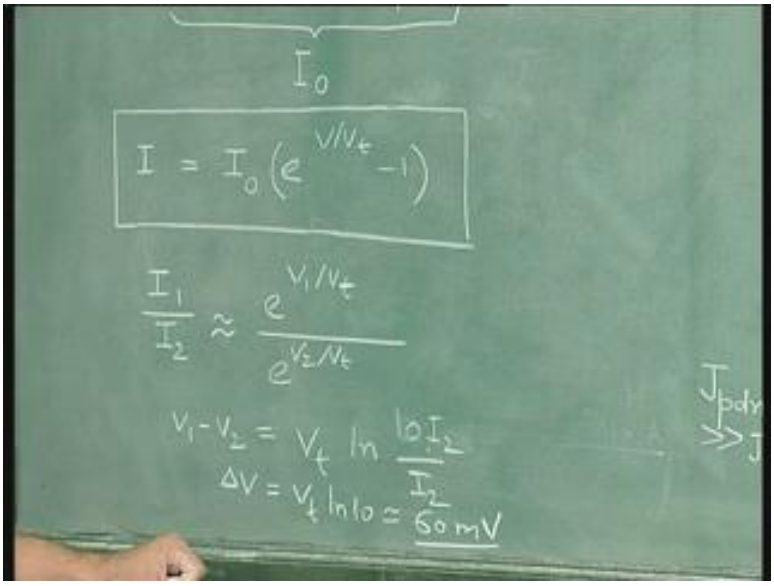

Please note that the cutting voltage is this voltage here which was 0.06 V in our graph here. So this is the 0.06 V point and this is the cutting voltage. We will rewrite this equation to see how a cutting voltage depends on the material parameters. This is equal to A into q and this N_{p0} and P_{n0} we will write in terms of the minority carrier concentration in terms of the n_i square product as n_i square by doping level so this is Dn by l_n N_a plus Dp by L_p N_d into exponential of V by V_t minus 1. And further we will write this n_i square as N_c N_v into exponential of minus sig by V_t and sig is the energy gap.

Now we will make some assumptions to simplify this whole thing. One thing is that since it is a p plus n junction the N_a is much more than N_d so we will neglect this term. And then sincere considering forward dash and for V greater than three times V_t exponential of V by V_t is much greater than 1 so we will neglect this 1 also. Then we will get a simple equation and that is A into q into N_c N_V by N_d into Dp by L_p into exponential of V minus sig by V_t. So here we are getting the equation in terms of all material parameters, this is the energy gap of the material with which the diode is made.

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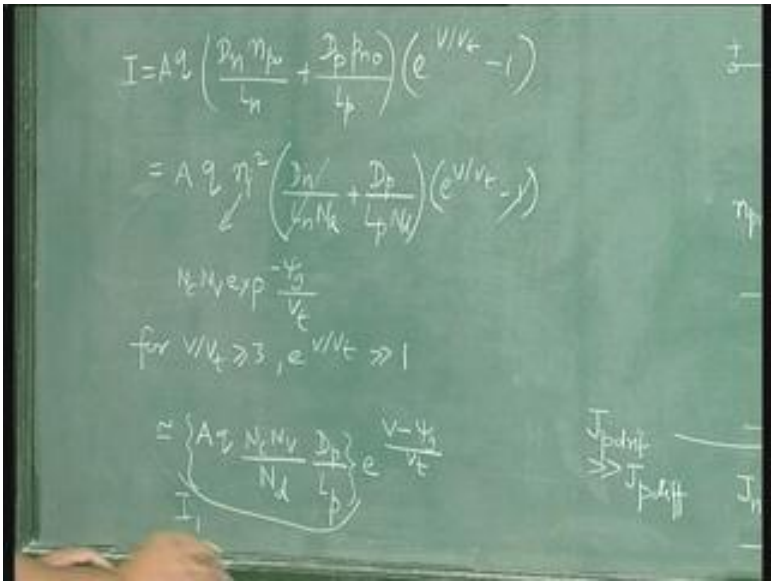

Now we can identify this whole term as a current that we will call I_1 to distinguish it from I_0. So, when we use a symbolism we will get a simplified equation as I_1 exponential of V minus sig by V_t. From here we can clearly see the difference in the voltage for two different diodes for a given current I. So we can rewrite the equation as V is equal to sig plus V_t l_n I by I_1. Now notice here that this I_1 is a large current so the current I is of the order of mAs and when you substitute the values here and you will find I_1 will be of the order of amperes. If this is mAs it will be in fact about hundreds of amperes. And therefore this is actually a negative quantity so it may be useful to rewrite it as minus I_1 by I.

Now we can compare two diodes for any given I a gallium arsenide diode voltage minus this silicon diode voltage would be equal to the difference in the energy gaps plus V_t into l_n I_1 of silicon diode by I_2 of gallium arsenide. So the difference in cutting voltages of gallium arsenide in silicon diodes will be equal to difference in energy gap of silicon and gallium arsenide plus a quantity that depends on these currents which are sensitive to processing and material parameters. Now gallium arsenide energy gap is 1.43 this is 1.43 electron V in energy but in terms of V it is 1.43 V and this is 1.1 V and therefore this difference is 0.033 V. So 0.033 plus V_t l_n I_1 silicon by I_1 of gallium arsenide. So the difference in cutting voltages would be more than 0.033 V. So this is silicon characteristics and this is gallium arsenide diode characteristics, this is about 0.06 and this will be more than about a volt because it is 0.06 plus 0.033 plus a voltage so about a volt. Let us see this clearly on this graph.

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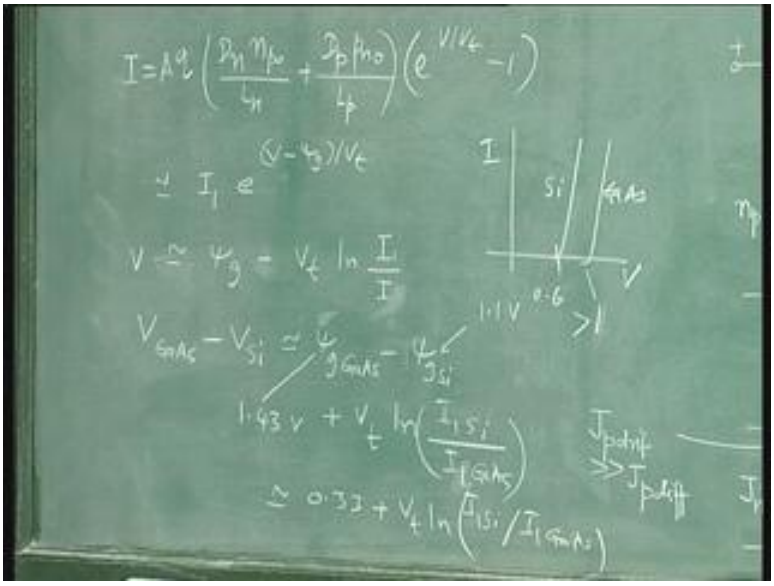

So this is the cutting voltage for this silicon diodes and this is the characteristics for the gallium arsenide diode on which you see the cutting voltage more than about 1. So this difference is about 0.045 or so between the silicon cutting voltage and the gallium arsenide diode cutting voltage.

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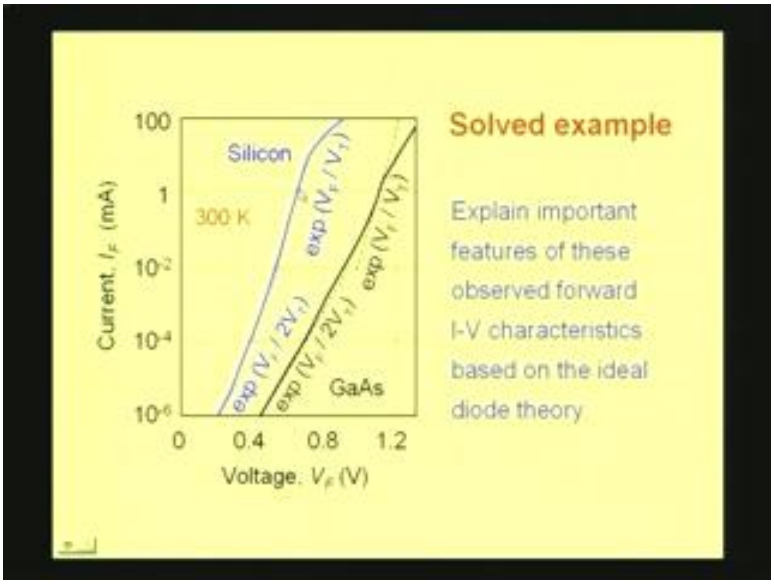

Many times we assume that the cutting voltage represents the built-in voltage of the PN junction, this is wrong. So we need to understand the cutting voltage and built-in voltage both properly. The cutting voltage is the voltage obtained by linearly extrapolating the current voltage curve to the voltage access in the range in which the current are shown in

the graph. So, for example, if you take the current voltage characteristics shown on scale of 0 to 10 mAs here we are plotting the current on a linear axis this is very important. The cutting voltage concept can only be understood with reference to a current voltage characteristics plotted such that the current is only linear scale and the voltage is also on a linear scale.

So, when you plot on the linear scale, if the range is 0 to 10 mAs then your characteristics will look something like this. You extrapolate this region then approximate it by a straight line and extrapolate it here this is the cutting voltage. Now this cutting voltage is dependent on the currents which are being considered on the characteristics. So, for example, if I were to draw the current voltage characteristics in the range 0 to 10 microamperes instead of mAs then your characteristics will look as something like this. So this scale is 0 to 10 microamperes for this curve and the same scale is 0 to 10 mAs for this particular curve. Now you find that you have linearly extrapolated voltage here is much lower than this voltage. So the cutting voltage will depend on the range of currents that you are considering. In fact more specifically it is not exactly the range of currents but the range of currents for a diode of a particular area.

For example, for small signal devices the diodes have a certain area and the currents used are of the range 0 to 10 mAs. So, for diodes of small signal applications 0 to 10 mAs current this cutting voltage of 0.06 V is appropriate for that particular area. Now if you have to go for lower currents using the same diode you will have to use a lower cutting voltage. You may even use cutting voltages of 0.04 V for example if your currents are lower for the diode of that particular area.

On the other hand, if your currents are higher than 10 mAs and if you are going to amperes range you will use a higher cutting voltage. So the cutting voltage is very sensitive to the current range that you are considering in the particular application. It is not a constant for a diode but it is independent of the current range. And also another thing to notice is that this cutting voltage concept can only be understood with reference to a current voltage characteristics plotted with current on the linear access. Now the fact that the cutting voltage would be lower, if you take 0 to 10 microamperes instead of 10 mAs it can easily be seen by looking at the current voltage characteristics plotted on the log scale which shows the currents over every wide range.

The log scale is important to show characteristics over a wide current range. Now, supposing I were took take this 0 to 10 microamperes range then the cutting voltage here may correspond to current of approximately somewhere around 1 microampere. So this current here maybe a microampere but exactly it may be a little bit different but let us assume that approximately it is 1 microampere here which is 1 by 10th of this current. So this extrapolated voltage may correspond to this current.

Now you see that if you take a current of 1 microampere here that will be somewhere here because this is mA axis, this is about 10 to the power minus 3 mA so 1 microampere for a silicon diode and you are here. So this is the cutting voltage. You can see that this is little more than 0.04 may be about 0.045.

On the other hand, in the 0 to 10 mAs scale you are operating here. Then the cutting voltage corresponds to the current of about 1 mA that is here. So you can see the different between this cutting voltage and the cutting voltage corresponding to diodes operated in the microamperes range. Let us now look at the built-in voltage. The built-in voltage is represented here by the potential versus distance curve for a PN junction over which no bias is applied and this device is under equilibrium. So this psi versus x potential versus distance and here this difference in the potential from the two sides is psi_0 which is the built-in potential. Now the potential versus x is normally inverse of the electronic potential versus distance as shown in the energy band diagram because these are electronic energies.

What is shown here is, potential corresponding to negative charges whereas normally by convention the potential psi corresponds to positive charges. So this built-in voltage on the energy band diagram will be shown here on a potential versus distance. This built-in voltage is not a measurable quantity, it is very difficult to measure this quantity because this is in equilibrium condition. So, under equilibrium conditions supposing you connect a volt meter here you will not read any voltage so you should not think that this built-in voltage is a measurable voltage whereas this cutting voltage is a measurable voltage you can measure it because you are measuring a current voltage characteristics under forward bias. You can plot this characteristic and get this cutting voltage and it will correspond to some measurable point on this curve here.

The reason why the built-in voltage which appears under equilibrium conditions cannot be measured is because if this volt meter was able to measure this voltage then it means that the diode was pumping some current to the volt meter because otherwise the volt meter cannot measure and that would mean that the diode is delivering energy to the volt meter. Even though there is no source of energy to the diode itself because it is under equilibrium and no bias is applied so there is no input of energy into the whole arrangement but the diode is giving energy to the volt meter. You cannot have energy out of the device without giving any energy into the diode, it is not possible. This is contrary to the law of conservation of energy, so you cannot measure the built-in voltage.

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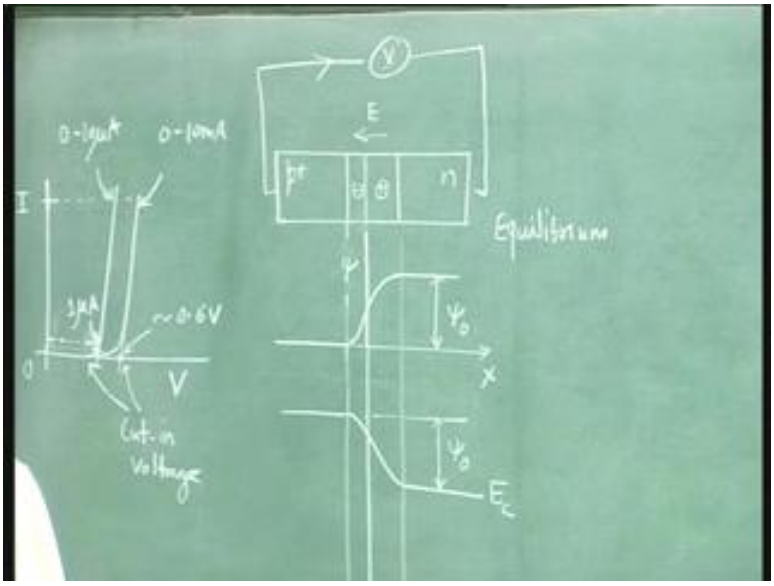

Then one may ask what happens to this potential, does it not come across this voltmeter? It does not come across this voltmeter because the movement you want to connect the voltmeter to the PN junction you are using metal wires here so this is metal and this is also metal which means you are connecting metal regions here. Now what is going to happen is that there is going to a built-in potential between these metal and this n-type semiconductor and this metal and this p-type semiconductor.

Now these built-in voltages which are coming across these two metal semiconductor junctions will cancel the built-in voltage that is shown here for the PN junction and overall in the loop you will get a zero voltage. So as Kirchhoff's law no voltage will appear across the voltmeter because these two voltages are across these two short key contacts because metal semiconductor contacts are called short key contacts. So these two metals semiconductor conduct will have built-in voltages which will together oppose this particular built-in voltage and then you will get a 0.

Now, another misconception students have is that whenever the applied voltage across its diode is more than the built-in voltage then the current starts flowing because they think that when you forward bias the diode then you are superimposing a voltage in this direction which is opposite to this built-in electric field. So unless you remove this complete built-in electric field no current can start flowing. Now this is absolutely wrong because as we have seen, even when you apply a voltage that is very small compared to the built-in electric field. In fact that is the condition under which ideal diode characteristics are derived called a quasi equilibrium condition where equilibrium is disturbed only to a small extent and under such conditions the current starts flowing. And in fact you can never really totally cancel this built-in voltage. So whatever applied voltage is there it comes across the contacts then across the p-region then partly across this particular junction. So this is the voltage across the junction called as vd then you have voltage drop across the n-region and you have voltage drop across the contact here.

Here V_d will always remain less than psi_0. That is, if your V goes on increasing even beyond psi_0 what is going to happen is that the extra voltage beyond psi_0 is going to drop here and this voltage will always remain less than psi_0 but it will approach psi_0. The built-in voltage can never be washed out by the externally applied voltage and whenever the applied voltage is more than built-in voltage the current starts flowing.

So cutting voltage is not the same as built-in voltage. The built-in voltage is a constant for a diode whereas a cutting voltage is a parameter that depends on the current levels which are being used for the diode in the applications. Cutting voltage is a measurable voltage whereas built-in voltage is not a measurable voltage. Now having discussed the aspects let us look at the characteristics again. You find that only in a small range here for the silicon diode the characteristics follow the ideal law of I_0 exponential V by V_t. In higher current ranges that is here as well as in lower current ranges here the characteristics deviate significantly from this exponential V by V_t law.

In fact for very low currents it follows exponential V by $2V_t$ law and for very high currents again it becomes exponential V by $2V_t$ and maybe even different from that later on. And similar things are observed also for the gallium arsenide diode. So here in the lower current range it is exponential V by $2V_t$ and then again at higher currents there is a deviation. We will now explain about these deviations.

Now how to explain the deviations from the ideal diode characteristics?
Now to arrive at these explanations let us look at the characteristics again. You find that in the range where the characteristics are following exponential V by $2V_t$ law the low current range the current is more than that predicted by the ideal diode law. So if you sketch I on the log scale versus V supposing the ideal diode law is going like this, this is the exponential of V by V_t, Now in the lower range you are getting exponential of V by $2V_t$ at every point you can see every voltage instead of this current predicted by the ideal diode law. So clearly your current according to the exponential V by $2V_t$ law is more than the current predicted by the ideal diode which means there is additional current flowing through the diode at low current levels in addition to the currents we have assumed to derive the ideal diode characteristics.

So, what is this current? Now, it can be shown that the additional current is because of the recombination in the depletion layer. Please note that this current was neglected in our ideal diode analysis. We assumed that when the currents flow across the depletion layer there is no change in their magnitude which is the hole current as well as electron current. We have to add this current in the low current range. This is generation recombination in the depletion layer. This is the additional current that flows at very low currents. Now as the current levels increase, however, this current, increases slowly as compared to this current and these two currents are because of diffusion. So this can be seen again here, if you extend this line it goes as something like this whereas you extend the other line which is corresponding to diffusion current it goes like this, this is steeper. In the beginning it is less but after this point it is more. So this current takes over this current in this range.

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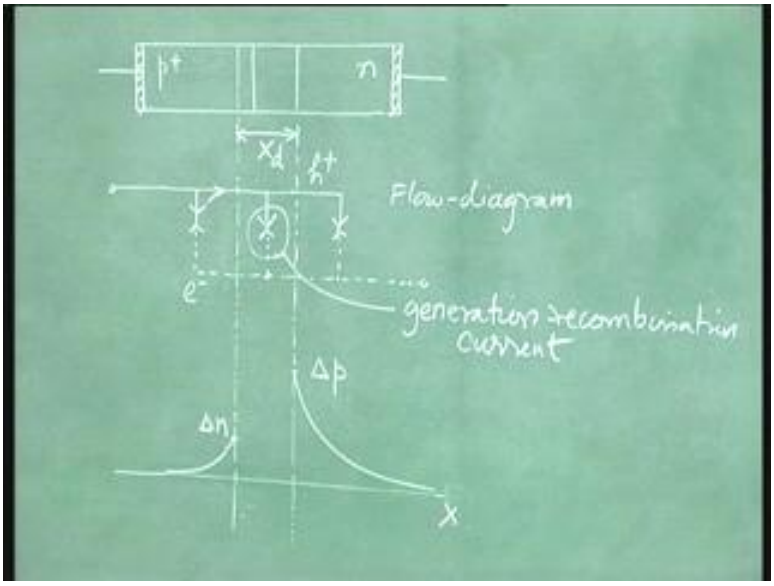

The diffusion current takes over for higher currents whereas for lower currents the generation recombination current is dominating over the diffusion current. If you look at our approximations here, this is the approximation that is not working out at low currents.

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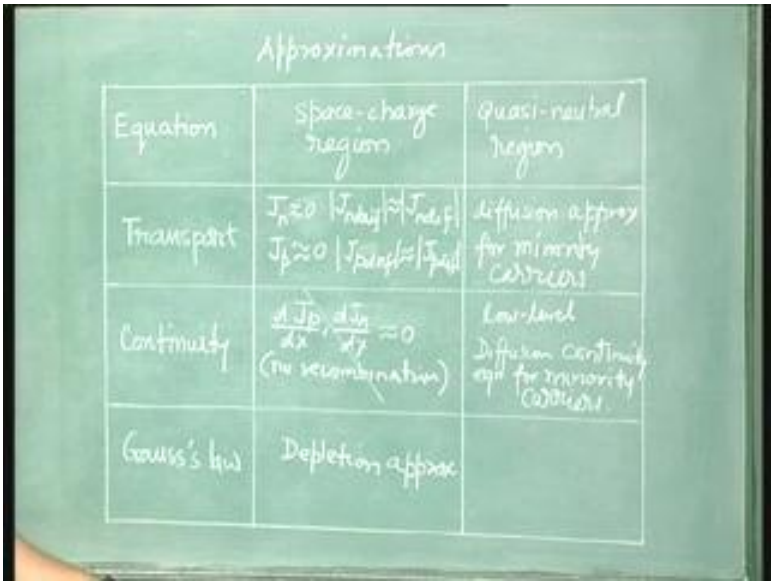

This particular approximation is the one that is getting violated at low currents so we have to relax this approximation to predict the current at low current depths. Now what about high current levels?

Let us look at the characteristics of high currents here again. At high currents the currents are lower than that predicted by the ideal diode law so the currents are lower than this.

This means, if this is the way the ideal diode law goes your actual current is going like this so this current is lower.

So, why is the current lower for a given voltage than the ideal diode characteristics?
The reason for this is that, when the currents are higher high injection levels are reached in this n-region. That means this delta p becomes more than N_d by 10 where N_d by 10 is the doping in this region. N_d is the doping in this region. Once this happens when you have high injection level it turns out that the current due to minority carriers flows not only because of diffusion but also because of drift so you have electric fields generated there when the injection levels are high. The electric fields are generated when the injection level is high and therefore there is a voltage drop here and this voltage drop which we have been neglecting becomes significant across n-region.

Now because of the voltage drop there is a reduction in the amount of voltage that comes across the PN junction as compared to the applied voltage. So the entire applied voltage V is not coming across this junction here because this voltage is there. This can be also called as series resistance effect. It is because of this series resistance effect that your characteristics are showing that the current is lower than you predict based on the ideal characteristics for any applied voltage V. So you can incorporate these deviations in the equation as follows. So real diode equation will be I is equal to I_0 exponential of V minus IR_s this is the so called series resistance because of the p and n-regions. So V minus IR_s is the voltage drop that comes across the junction and that is the V_d by V_t and then you put an eeta there to take into account the presence of other currents for example the current in the depletion layer because of generation and recombination that is accounted for by this eeta minus 1. So this is the real diode characteristics equation, R_s is the series resistance and eeta is the so called ideality factor. For very low currents this term is absent and eeta is about 2. In general, for a current, eeta layer is between 1 and 2. These are the various features of the current voltage characteristics under forward bias.

Now we will discuss about how the energy band diagram looks like under forward bias. Let us look at the energy band diagram under equilibrium. When you apply a forward bias what is going to happen is this equilibrium depletion width is going to shrink which is X_{d0} the 0 here or not stands for equilibrium. And your potential drop across a depletion layer will reduce from q psi_0 to q psi_0 minus V where V is this applied forward voltage, this is the voltage that is coming here. So, if I were to draw a conduction band edge under forward bias then it should look as something like this. This difference is q(psi_0) minus V because psi_0 is in V and we are writing q times this because it is a energy band diagram where you are showing the electron V.

The depletion width has reduced so this is the depletion edge on the p-side and this the n-side and somewhere here you have the depletion edge on the n-side. This is the new depletion width under forward bias. So potential drop has reduced and the depletion width also has reduced.

Now, from here we will draw the diagram under forward bias based on this information. So this is the depletion width under forward bias, this is X_d, this shows the depletion

edges. And now you can see that since the conduction and edge on the n-side has moved up by voltage V and far away from the depletion-region the conditions in the semiconductor are same as under equilibrium the Fermi-level or the so called neutral region where there are no excess carriers. So all the excess carriers are near the depletion edge here, the injected edges carriers are here. So beyond this in this region there are no excess carriers and in that region the Fermi-level will also move up by V because carrier concentration will be given by the difference between the conduction band edge and the Fermi-level.

Therefore what we do is we start drawing the energy band diagram under forward bias by assuming that the left hand side is same as under equilibrium but the right hand side diagram has shifted up by voltage V. So the Fermi-level on the n-type is shown as Volts above the Fermi-level on the p-side. Now this is called as the quasi Fermi-level as under non equilibrium conditions you use a concept of quasi Fermi-levels which we have discussed. So this is E_{fp} and this is E_{fn} quasi Fermi-level on the n-side and the different between these two levels is q(v) where the quasi Fermi-level on the n-side is shown above the quasi Fermi-level on the p-side.

A simple way of remembering that the n-side Fermi-level will go up as compared to p-side for forward bias is you should note that forward bias polarity is this which means n-type is more negative. So, on energy band diagram where you show electronic energies going up, the more negative regions will be shown with higher energies that is why E_{fn} is above E_{fp}. What we have done here is we have drawn E_{fn} and E_{fp} in-regions where there are no excess carriers. So this is the region near the depletion edge where you have excess carriers so the length of this region will be several times the diffusion length here of minority carriers. This is p-side minority carrier diffusion length of electrons so may be about three times L_n because you know that the carrier concentration decay exponentially with distance so over three times L_n the decay will be E to the power minus 3 times L_n by 3 that is E to the power minus 3 times it will decay which means the excess carriers would have come down significantly.

Similarly, this is a distance on the n-side which is three times L_p. L_p is the diffusion length of holes in the n-side. These are the regions where excess carriers are significant. In these regions you almost do not have excess carriers so we first start with the energy band diagram in these regions. Now we can put the other elements of energy band diagram here so you draw E_c and then you draw E_v and a similar thing you can do on this side, this is E_v and this is E_c. Now how do we complete the picture? Now what we do is we look at assumptions one by one.

First we start with assumption that there are no voltage drops in the p and n-regions. This means that the conduction band edge in the n-region and in the p-region should be shown flat, there is a variation in these conduction band edges and also of course similarly the valance band edges. So I can extend the E_c here in this region because there is no voltage draw and similarly I extend E_c here and then extend E_v parallel to E_c so we have completed the E_c and E_v in this region. Now, what we do to the quasi Fermi-level in this region?

Now we invoke the assumption that the injection level in the p and n-sides are low. We have set that quasi-neutral region the injection level is low which is the assumption for deriving the ideal current voltage characteristics. Since the injection level is low it means that the majority carrier concentration is not disturbed. So the electron concentration on the n-side is shown by the difference E_c minus the quasi Fermi-level of electrons on this side that is E_{fn} so this difference shows the majority carrier concentration. Since it is not disturbed even in this region where there are excess carriers we can extend this E_{fn} as a straight line and even here and the same straight line is extended here because the difference between these two should be approximately constant. Injection level is low and the majority carrier concentration is not disturbed.

We do a same thing for E_{fp} on this side because the difference between E_{fp} and E_v indicates the hole concentration on p-side. Now how to we move into the depletion layer. In the depletion layer we have to join E_c as a continuous line because the entire voltage is dropping there and same thing we do to E_v. So this difference is q (psi_0 minus V). What you do to the quasi Fermi-level E_{fn}. We invoke the quasi equilibrium approximation in the depletion layer so this is this approximation.

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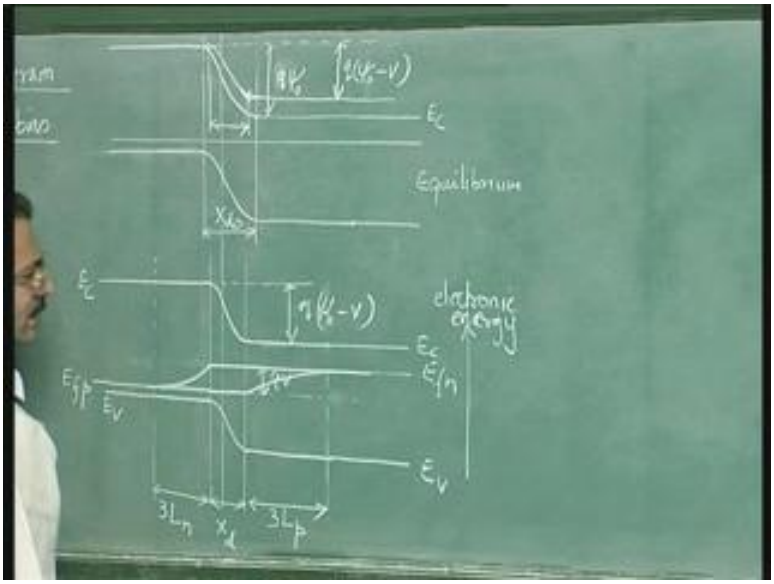

J_n is approximately equal to 0 and J_p is approximately equal to 0. Now, if you look at the transport equation in terms of quasi Fermi-level then the J_n and J_p depend on the gradients of the quasi Fermi-level including drift and diffusion. Therefore gradient of the quasi Fermi-level can be approximately assumed to be 0 which means the quasi Fermi-level is constant. This is the statement of quasi equilibrium. So we extend this E_{fn} in the depletion layer and E_{fp} also in the depletion layer and this is because of quasi equilibrium assumption. Now thereafter we can complete the diagram, the E_{fn} will vary like this, here there are no excess carriers so E_{fn} and E_{fp} are same and here the difference between E_{fn} and E_{fp} shows the presence of excess carriers. And similarly you can do the same thing

on the other side where the E_{fp} varies. And here you have no excess carriers. So this is how the energy band diagram under forward bias is completed.