Solid State Devices
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Lecture - 19
PN Junction

In the last eighteen lectures we have discussed the basics of semiconductors. We considered the equilibrium carrier concentration then we considered Excess Carriers. We saw how the carriers move in response to electric field and concentration gradients, then we saw how we can translate all these basic understanding into five differential equations which described the movement of carriers in any physical situation in semiconductors. These five equations were the two transport equations for electrons and holes, the two continuity equations: one for electron and one for hole and then the Gauss's law.

Starting from these five basic equations we showed with an example how we can analyze any physical situation. The most important in this analysis is the set of approximations which are based on the physical understanding. Now we are ready to consider various semiconductor devices one after the other such as: the diode, the bipolar junction transistor, the field effect transistor and so on. So we will begin our discussion with the basic device namely the PN junction.

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What are we going to do in the lectures on PN junction? We will mention our objectives by showing a set of characteristics which we will try to explain and for which we will try to derive mathematical equations. The first characteristic of interest would be the forward characteristics.

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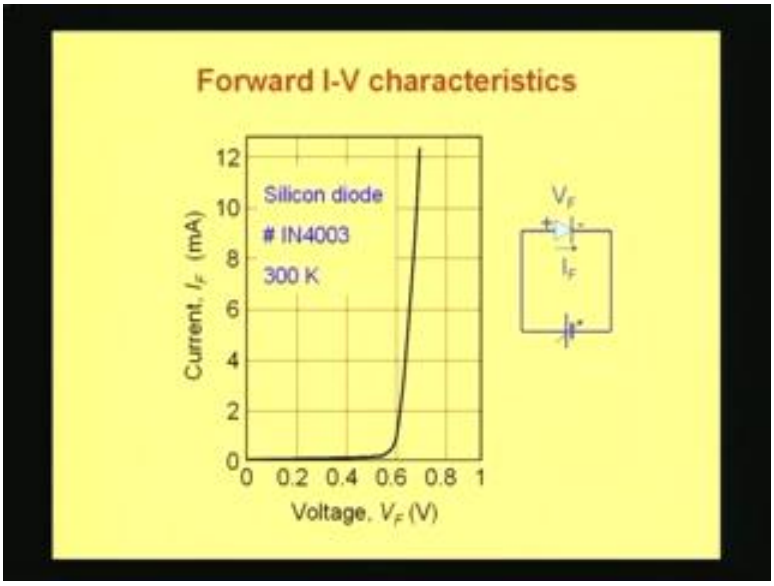

This particular diagram shows the experimental forward characteristics of a PN diode. These characteristics are measured using a circuit as shown here. This arrow indicates the P region and the vertical line here indicates the n region. The forward bias means the p region is positive with respect to the N region. Under these conditions the characteristics which result are shown here. It will be of interest to see the order of the currents. The currents are of the order of mA. This is the small signal diode we are considering and the voltages are less than a volt. The important thing to see in these characteristics is that beyond about 0.6 volts, the current seems to rise very steeply. This voltage beyond which the current rises steeply is normally referred to as the cut in voltage.

We need to explain the physical phenomena which result in these kinds of characteristics where the current rises steeply beyond the certain voltage. Now, it is also important to note that the temperature should be mentioned whenever we discuss characteristics of any semiconductor device. This is because the characteristics are very sensitive to temperature. To understand the kind of behavior this current voltage characteristics indicate it is useful to see the same set of characteristics on a slightly different scale where the current is plotted on a log scale rather than a linear scale.

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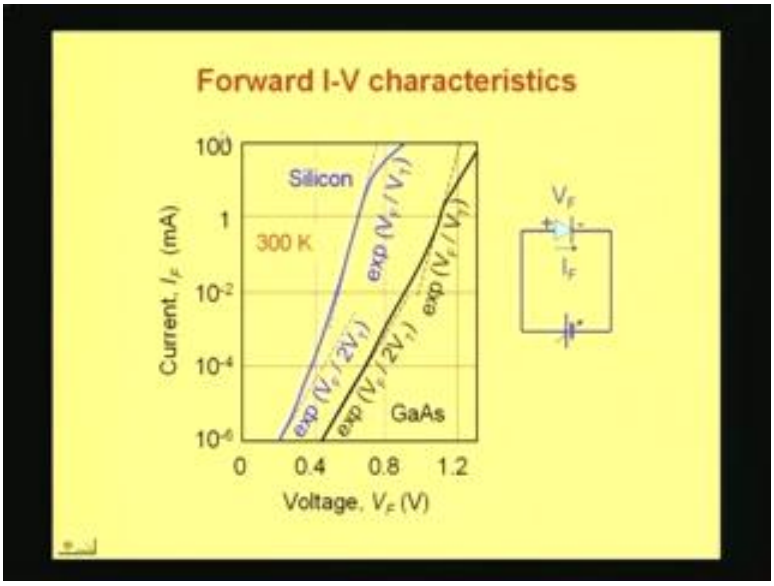

Now, that is the diagram showing the current on a log scale as a function of the voltage. Notice that 0.6 volts is somewhere between 0.4 and 0.8. We find that at 0.6 volts for the silicon diode the current versus voltage seems to be an exponential behavior. That is the current is varying as a exponential of V_F by V_T as it is shown by this dotted line. However, for lower voltages where the current was low on a linear scale the behavior seems to be exponential but in the exponent there is a factor 1 by 2 coming in. That is the current varies as exponential of V_F by 2 into V_T. Now exactly a similar behavior can be seen fall the gallium arsenide diode. Let us look at the diagram. This black curve here is for the gallium arsenide diode. At low currents the gallium arsenide diode also shows the current varying as exponential of V_F by 2 into V_T whereas at higher voltages the current becomes exponential V_F by V_T.

Another thing to see is that at voltages even higher the current is again deviating from the exponential behavior for both silicon as well as the gallium arsenide devices. This is the range where actually if you plot the current voltage characteristics in the linear scale i.e. current on the linear scale as a function of voltage on the linear scale then you will find the current voltage characteristics to be linear. This is the range on the diagram where the current voltage characteristics are linear. We need to explain why there are kinds of variations.

The advantage of plotting on the log scale is that whenever you get the straight line portions on a log of current versus linear voltage scale it implies that the current is varying exponentially with voltage. The exponential nature of the current voltage characteristics is very clearly shown by this log current versus voltage plot. Another thing to see here is that for gallium arsenide diodes the cut in voltage is higher. You can see that for the same current the voltage in the gallium arsenide diode is higher by about 0.2 volts.

We need to explain this particular aspect as to which parameter of the semiconductor is responsible for deciding the cut in voltage. As we will see it will be the energy gap of the semiconductor. We will next see the reverse current voltage characteristics.

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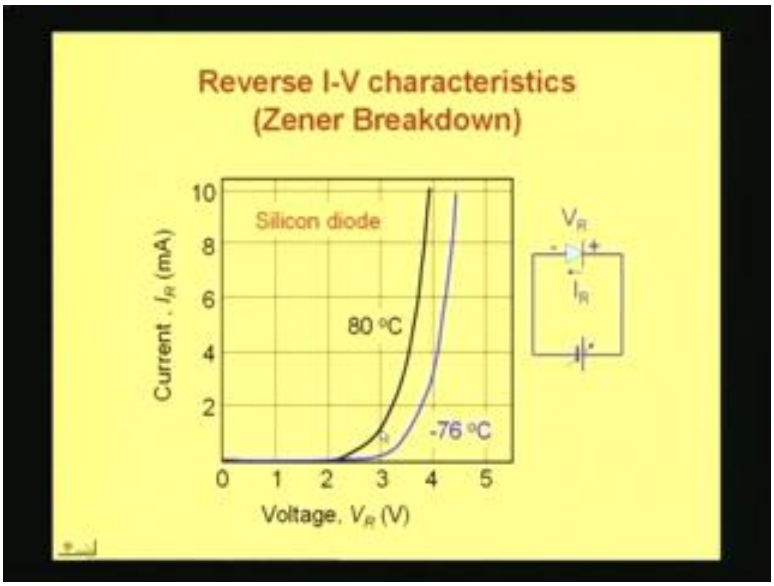

Here are the reverse current voltage characteristics of a silicon diode which has a low break down voltage. You know that the diode is a rectifying device so it must not pass any current in the reverse bias. The reverse bias arrangement is shown here a circuit in which these characteristics are measured. V_R is the magnitude of the reverse bias and I_R is the magnitude of the reverse current. The reverse current flows from the N region to P region. This is the direction of the reverse current. When the diode breakdown voltage is of the order of about 3 volts then you find this kind of reverse characteristics. That is the current starts increasing gradually beyond the breakdown point and then the rise becomes steep.

So whenever the breakdown voltage is low there is a particular mechanism that is responsible for the breakdown voltage called as the Zener mechanism. That is why on this graph you will see these characteristics are referred to as Zener breakdown. An important thing to note here in this diagram is that as the temperature increases from minus 76 to 80 degree C the breakdown voltage is reducing. Which is the breakdown voltage here? It is difficult to locate the exact value of the breakdown voltage because the characteristics are not increasing steeply beyond a particular point. This is rather a gradual increase and that is why these are called soft breakdown characteristics.

You can locate the breakdown by extending this line downwards from here and then take this intersection which is one way of locating the breakdown voltage. Another way of locating the breakdown voltage will be to refer to the voltage corresponding to a particular current e.g. you could take a current of about 1mA and try to see what the voltage is and you can call that as a breakdown voltage. Zener breakdown characteristics

are soft i.e. the current increases gradually. And in these characteristics as the temperature increases the breakdown voltage reduces, this is one thing that we would like to explain. Now let us see another type of breakdown characteristic in the reverse direction and that is the Avalanche Breakdown.

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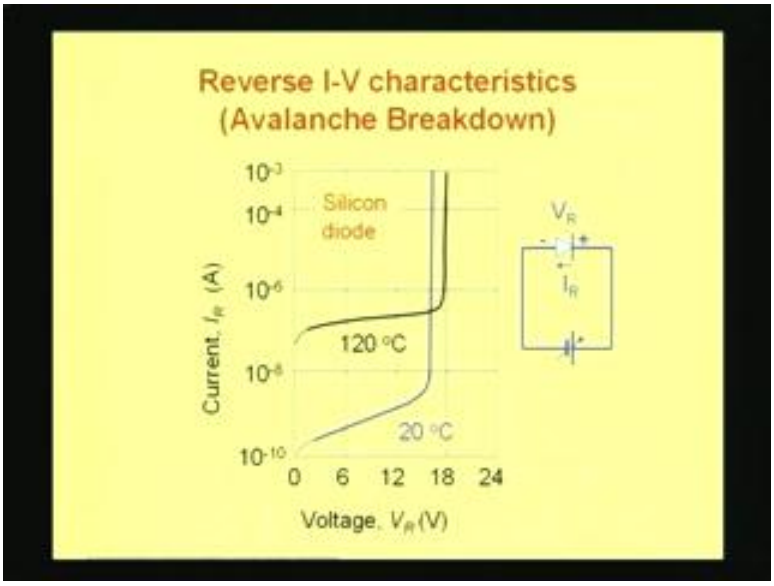

Normally these kind of characteristics are seen when the device has a high breakdown voltage. What is it that decides a breakdown voltage? As we will see the break down voltage is decided by the doping in the PN junction. What is important here is to see that these characteristics are rather sharp i.e. the current seems to rise very rapidly beyond a certain point which we can call as a breakdown point. The breakdown voltage on Avalanche breakdown characteristics can be located very easily and precisely. As against the Zener breakdown voltage for the avalanche breakdown voltage as the temperature increases the breakdown voltage increases. So for 20 degree C this is the breakdown whereas for 120 degree C the breakdown is higher.

We will try to explain why for Avalanche breakdown mechanism the breakdown increases with temperature. We can see this part of the curve which shows that as the temperature increases the reverse current increases. A rapid increase in the reverse current with temperature is another thing we would like to see. You can see that from 20 degree C to 120 degree C the increase in reverse current is more than about three orders of magnitude. So this is about 10 to the power minus 7 here and this is 10 to the power minus 9 which is about two orders of magnitude for 100 degrees change in temperature. After considering the DC characteristics namely the forward current voltage characteristics, the reverse current characteristics below breakdown and the break down voltage of the diode we will go to AC characteristics or small signal characteristics.

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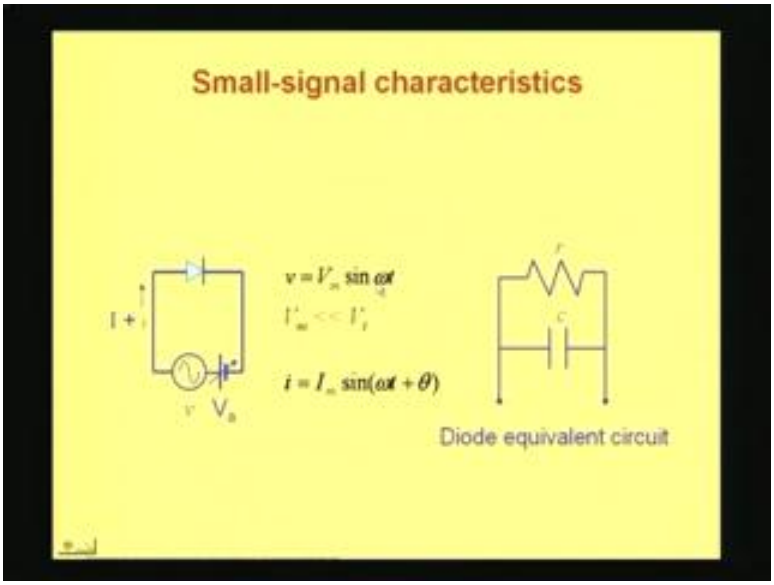

This is a circuit used for measuring the small signal characteristics. It is necessary to emphasize here that there is a DC bias. Small signal characteristics are measured in the presence of a DC current and voltage. This is very important to understand so we should not be under the impression that small signal characteristics are measured by applying an AC voltage to the diode alone. It is not the AC voltage alone but rather a DC voltage over and above which an AC voltage is superimposed and this AC voltage is very small. What is the order of this voltage? The circuit that we are going to develop, the characteristics that we are going to study will correspond to the applied voltage magnitude much less than the thermal voltage. So the applied AC voltage is V_m sin omegat wherein the amplitude V_m is much less than the thermal voltage V_t which means the small signal characteristic. Now what will happen is the current would be given by the small signal current which is present in the circuit in response to the small signal voltage and that would be given by I_m sin omegat plus theta.

There is a phase difference between the voltage and the current. We will try to find out what is the magnitude of the current as a function of the magnitude of the voltage. We will also try to find out the magnitude of the phase and how this depends on the frequency of the applied AC voltage? The applied voltage is V_a, a DC voltage and plus a small AC voltage and the resulting current is shown here as the DC current I plus a small AC current i. This behavior is often represented in terms of an equivalent circuit. You could either give mathematical equations for I_m in terms of V_m and theta in terms of the frequency omega or equivalently we can find out the values of small signal resistance r and the capacitance c in parallel which will represent the diode. So any such behavior of an AC current in response to an AC voltage can be represented also by an equivalent circuit. This is the equivalent circuit concept.

Notice that the resistances r and the capacitance c are parallel. We will try to explain why the resistances and capacitance should be regarded as parallel for this diode and we will

try to find out the values of r and c which in turn depend on the phase theta and the magnitude I_m of the current in response to the voltage V_m and the frequency omega. Next our effort will be to study the capacitance voltage characteristics in reverse bias. We have seen that the small signal equivalent circuit of a diode consists of a resistances r in parallel with capacitance c, this equivalent circuit is valid for both forward and reverse bias but in reverse bias as we shall see the resistances r is very large and the diode is almost like a capacitor. There are lots of applications of a diode under reverse bias where the capacitance of the diode is of interest.

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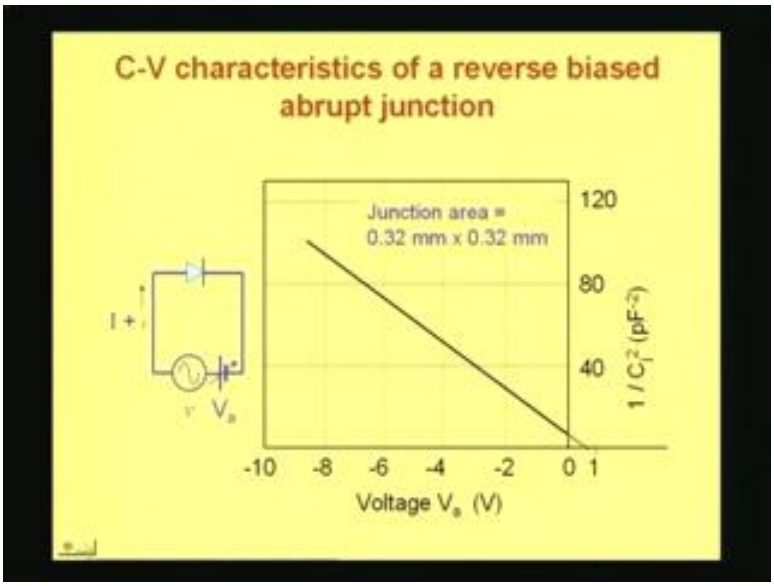

What is the behavior of this capacitance? C-V characteristics of a reverse biased abrupt junction: We will see what is meant by an abrupt junction when we discuss the issue of the topic of junctions in detail.

Right now all that we need to emphasize here is using the variation of capacitance as a function of reverse bias that is shown in this graph here. What you find is if you plot the reverse bias small signal capacitance of the diode squared 1 by C_j square the j here stands for the junction. If you plot 1 by C square versus the reverse voltage notice here that the voltage is negative and this is because what is shown here is not only the magnitude of the bias but also the polarity of the bias. So reverse bias means a negative voltage and forward bias is positive that is the reference. So 1 by C square versus V is a straight line that is what is seen here. We will derive a mathematical relation which will explain this particular behavior. Having seen the various characteristics that we are going to explain namely the DC current voltage characteristics and the small signal characteristics we will now list the various topics we will have to cover to derive these characteristics.

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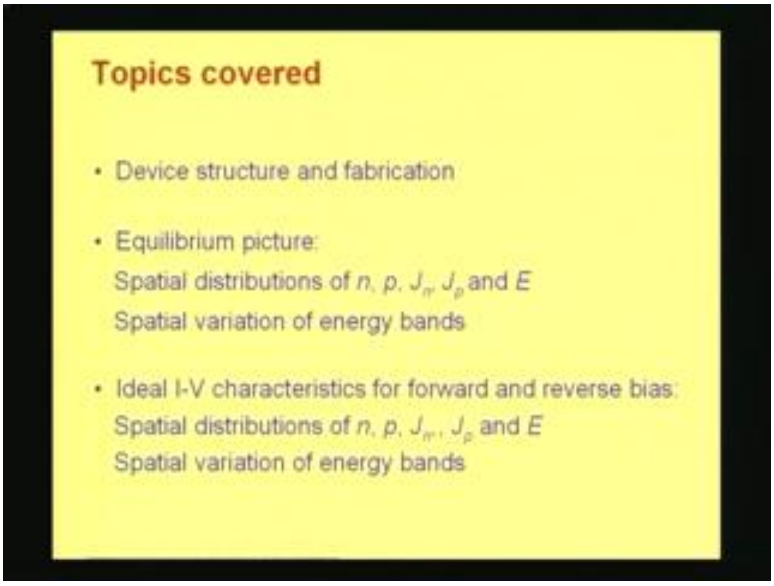

Now these topics are: first we will consider the device structure and how the device is fabricated. This discussion will be brief but this is important to begin with. Then we will consider the equilibrium picture of the PN junction. When no applied voltage is present how does a PN junction behave?
Our aim in this analysis will be to show this spatial distributions of n, p, J_n, J_p and E that is the electron and hole concentrations, the electron and hole current densities and the electric field. This is very much on the same line as that in the solved example which was considered in the procedure for device analysis topic.

Next, we will consider the spatial variations of energy bands under equilibrium. After that we will derive the ideal current voltage characteristics for forward and reverse bias. So we will define an ideal PN junction. Obviously lot of simplifications will be involved but the result of this will be exponential current voltage characteristics. These characteristics will be obtained using the spatial distributions of n, p, J_n, J_p and E. After this discussion we will also show the variation of the energy bands under applied bias. One point I want to emphasize here is that the analysis of the PN junction can be done with or without the aid of energy band diagram. Although we find in books energy band diagrams will be referred to frequently.

It will be useful to see exactly what is the advantage gain using an energy band diagram for PN junction analysis. Most of the analysis can be done without aid of the energy band diagram but there are some advantages in using the energy band diagram. That is you can get some additional and involved details using the energy band diagram. We will clearly see this and do the analysis without the energy band diagram and then we will discuss the energy band diagram.

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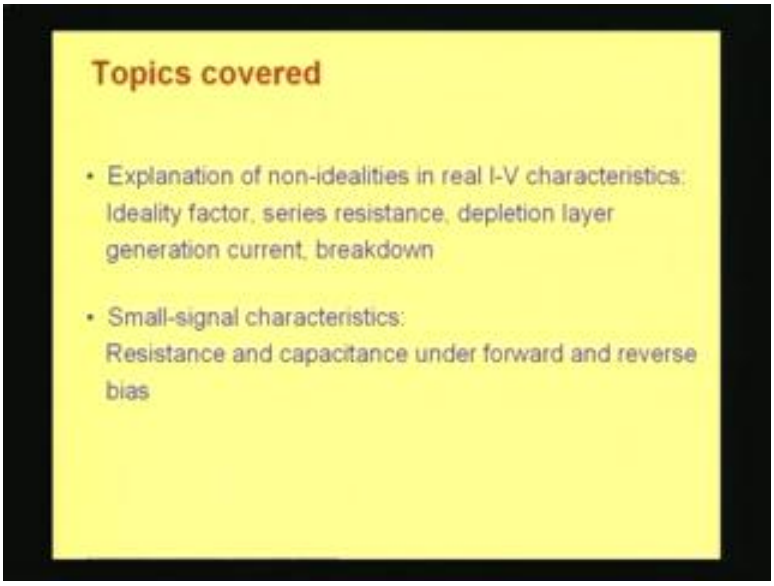

After that we will explain the non-idealities which are present in the real I-V characteristics. Let us also see how the real I-V characteristics differ from the ideal characteristics. More specifically we will explain the ideality factor, then the series resistances effect, then the depletion layer generation current and then the breakdown. So, ideal current voltage characteristics do not explain breakdown.

Finally we will consider the small signal characteristics wherein we will derive expressions for the resistance and capacitance under forward and reverse bias. Let us begin with the device structure and fabrication. Here is a diode that you would have used in the laboratory experiments related to circuits. This is a package device that is it contains the silicon PN junction encapsulated so that leads are available soldering to other components in the circuit. Let us look at the components of this particular device this is called an “axial lead glass package diode” and this has two leads here. Between these two leads a silicon chip is present and this whole assembly is put in a glass tube which is shown here. Now, let us consider the parts of this package diode in detail as shown here.

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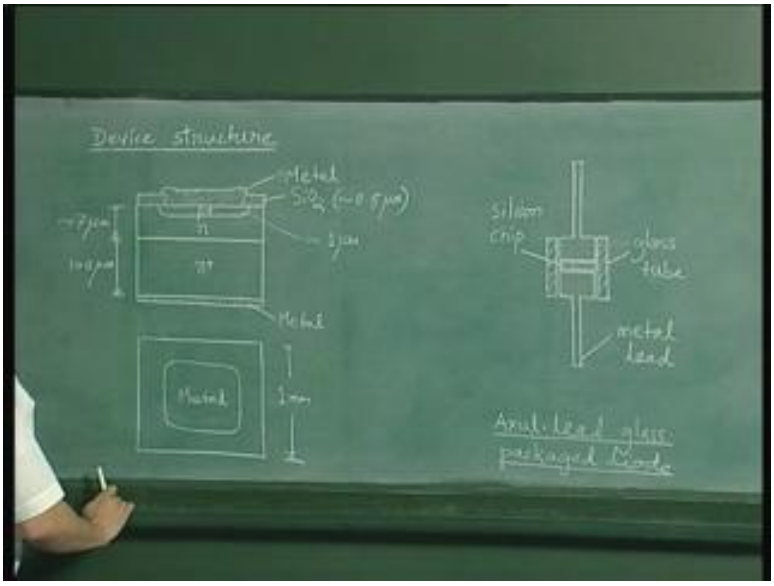

These are the two metal leads between which the silicon chip is held and the leads make a contact to the P and N region which are on top and the bottom. This entire assembly is held or encapsulated in a glass tube. By rising the temperature of this assembly to 600°C glass to metal sealing is ensured at this point, this point, this point and this point where the metal and the glass are in contact. The sealed portions here appear red in color in the photograph.

Let us look at the structure of the PN junction within the silicon chip in detail. This structure is as shown here, this is the cross section of the silicon chip and this is the top view. You can see the top view of the silicon chip shows the area this is about a mm square for this diode that has been shown. The area depends on the current rating of the diode. This is the cross section, it is important to note that the cross section has not been shown to scale. This dimension is about 1 mm whereas this dimension is close to 100 microns as you can see so this is 1 by 10 of this.

We have not shown the device to scale because we want to show the various parts clearly. What you find here is the P plus region or heavily doped boron region of thickness is equal to 1mu has been created through a window in a silicon dioxide layer. This is the planar diode structure i.e. a diode made using a planar process. The thickness of the silicon dioxide layer is about 0.5mu. This heavily doped boron layer is created in an n-type substrate. A part of the n-type substrate here is lightly doped and its doping depends on the break down voltage of the device that is required. The thickness of this layer also depends on the breakdown voltage considerations.

For e.g. for a diode of 30 volts breakdown the doping of this layer would be about 10 to the power 16 by cm cube and the thickness would be about 7mu. Now a 7mu thin silicon substrate cannot be handled very easily. So from the mechanical handling point of view

you need a thicker silicon chip. For this purpose the actual thickness of silicon piece has to be about 100mu or little more than that. Here it is for example 107.

Now if the entire silicon region were lightly doped then it would present high series resistance when the current is flowing between these two leads in the forward bias direction. So to cut down the series resistance what is done is the layer which is not necessary from the breakdown voltage consideration or from the breakdown voltage point of view is converted into a heavily doped region. Here the doping would be more than 10 to the power 19 cm cube so that is why this is an Nplus layer .Now this is PN diode or Pplus N diode. You can also have Nplus P diode that is this layer would be Nplus heavily doped phosphorus, this layer would be boron. In this particular diode this layer is boron and this is phosphorus.

Generally the Nplus region is made using the doping namely antimony and in some cases arsenic. Then, to take metal leads out you need metal contacts so these are the two metal contacts which are deposited on the silicon wafer. The top view of the chip looks something like this so what you notice is this is the metal electrode so this is the top view of this particular region.

Now it is important to note that the top view of the window also would be something like this but this would be smaller than the metal so the window would be somewhere here. The corners of the windows are normally rounded-off to get the required breakdown voltage. Sharp corners reduce the breakdown voltage. So to remove the effect of sharp corners generally these corners are rounded-off. In a planar process hundreds of such devices are made simultaneously.

Let us look at the fabrication steps in detail to understand how this is done. The device fabrication begins with a silicon piece called a wafer which looks similar to this. This is a 4 inch diameter silicon wafer. The thickness of this wafer is 500 micrometer or ½ mm. The thickness is decided by mechanical handling considerations. Now-a-days silicon wafers of much higher diameters are being used. Now you can see that the face of this device is mirror like that is it is polished, it has a mirror like finish. On the other hand, the back side of this silicon wafer is rough because we do not need a fine finish on this side. This silicon wafer is subjected to a number of process steps to make the diodes.

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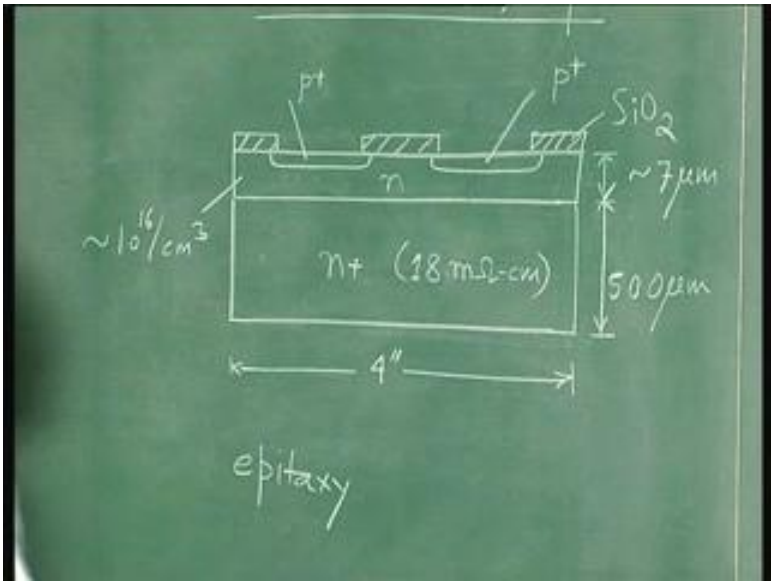

We will now see these steps in detail. This is the cross section of the 4 inch diameter silicon wafer. This is Nplus it is heavily doped and its resistivity is about 18 m omega cm. It is left as an exercise to you to convert this resistivity into doping. On this a very controlled layer of n-type doping that is phosphorus doping is grown by a process called epitaxy. So the thickness of this layer and the doping level both are decided based on the breakdown voltage requirements of this device. For a 30 volt breakdown this layer is about 7mu thickness and its doping level is 10 to the power 16 by cm cube of this order.

The epitaxy is a process which allows you to grow layers of very controlled thickness and doping level. After the growth of this n-type layer a silicon dioxide layer is grown all over this wafer and windows are etched into the silicon dioxide layer to create the Pplus or heavily doped boron layer. So windows will be etched like this in this silicon dioxide layer, this is silicon dioxide and through these windows boron will be diffused to create the PN junction so this is Pplus. This process of creating windows in a layer is called lithography. This is a very critical process in the planar process used for fabricating various devices in modern times. I will be discussing this process of lithography in some detail.

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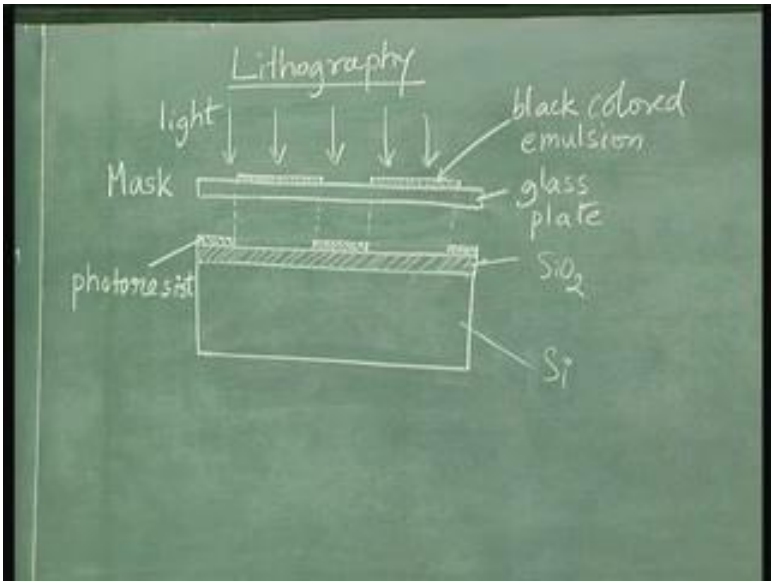

This is the silicon wafer with the silicon dioxide layer grown on it. The first step in lithography is to grow or deposit a layer of photosensitive material called photoresist. This particular wafer with the photoresist material is next exposed to light and passed through what is called a mask plate. This mask plate is actually a glass plate on which a black colored emulsion is present in selected areas where you want to create the junctions. These black or dark areas prevent the light from passing through the plate and falling on the photoresistor.

When light is passed through this mask plate on this photoresist coated layer these regions between the dark areas will be exposed to light and the light will cause a chemical reaction in this photo sensitive material or photoresist and harden these areas. These areas get hardened because of exposure to light. Next what is done is that, this exposed silicon wafer is dipped into a chemical which removes the areas where light had not fallen due to a chemical reaction. So the chemical solution will dissolve these unexposed photoresist portions. This is how windows are created in this photoresist layer using this mask plate.

I will show you how a real mask plate looks like. This is a mask plate, it is a transparent glass slab and you find dark patterns in selected areas. Coming back to our discussion of the lithography process this silicon wafer containing a photoresist layer etched in selected areas is dipped into a chemical solution which can etch the silicon dioxide.

A chemical that can etch the silicon dioxide is hydrofluoric acid. When this wafer is dipped in hydrofluoric acid these photoresist regions prevent the acid from attacking the silicon dioxide beneath. As a result the silicon dioxide will be etched only in these areas where there is no photoresist. This is how windows created in the photoresist layer have been transferred on to the silicon dioxide layer.

The photoresist has played its role and it is like a sacrificial layer. This layer will have to be now removed and this is done by again subjecting this silicon wafer to a chemical solution that can remove the photoresist. At the end of the lithography process now you have a silicon dioxide layer with windows in it. This is the silicon wafer through which now you can do further processing that is like diffusion and so on. Let us see how a practical silicon wafer looks like at the end of oxidation and lithography steps.

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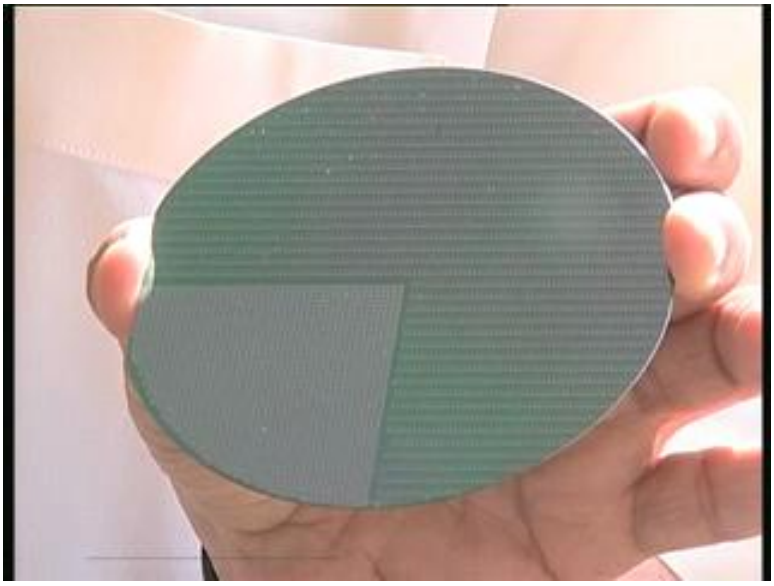

This is 1 by 2 mm thick silicon wafer. Since it is being shown in open air conditions you will find some dust particles sitting on the wafer. These particles are determinal to processing. We had earlier mentioned that we must process the silicon wafers under ultra clean conditions. In the second lecture we had shown a photograph of a clean room where semiconductor processing goes on.

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You can see that the man is in a hood and in the entire room clean conditions are maintained. We can also see the cleaner benches in which the silicon wafer is being handled and processed. This photograph will also help you to appreciate how dust particles can destroy the devices. The green areas on this wafer show silicon dioxide portions, the light grey areas are silicon exposed through the windows in the silicon dioxide. Each small grey area is a device the PN junction. You can see that a dust particle sitting on silicon wafer actually covers a single device or in some cases adjacent devices. The devices underneath the dust particles will not be processed properly and will be defective. Thus a large number of dust particles mean large number of defective devices.

Let us now take a closer look at the silicon wafer. The mirror-like finish of this surface over which the devices are made is evident. You can see the reflection of the pointer on the surface. These are devices of different sizes, these are the devices of the same size but which are bigger. This wafer is been used to study the effect of area on the device characteristics and that is why you have devices of different areas. This is how a wafer will look after oxidation and lithography and it is now ready for diffusion. Having considered the lithography process let us return to our discussion of the device fabrication and see further what process steps are needed to get the PN junction.

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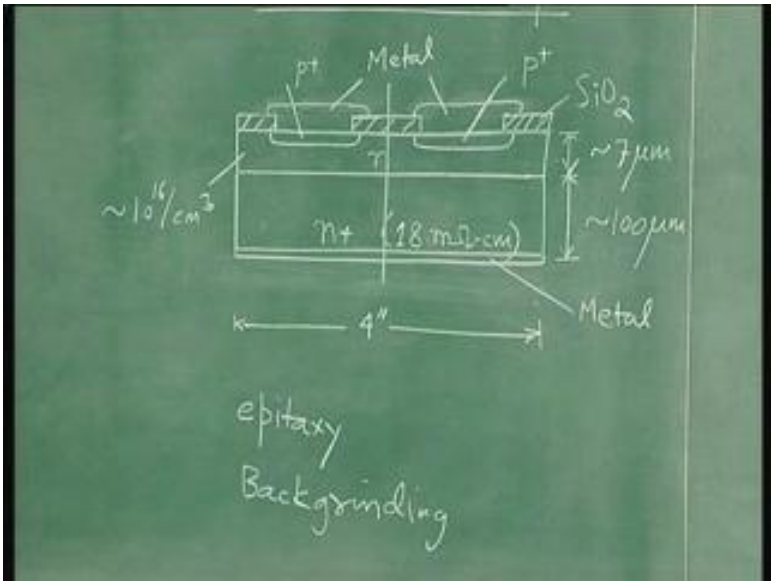

So, returning to this figure where we find Pplus regions are being created through the oxide windows. Now notice here that the oxide prevents the boron from diffusing in these areas. So the oxide is acting like a mask when you do the boron diffusion so that only the selected areas the boron regions are created or the PN junctions are created.

The next step is to metalize this structure. So what you do is you grow a metal layer all over and then by a process of lithography you remove the metal layer in these areas so that finally you end up getting a metal like this only on the PN junction areas. After the metallization on this side you also have to create a metal layer on the back side as an electrode. Before you create the metal layer on the back side what is done is this particular silicon layer which is quite thick which is about 500mu is reduced in thickness because a thick layer means a high series resistance when the current is flowing in this direction.

We need a thick silicon layer to start with because whenever you are doing all the process steps you must able to handle the wafer which is of 4 inch diameter. But after the process steps are almost completed except for the back side metallization not much of handling is required and now the layer can be thin so that the series resistance is reduced. So there is what is called a process of back grinding using this layer is thinned from the back side. At the end of this thinning this layer would be only about 100mu thick. After back grinding a metal layer is deposited all over on this side. So the diode fabrication is almost complete except that all the diodes are joined together on the wafer.

You can see that a large number of such diodes will present on a 4 inch wafer. So although only two diodes are being shown please do not think that this 4 inch wafer contains only two diodes. It depends on the area of the diode. As we have said the area of this diode is almost 1 mm square for the device that we considered so there will be thousands of such devices. This is only a schematic illustration of how devices are

present on the side. The final step is to separate this particular wafer into individual PN junctions and this is done by a process called dicing wherein you cut the wafers at these selected places. Now you have each individual PN junction so this region is what is shown here, this is the single diode chip which is available for packaging.

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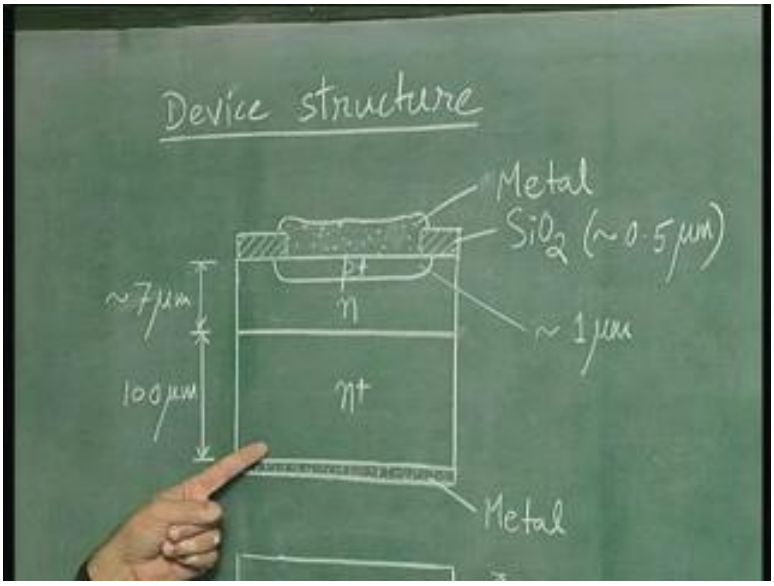

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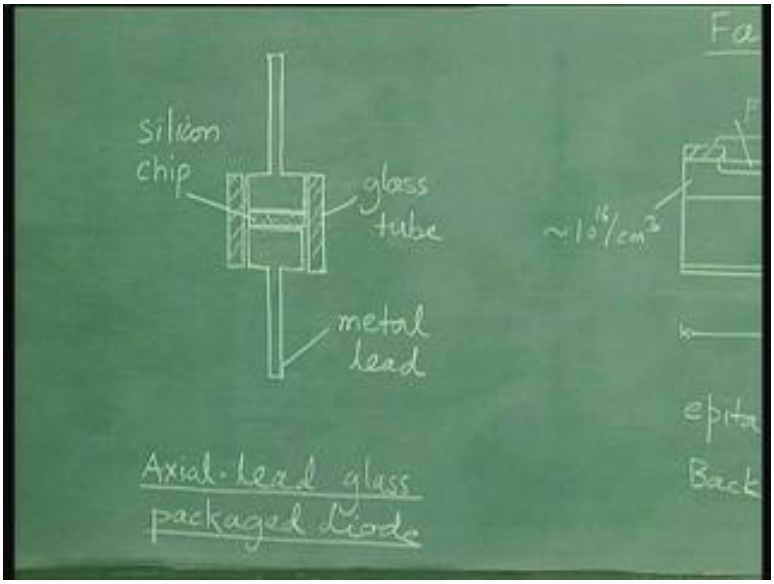

This chip is being put in the package as shown in this diagram. This is the silicon chip and then you have the two leads and the whole thing being put in a glass tube and then sealed so that you have the final package device for use. I must emphasize here that the axial lead glass package is not the only package that is used for encapsulating diodes or

any of the devices. There are many other types of packages also which are available. I have chosen this package for illustration because you would have used diodes in this form of package in your laboratory experiments related to circuits. I would also like to state that in our institute we have developed a technology for fabricating these diodes.

The critical thing in this technology is the growth of the metal layer over the silicon chip. The metal layer has to be grown using a special process and that is the process we have developed, with this we have come to the end of the discussion on structure and fabrication of the PN junction. Let us spend a few minutes on the structure that we will be using for the purpose of analysis. We will be using a simplified version of the real device structure in analysis to avoid complexities. Let us consider the simplifications involved.

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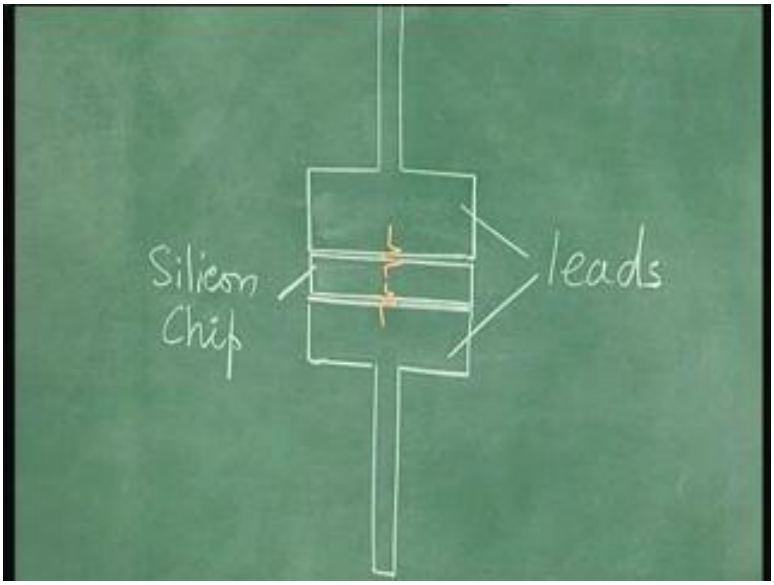

Here what we see is the silicon chip containing the PN junction along the leads that form a part of the package. There will be a contact resistance between the lead and the metallization of the PN junction or the silicon chip here and as well as here. Now we are going to neglect these contact resistances. In other words, we will avoid the effect of the contact between the lead and the chips, this is the first simplification we will be doing.

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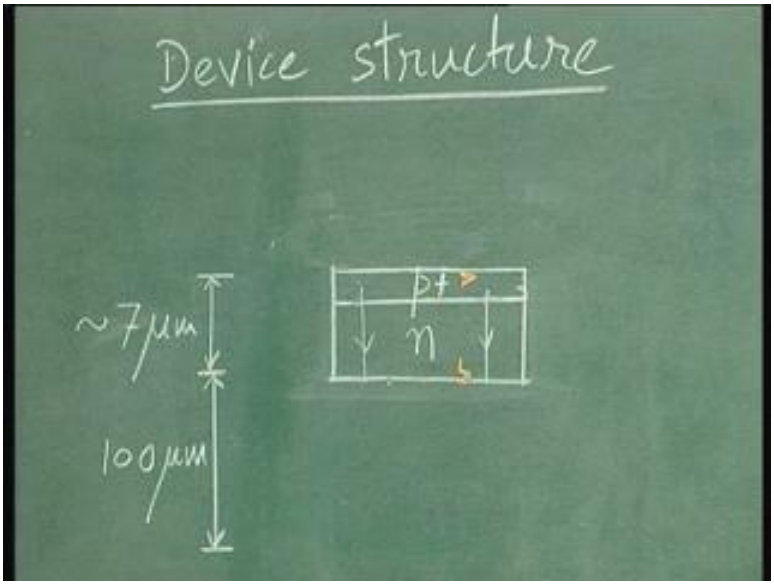

Let us look at the silicon chip itself. What are the simplifications that we are doing here? If you plot the lines of current flow in the device let us assume the device is forward biased then the lines of current flow from P to N region would look like this. They would be vertical in the central portion of the device area but along the edges they will be two dimensional. We would like to avoid the two dimensional areas. What we do is we ignore these portions of the device so that we are now left with the one dimensional situation. The current flow in the device is one dimensional.

The other simplification that we do is simply ignore this Nplus region so this is removed and we assume that the contact is here. Further we will neglect any resistance associated with the contact between the metal and the semiconductor i.e. the resistance here and the resistance here. These resistances which are contact resistances will also be ignored. As a result what happens is therefore we remove these metal regions also. The resulting device therefore will look similar to this which is in a bigger picture.

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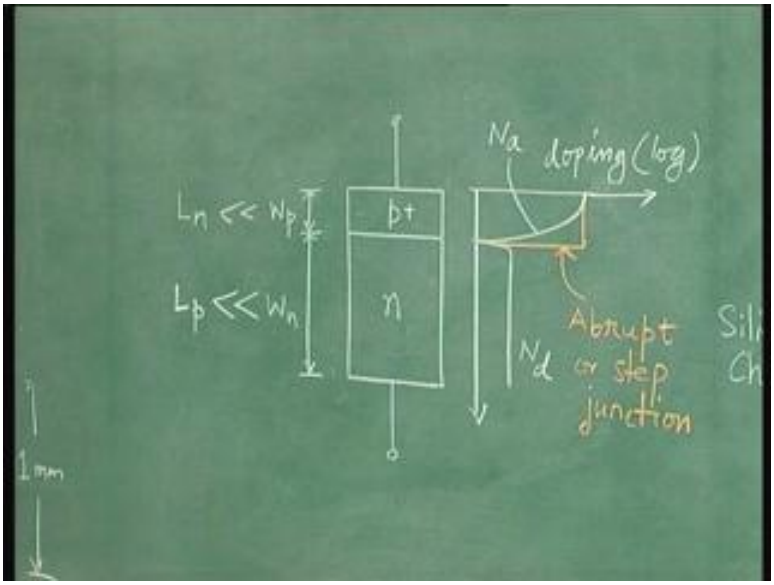

This is the device that is being used for the analysis. This width of the p region called W_p and this width of the n region called W_n we will be assuming that these two regions are sufficiently long. What is the meaning of sufficiently long? It means that W_p is much greater than the minority carrier diffusion length in that region that is the diffusion length of electrons and W_n is also much greater than the minority carrier diffusion length of holes in the N region. When we do the analysis we will understand why this criterion is used.

There is a comparison between the physical length and the diffusion length which is used to decide the length of the regions. So long regions are sufficiently long PN regions imply that these regions are longer than the minority carrier diffusion length in those regions. Further, if you now plot the doping profile in this diode the real doping profile would be something like this. It is to be noted that we are plotting the doping on a log scale. Since you are plotting on a log scale we cannot show the opposite polarities appeared in N regions, we plot only the magnitude. And the shape of the variation of the doping which is caused by diffusion will look something like this on a log scale. So, this is the location of the junction where the net doping is 0.

On a log scale this goes to minus infinity so this is the junction, this is doping $N_{a,}$ p-type doping and this is N_d the n-type doping so the actual doping is non-uniform in the device. But we will assume that the doping is uniform in either region. This means the doping profile assumed will be something like this. So it is uniform doping in the P region as well as uniform doping in the N region. Such an approximation is called step doping or abrupt junction approximation.

The analysis will be based on an abrupt or step junction approximation. This summarizes the structure that will be used for the purpose of analysis. Uniform doped regions, no contact resistances and length of the regions is much greater than the minority carrier

diffusion length in those regions. Now, towards the end of the lecture let us explain in a very simple manner why rectification is achieved using a PN junction or why a PN junction has rectifying current voltage characteristics. This can be easily understood with the help of a diagram here.

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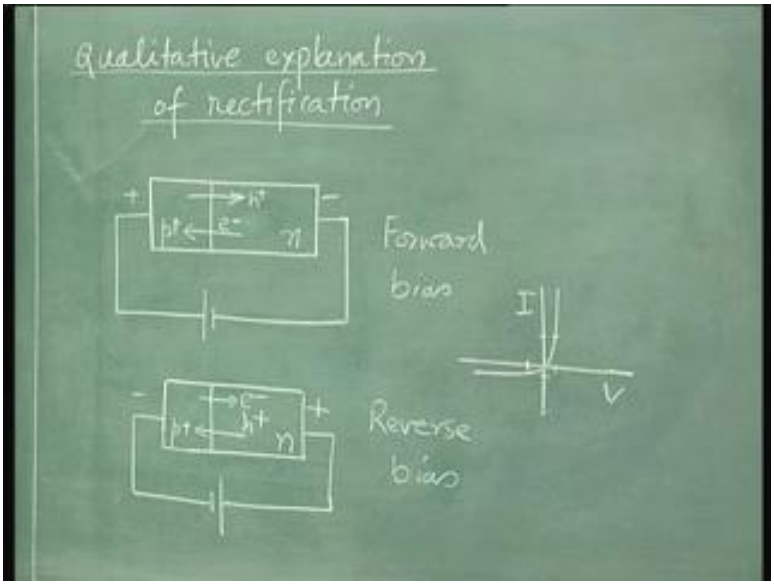

This is a forward bias PN junction. This means the n-type region is negative and the p-type region is positive. Now it is easy to understand that a negative contact will attract holes or positive charges.

On the other hand, the positive contact will attract electrons towards it so it leads to negative charges. The holes are majority carriers in the P region so P region can readily supply the holes which are required by the negative contact. Similarly, the n-type regions has majority electrons and it can supply electrons very easily which are required by the positive contact. Therefore this type of current flow is very easy in a PN junction. So in a forward bias therefore you get a large current. Look at the picture for reverse bias. Now n-type contact is positive and p-type contact is negative. The positive contact attracts electrons but these electrons are minority carriers in the P region. So the P region really cannot supply a large number of electrons.

Similarly, the N region cannot supply holes which will be attracted to the negative contact because holes are minority carriers here. This current will be very small in the reverse direction. This explains why for a given voltage in the forward direction you have a large current whereas in the reverse current you have a very small current. That explains why you have characteristics like this. For any given voltage in the forward direction we have a large current but if this same voltage is taken on the reverse side i.e. on this side you get a small current. That is a very simple explanation of the current voltage characteristic that is the rectifying I_v characteristics of the PN junction.

We will begin the analysis of the PN junction in detail in the next class. Let us quickly summarize what we have done today. Today we have seen the current voltage characteristics of the PN junction that we are going to explain in all the lectures related to this topic. Then we saw in detail how a PN junction is fabricated, what is the real structure of the device. Then we saw what simplified structure is used for analysis. Finally we gave a very simple qualitative explanation for the rectifying nature of the current voltage characteristics of a PN junction.