High Speed Devices and Circuits

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Lecture – 35

HEMT: I–V Characteristics and Transconductance and Optimization

We have been discussing the high electron mobility transistor with AlGaAs/GaAs structure.

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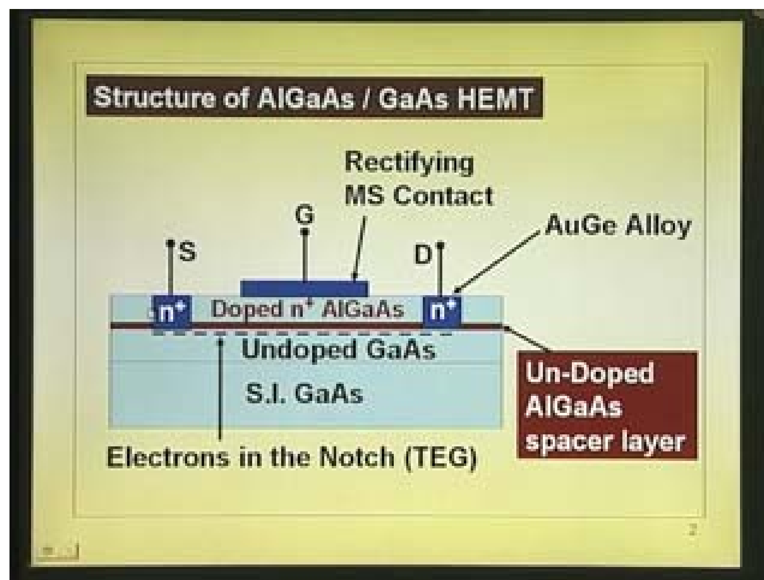

This is the most popular structure because of the ability to have AlGaAs in GaAs. We have gone through the entire physics behind this, how it works, etc. Just like in the case of MOSFET… the structure is almost similar to MOSFET in one sense and in another sense, it is similar to MESFET. You just only take the top layer n plus source contact, n plus drain contact, and doped aluminum gallium arsenide. That is equivalent of the MESFET, but we disable the MESFET here (Refer Slide Time: 02:29) by putting a gate on this, which actually depletes the entire layer. When you deplete that and also, when you have this doped aluminum gallium arsenide on the gallium arsenide, you have got a two-dimensional electron gas here. It is actually these electrons that we are actually using

for current transport and to ensure that this layer (the top layer, heavily doped layer) does not participate in the conduction of any portion of the device operation, you ensure that the entire layer is depleted.

What we have computed also is you have seen that the voltage required to deplete this entire top layer will be V_{bi} minus V_{p0}, which is actually the equivalent of the threshold voltage of this top layer just when it is depleted. Now, because of the presence of the n plus layer on the undoped gallium arsenide, we have this notch layer. We have also said that there are electrons here due to additional band bending in this layer (Refer Slide Time: 03:37). Corresponding to delta E_c by q or delta E_c notch, there are electrons here.

What we are telling is that you can actually remove these electrons in the sense wipe out those electrons from that region by forward biasing this junction, which actually is plus here and minus here. When you apply a total voltage to the gate, which is equal to V_{bi} minus V_{p0}, which will deplete the top layer, if you apply additional negative voltage (which is actually delta E_c by q), this layer will be depleted in the sense that it is just on the verge of conduction.

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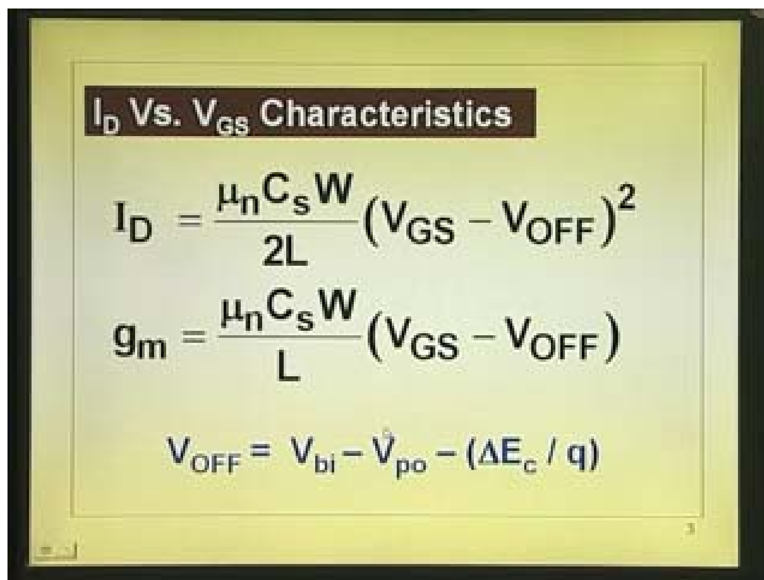

The threshold voltage of that device or the off voltage of the device will be given by V_{bi} minus V_{p0}; please remember that V_{bi} minus V_{p0} by itself has polarity. For example, if V_{bi} is larger than V_{p0}, this is positive. That is what we saw in enhancement type of MESFET. If V_{bi} is less than V_{p0}, this quantity will be negative. So, V_{OFF} will be the negative quantity minus another positive quantity and that is negative.

We can rest assured that if V_{bi} minus V_{p0} is negative, you have a device with V_{OFF} that is equivalent of the threshold voltage, which is negative, and that means it is depletion type of device. Now, you can make this as enhancement type of device by making this quantity positive (Refer Slide Time: 05:04). It is more positive than delta E_c by q. How do you make this more positive? We make it more positive by making this less, V_{p0} less. Making the AlGaAs layer thinner, we can actually make this layer more positive. The entire theme of the device (Refer Slide Time: 05:27) is we can have depletion type of device or enhancement type of device. The operation of the device is similar to MOSFET and we can see the difference.

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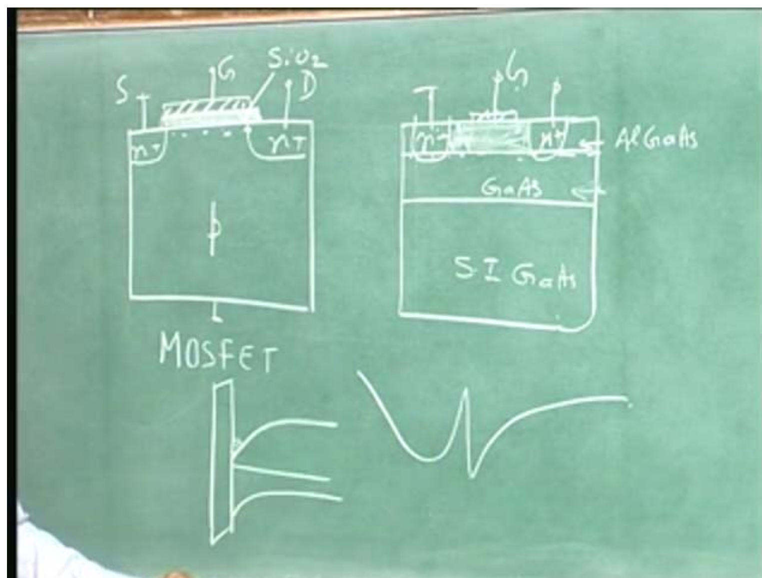

In the case of MOSFET, p channel, p type substrate, n plus source, n plus drain, between the gate and the substrate, what do you have? You have SiO_2; an insulating layer with $epsilon_r$ equal to 4. In the case of HEMT, what do you have? You have a semi-insulating

gallium arsenide, I am referring to gallium arsenide because this is the device that we are talking of right now, then, undoped gallium arsenide and on top of it, you have got this AlGaAs. What you have now is a doped layer and undoped layer that I have already put there. In fact, this will give rise to the two-dimensional gas; we have already been discussing that diagram.

We have this n plus here, we have this n plus here and we have the gate here (Refer Slide Time: 06:51). I can call this as the gate in the case of MOSFET and this is the gate in the case of MESFET. The difference is that this is metal oxide semiconductor and this is metal semiconductor contact, a Schottky barrier but you ensure that the thickness (Refer Slide Time: 07:11) is such that the built-in potential itself will deplete the whole thing; so you do not want this to conduct. Now, when I apply a voltage between the gate and the source, this is depleted and so, this entire layer is equivalent of that and this layer can be made (Refer Slide Time: 07:37) micron or even smaller. This layer can also be made 300–400 angstroms, very thin. This is actually almost equivalent of this or is exactly equivalent of that.

We have got a notch here, I have discussed earlier. Recall a p–channel thing. That is the oxide and then we have the Fermi level. We have got the band bending taking place. That is where the electrons (Refer Slide Time: 08:10). That is the electrons here (Refer Slide Time: 08:14), inversion layer. The threshold voltage is the voltage at which band bending is such that this becomes n type completely. Here, what we have is similar notch conduction band. I am plotting only this one here, that is, the conduction band notch. From there onwards, what is this? This is the depleted layer there (Refer Slide Time: 08:41).

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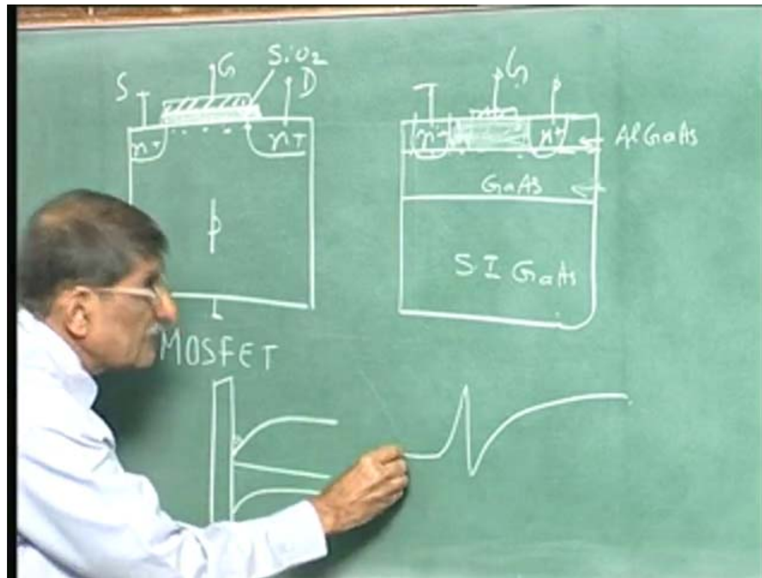

If it is not depleted, it will go like that, thin depletion layer.

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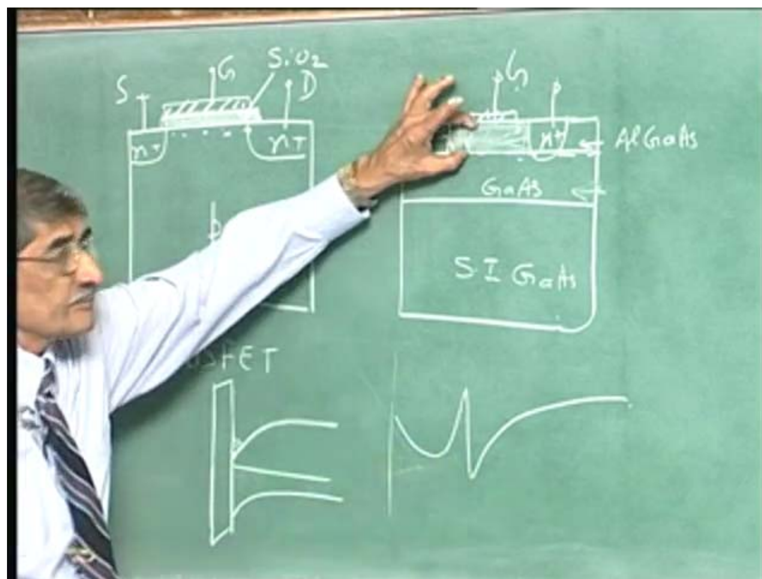

But when we apply a voltage, it will go like that. So, the entire layer is depleted here. Here, it is oxide (Refer Slide Time: 08:55). So, replace this with that. I showed it thicker here just to enable me to draw this diagram. This can be thick or as thin or even thinner than that. Between the two insulating layers here, this has epsilon$_r$ equal to 4 (Refer Slide

Time: 09:11) and this has $epsilon_r$ equal to about 12.8. For the same thickness, this will have larger capacitance, which would mean that the coupling between the gate and the channel will be better. For a given voltage change here (Refer Slide Time: 09:30), the charge that will be here will be more.

q is equal to c into V. For a given V, if c is large, q is large. That is what is happening here, better coupling here; that too, we can have better current and better transconductance. For a given delta V, delta q will be more because capacitance is large. If delta q is more, transconductance will be more. delta q by delta t is the current. If delta q by delta t is large, the current is large or g_m is large. So, this device will have better transconductance compared to that; so, one-to-one correspondence here. If one-to-one correspondence is here, this device will behave similar to a MOSFET with regard to I-V characteristics. I do not have to derive that. It is equivalent of the inversion layer. When I apply V_{DS} here, the inversion layer will start beginning to disappear at this end here. Similarly, when I apply V_{DS} here, it is equivalent of applying negative voltage to that. So, the charge will be reducing here.

In the same way, you can derive the I-V characteristics of this MESFET, exactly similar to the MOSFET. All that you will have will be the MOSFET equation with C_{oxide} replaced by this C_S, threshold voltage replaced by threshold voltage of this device, which we call it as off voltage and mobility replaced by mobility of this two-dimensional electron gas, which will be tremendously large compared to that. It will go down to lower temperatures, which can be as high as 10 to the power 5 or more centimeter square per Volt-second, whereas this will be just suffering from the lattice scattering as well as scattering from the impurity scattering. Impurity scattering is absent here and that is a benefit of this device. With one shot, we can write down the equation of the MOSFET adapted to this particular condition and that is the equation that you see here (Refer Slide Time: 11:36).

What we have written is the equation of MOSFET exactly, because it is replaced oxide with the depleted AlGaAs layer and the channel inversion layer is replaced by the two-dimensional electron gas, mobility by mobility of this electron gas, which is high and C_S

is actually $epsilon_r$ $epsilon_0$ by thickness of that layer. Now, notice your bargain for thinner layers. Why do we ask for thinner layer? C_S will be larger. If the C_S is larger for a given change in voltage, I_D will be large, change in I_D will be large, which means g_m will be large. We look forward to devices that have large g_m, because the figure of merit of a device, any device for that matter, is g_m by c. If g_m is large, the Ft will be large, cut-off frequency will be large, so V_{GS} minus V_{OFF} whole square (Refer Slide Time: 12.36) device. I do not know why they started putting this as V_{OFF}. That is because usually, it was depletion type of device, but we have seen just now that we can make this as enhancement by making the V_{OFF} positive by reducing the pinch-off voltage; delta I_D by delta V_{GS} is actually this quantity g_m.

Compared to the MOSFET, we can see that even at room temperature, this factor for MOS, n–channel MOSFET of a 1,000 mobility all in centimeter square per Volt-second and this will be close to about 10,000, in the range of 8500 to 9000, very high. This is a factor of about 8 to 9, that is, 8 and this is larger for the same thickness by a factor of at least 4 and 12.8, about 3. (Refer Slide Time: 13:36) 25 to 30 times larger transconductance and mobility, which is fantastic. We also argued out in the previous case of MESFET when you go to higher and higher electric fields, the mobility will degrade (Refer Slide Time: 13:56) but then, you write everything in terms of velocity and then you can get the velocity overshoot benefits, which are very large. In this connection, I would also like to mention that suppose I go to very high fields, we get velocity overshoot effect and we get the transfer of electrons from the lower value to upper value. Suppose we have very high field, the field is high but voltage is small.

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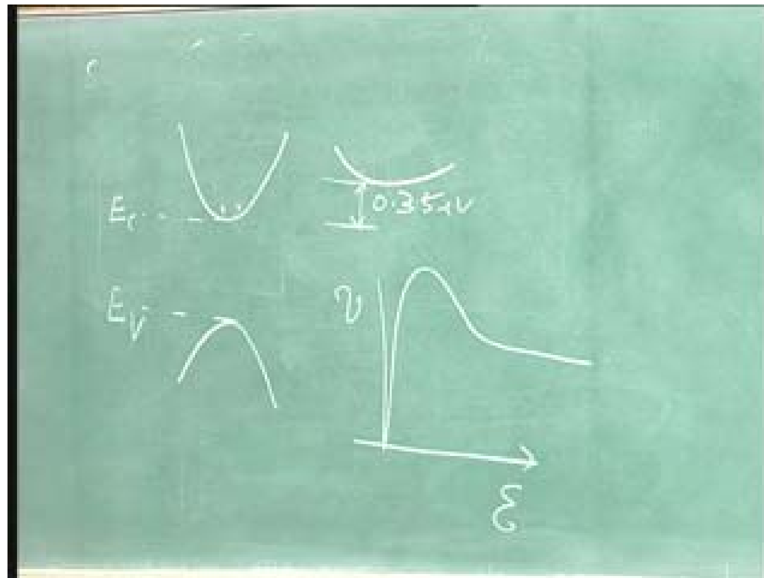

I have a diagram like this; I would like you to spend some time and think about this. The conduction band is here, valence band is here and the electrons are there. This will be the gallium arsenide high electron mobility gas which is located here, undoped, but there is a (Refer Slide Time: 14.55) value here. This gap is something like 0.31 or 0.35, 0.36. In fact, people quote different values there depending on (Refer Slide Time: 15:11) this value or other values – 0.35. I see different values quoted for that. Definitely, it is about 0.3 or 0.35. The value that I have given was around this value.

Suppose you have these channel electrons and the velocity (Refer Slide Time: 15:37) characteristic is like this. It goes up like that. (Refer Slide Time: 15:46) to Schottky channels, you will have velocity (Refer Slide Time: 15:49) improve that we will be happy. So, because of this, you get velocity (Refer Slide Time: 15:55) in excess of 4 into 10 to the power of 7 centimeter per second. Now, what I am trying to point out is this entire process of negative differential mobility dV divided by dE is negative and that is called negative differential mobility.

This region occurs because electrons are transferred from here to here. You can acquire a high field if the channel length is very small and the voltage is less than 0.35 electron Volt. Suppose you have a voltage 0.3 V, what is the energy of the electron? q into V is

energy. If voltage is 0.3 Volts, the energy is 0.3 electron Volts. The electron has no chance to go into that layer. Now, you can see the beauty of the whole thing. You have an electron residing here and you have electrons that cannot acquire energy to go up to that point and you have electrons that experience very high field. That means we are on this line (Refer Slide Time: 17:11).

On this line, your velocity can be much higher, but still, you do not have it. What happens is the electron (Refer Slide Time: 17:24) lower valley and the entire transport takes place in the lower valley itself. Virtually, people talk of the transport of the electrons without intra-valley scattering; this is called intra-valley scattering. Once scattering phenomenon is cut down, that reduction is cut down. It is very high mobility right through, all the way. V will be mu into E; that is all; that will be the type of (Refer Slide Time: 17:53).

(Refer Slide Time: 17:56) You can get very high velocities in the (Refer Slide Time: 17:59) region. In fact, people even tend to call it as ballistic transport. Ballistic transport is actually the transport where there are no collisions, but there are collisions, that is, scattering is there and that is what governs the mobility, but we do not have the intra-valley collision or scattering. I just wanted to point out this to you that when you go to very short channels, if the voltage is low, you can still have high fields and high velocities because the electron remains in the lower valley itself.

Put some number 0.3 Volts applied across the channel, the channel length is 0.3 microns, the field is 10 to the power 4 Volt per centimeter. The field is 10 to the power of 4. If we talk of the entire static characteristics here, you will think that is the velocity. 10 to the power of 4 is 10 kV per centimeter, somewhere there (Refer Slide Time: 19:09), this is 3 kV per centimeter. But you are not going to that curve, you are still remaining in this portion of the curve. (Refer Slide Time: 19:17) by the slope (Refer Slide Time: 19:19) the velocity because the electrons do not have energy. This is the irony of the whole thing. In devices that have 0.3 microns and 0.3 Volts, you will have high fields and high velocities because there is no intra-valley scattering. Even if you have channel length of 1 micron,

you get… just about here (Refer Slide Time: 19:46). This is just incidental. Now, let me just move on further with some of the discussions related to this AlGaAs HEMT.

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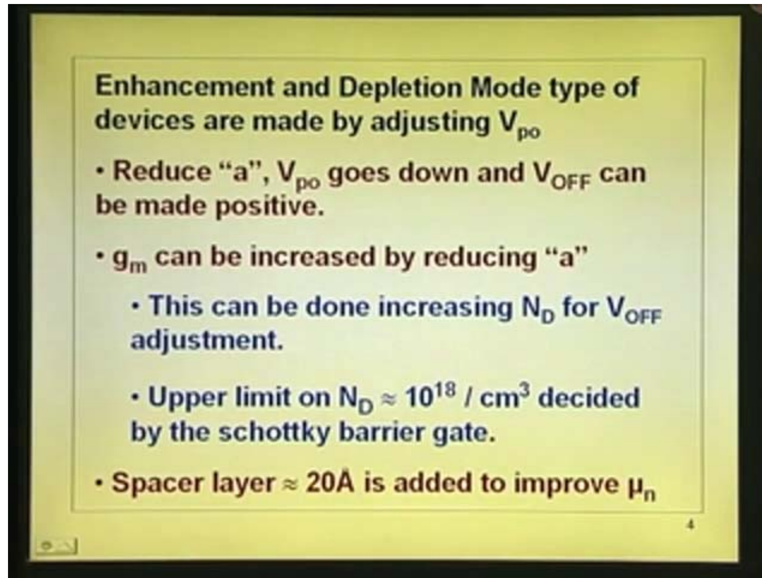

We will just go through whatever we have been saying. Enhancement and depletion mode type of devises are made by adjusting V_{p0}. Since off voltage is V_{bi} minus V_{p0}, I can reduce the V_{p0} by reducing a and V_{OFF} can be made positive. Let us go to this equation (Refer Slide Time: 20:20). Reduce V_{p0} because V_{p0} is nothing but q N_D a square by twice $epsilon_r$ $epsilon_0$. I reduce a, V_{p0} reduces, square of a. g_m can be increased…. Go back to the equation again (Refer Slide Time: 20:40).

g_m can be increased by increasing capacitance, better coupling and capacitance can be increased by reducing the thickness of the insulating layer that is present between the gate and the channel. g_m can be increased by reducing a. Once you fix your threshold voltage or off voltage by fixing V_{p0}, if you reduce a, V_{p0} will fall, but if you want to bring back the V_{p0}, you must increase the doping. This can be done by increasing N_D for V_{OFF} adjustment. I hope that statement is clear. Reduce a to get better transconductance, but you cannot get greedy and go on reducing E, because then, you have to accompany by increasing doping but there is an upper limit on doping. The upper limit of the doping is…. What is the upper limit? Schottky barrier diode. After all, it is this doping we are

talking of (Refer Slide Time: 21:45). Reduce this thickness but you must increase the doping so as to keep the pinch-off voltage the same, but the upper limit is the Schottky barrier. If you go to a doping concentration of 10 to the power of 19, you will not have a Schottky barrier, you will have a bad Schottky barrier, leaky diode and closed Ohmic contact.

The upper limit comes up by the doping concentration there. We are stuck up with that and we are stuck with a certain layer thickness. So, the g_m upper limit is there because of that. Of course, you can always play with the velocity overshoot effect and like very short channel length and very high fields to get high velocities and better transconductance. The spacer layer is…. let me go back to the diagram once more (Refer Slide Time: 22:44).

The top layer is doped and this layer is the spacer layer. We have put that layer there because we do not want this two-dimensional electron gas to suffer from the scattering. We do not want them anywhere near these impurity atoms. Put a spacer layer and it spatially separates the donors physically from these ions. There is absolutely no contact, no Coulombic force of attraction and no scattering because of that (Refer Slide Time: 23:25)

You cannot make this (Refer Slide Time: 23:27). People have seen that if you make it thicker, it is better. Why? If we make it thicker, there is less chance of these electrons coming under the effect of the dopants. So, we would like to make it thick, but the moment we make it thick, the total layer thickness, insulating layer thickness becomes more. If it becomes more, C_S falls and transconductance falls. That is an optimization there. If you find that 20 angstroms is what you would prefer and if you are grudging, you can say I want 30 or 40 angstroms; 20 angstroms improves the mobility quite a bit and that is what we have put.

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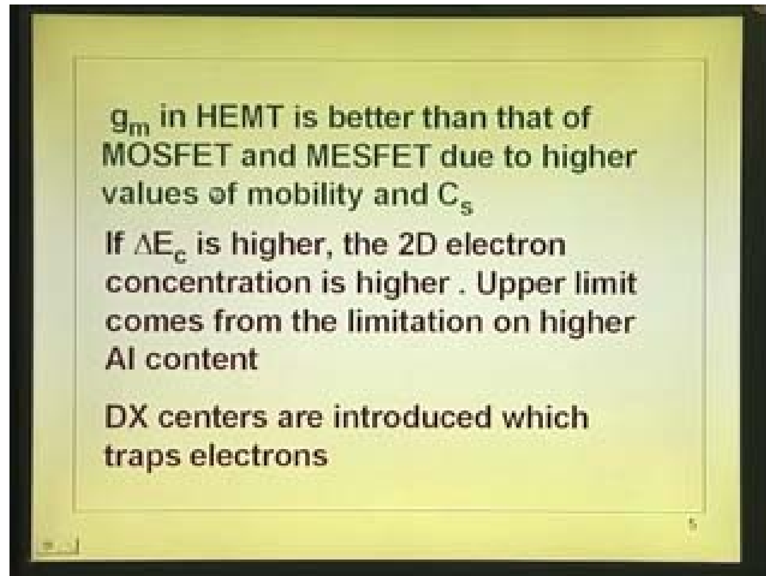


This is what we have said already: g_m in HEMT is much better than that of MOSFET because the mobility is 8 to 9 times larger and C_S is at least 3 times larger; at least 25 times better g_m compared to MOSFET. Even when we have velocity overshoot, short channel length effects, because of velocity overshoot effects and virtual transport without intra-valley scattering, we get much better performance, much better g_m with HEMT.

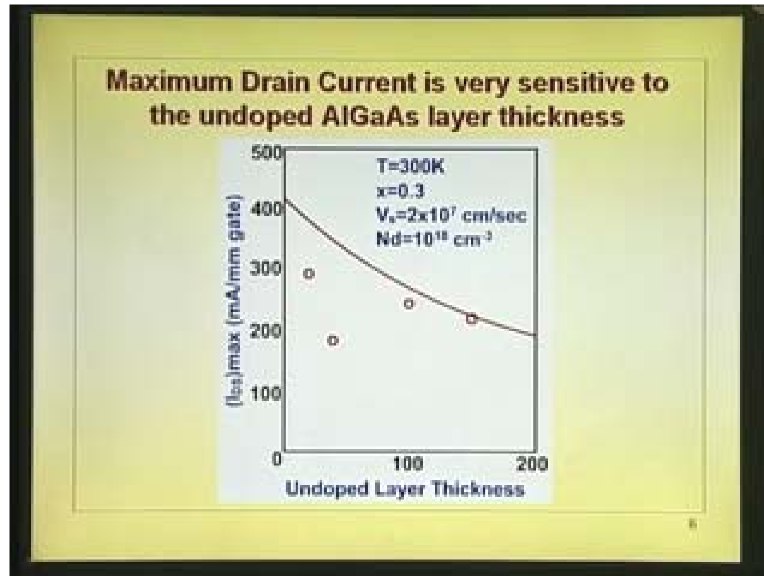
The other thing that we have been telling is delta E_c. We have taken the case where this x is about 0.4 or so and delta E_c is about 0.32 corresponding to that. Higher the delta E_c, better is the ability to notch the electrons. You have got a well that is deeper and you can connect more electrons there because after all if you remember, the band bending of the slightly doped region is equal to the built-in potential of the homojunction plus delta E_c by q. If delta E_c is higher, more is the band bending. If more is the band bending, more will be the electrons. That is what is implied here – the 2D electron concentration is higher if delta E_c is higher.

From that point of view, we would like to have a device that has got higher delta E_c but there is an upper limit for delta E_c in the AlGaAs/GaAs system. What does delta E_c depend upon? delta E_c depends upon x, the mole fraction of aluminum. Higher this aluminum concentration, higher will be delta E_c. Virtually, 0.6 is (Refer Slide time:

26:22) E_{g1} minus E_{g2}. E_{g1} is the band gap of AlGaAs and that is higher if the mole fraction is higher, but there is an upper limit because higher aluminum content introduces some trap levels, which actually affects the total performance of the device. Trap levels will be present in that layer and they seem to trap some of these electrons without releasing them to the channel itself. The electrons are trapped there and are not available for (Refer Slide Time: 26:55) the channel. Even if you increase, there is no benefit (Refer Slide Time: 27:00). You may say that you will still tolerate with that thing but it gives rise to poor performance at lower temperatures, because more trapping takes place.

The second one is it is difficult to make Ohmic contact on wider band gap materials. We have put another material on AlGaAs, which has a lower band gap to make the source–drain contact; the source–drain contact is Ohmic contact. It is always difficult to make Ohmic contact on wider band gap semiconductors. I think we have understood that long time back, because if it is a wider band gap material, the (Refer Slide Time: 27:41) will be two-thirds of that if it is… (Refer Slide Time: 27:44). That way, you can understand; it is easy to understand that; if you have higher (Refer Slide Time: 27:52), it will be difficult to make Ohmic contact. The technology suffers from this difficulty. The technologists put their hands up and will immediately say there is an upper limit and added to that, there is a performance limitation because of the center called DX center. I do not know why they call it DX center (Refer Slide Time: 28:14). There are usually funny ways of naming some of these devices and some of the behaviors. This is the DX center. trap (Refer Slide Time: 28:28)

(Refer Slide Time 28:30)



They usually limit the upper limit of that to about 0.3, that is, the x of about 0.3, not even goes to 0.4, which will be giving you delta less than 0.3 electron Volt. Now, about the spacer layer, undoped layer thickness. These are some of the experimental points (Refer Slide Time: 28:56). I think Illinois University has made these measurements. This is the maximum current that you can get as the spacer layer thickness is varied. It is understandable; I_D is proportional to C_S; if spacer layer is thicker, C_S slope falls, I_D falls. I_D is the maximum current means when the band bending is maximum.

If I forward bias the diode junction, the band bending in the gallium arsenide layer reduces. We can remove all the electrons that go (Refer Slide Time: 29:34) off state. If it is fully on, the device is fully on, maximum current that you can get is this – about 300; that is what they have seen. This is of course some theoretical computation that they have made (Refer Slide Time: 29:47) but they have seen this. But of course, they do claim that these are not the final and there may be many more points filled up here. This particular (Refer Slide Time: 29:58) these are values that are there and some more points might have been fitted into that, but the truth is that thinner is better. So, they use about 20 angstroms so that we get the best result.

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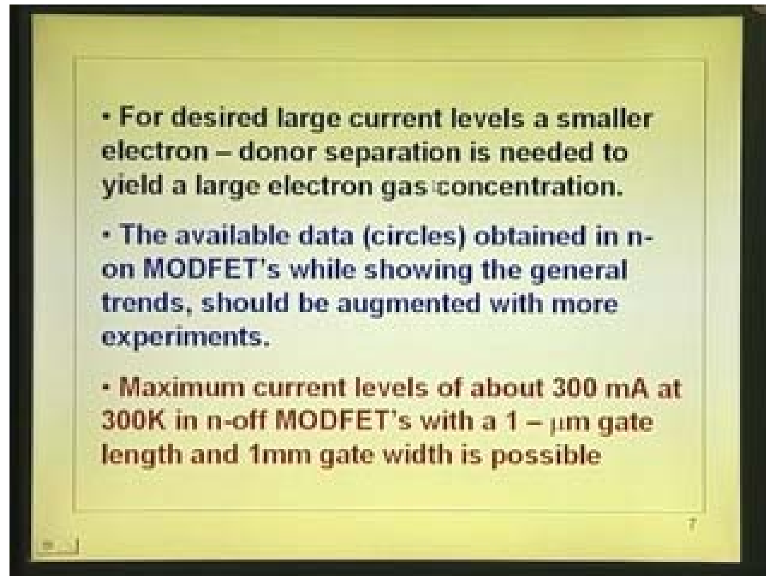

This is summing up what we have said now. For desired large current levels, a smaller electron–donor separation, that is, a spacer layer is needed. Reduce the spacer layer or the setback layer, both (Refer Slide Time: 30:31) names are there, to better get electron concentration. I am repeating what is there in this diagram (Refer Slide Time: 30:37) in the form of words. Available data (Refer Slide Time: 30:41)…. some results (Refer Slide Time: 30:43) more points are required, it is better.

Maximum current levels of about 300 milliamperes at 300 K in MODFET with a 1 micron gate and 1 millimeter gate width has been observed. This is actually what is reported for an AlGaAs/GaAs system. You can get better if you can have a material that has better delta E_c. You have to switch over from gallium arsenide based material may be (Refer Slide Time: 31:12 min) based materials. We will see later at least some of examples of that and what is the impact of phosphide based devices; we will see that a little later.

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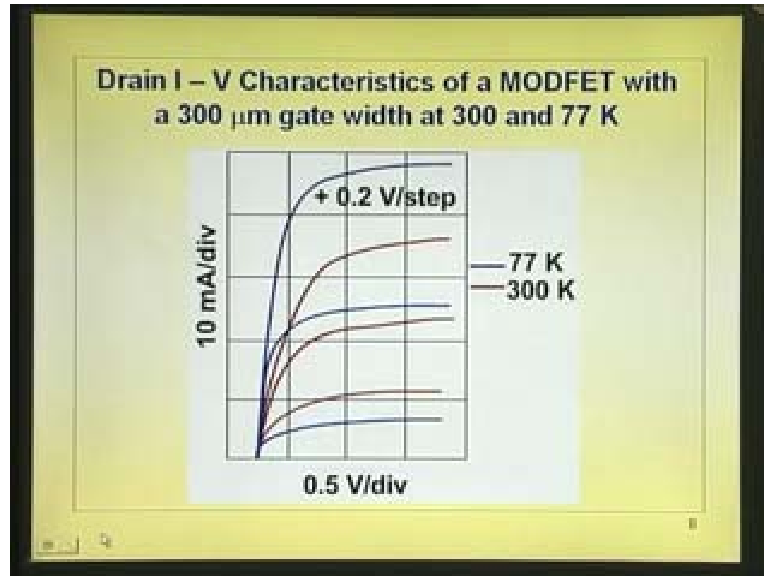
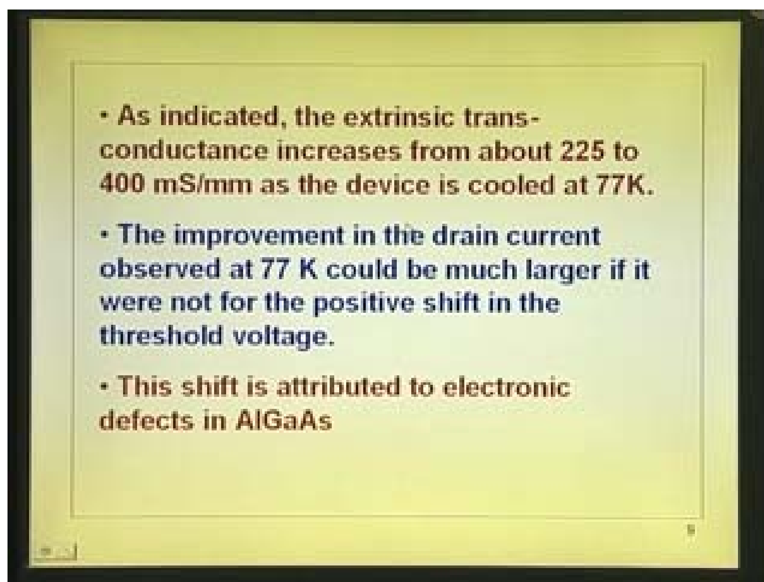


This is actually to show that this is the reality – it is a reality device that has been made and tested. At room temperature, these are the curves: 1, 2, 3 curves (Refer Slide Time: 31:34); they are at room temperature, the red curves. The blue ones 1, 2, and 3 are at 77 degree Kelvin. The X axis is 10 milliamperes per division 10, 20, 30, 40, 50 milliamperes. The Y axis is 0.5 Volts per division: 0.5, 1, 1.5, and so on; that is V_{DS}. This is I_D (Refer Slide Time: 32:09), it is understood that drain I–V characteristics (Refer Slide Time: 32:12) there, drain current versus drain voltage. These are the output characteristics of the device as V_{GS} is varied – the gate voltage V_{g1}, V_{g2}, V_{g3} in steps of 0.2 Volts per division. If this is 0.2, 0.4, 0.6 Volts; for two temperatures, it is given. I would like you to observe this characteristic carefully. There are two things to observe.

One is the spacing between the two curves is more. For 0.2 Volt, the spacing is that much there, which is almost about two divisions – that is about 20 milliamperes, almost in that range, whereas if you take these two curves for the same voltage difference of 0.2 Volts, it is slightly more than one division. It is not double the current, but almost double. What we are telling is that the change in current in the case of 77 degree Kelvin is more than the change in current for the same change in voltage at 300 degree Kelvin. What is the reason? The reason is what we have been telling all along – mobility is higher at lower temperature. Mobility at room temperature may be something like 8500, best and at 77, it

is 100,000 centimeter square per Volt-second. Tremendous improvement is there – 10 to the power 5; that is about the range that people talk of. We will get much better performance, but this will have combined effect of mobility and also when we go to higher field here, (Refer Slide Time: 34:02), we are talking of 1 micron channel length, you have velocity overshoot effects, you will not get the full benefit of mobility. You do not get that complete factor as much as you expect, 25, but you get a much higher (Refer Slide Time: 34:16).

(Refer Slide Time: 34:22)



We will just go to the next slide and see the values. The extrinsic transconductance at 77 degrees Kelvin is about 400 milli-Siemens per millimeter. Per millimeter is implying gate width or channel width is 1 millimeter. Milli-Siemens is milliampere per Volt. At room temperature, it is 225 milli-Siemens per millimeter. It is a tremendous benefit that we get, which will tell you that the cut-off frequency (Refer Slide Time: 34:53) will be much higher. The improvement in the drain current…. One more thing I want you to notice here, which I have not listed down in the slide, is notice the characteristics at this portion (Refer Slide Time: 35:10). I will just go to the board and put that out so that it becomes much more clearer.

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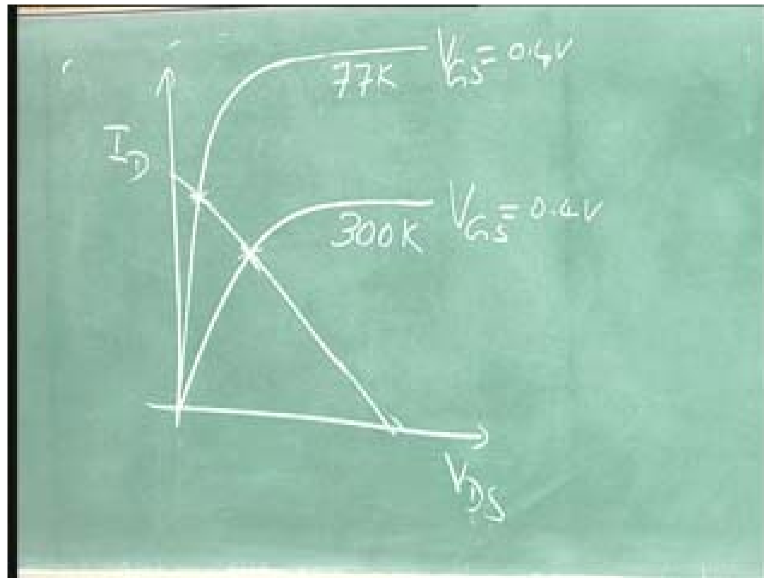

I will plot one characteristic: V_{DS} versus I_D. To avoid confusion, I will plot one characteristic. At room temperature, we have this characteristic for V_{GS} is equal to say 0.d Volts; for same V_{GS}, no doubt you get higher current but you also get that sort of characteristic (Refer Slide Time: 36:01). This is V_{GS} equal to 0.4 Volts. What I mean is whatever is V_{GS} minus V threshold, some value I am putting arbitrarily. This is at 300 degree Kelvin and this is at 77 degree Kelvin; we can see the benefit here.

Not merely better transconductance but you also get smaller on resistance. For digital circuits, it is really required – we want to have smaller on resistance. Just see here, if I put a load resistance like this, you will end up for the same gate voltage here (Refer Slide Time: 37:04) in the on state, whereas here, you will end up here (Refer Slide Time: 37:08). This is the drop in the on state and this is a much lower drop – (Refer Slide Time: 37:15) dissipation will be smaller and the frequency response of the circuit will be much better because charging times are all smaller because resistances are smaller – on resistances.

In the first one or two lectures we discussed, the theme of these high speed devices is to go to smaller capacitances and stronger resistances. We have achieved that here, but of course, you have to put up with going down to lower temperatures. This is one key thing

for these high electron mobility transistors: apart from better transconductance, lower on resistance.

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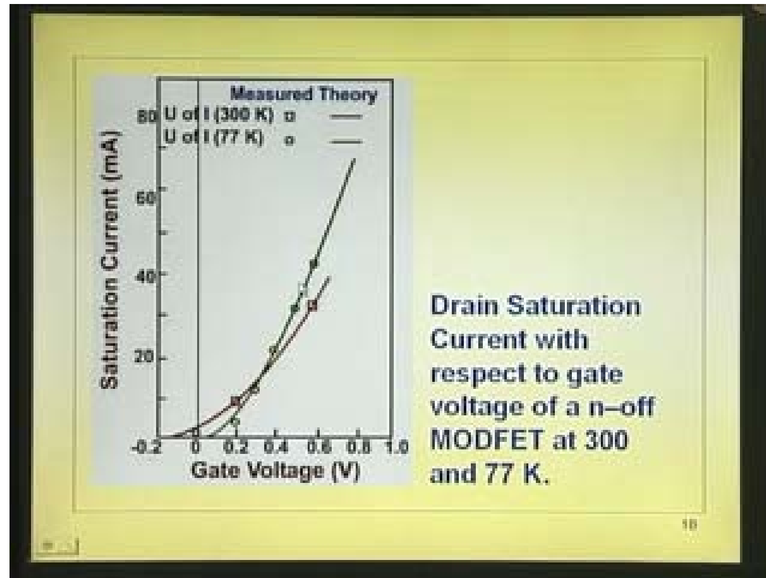
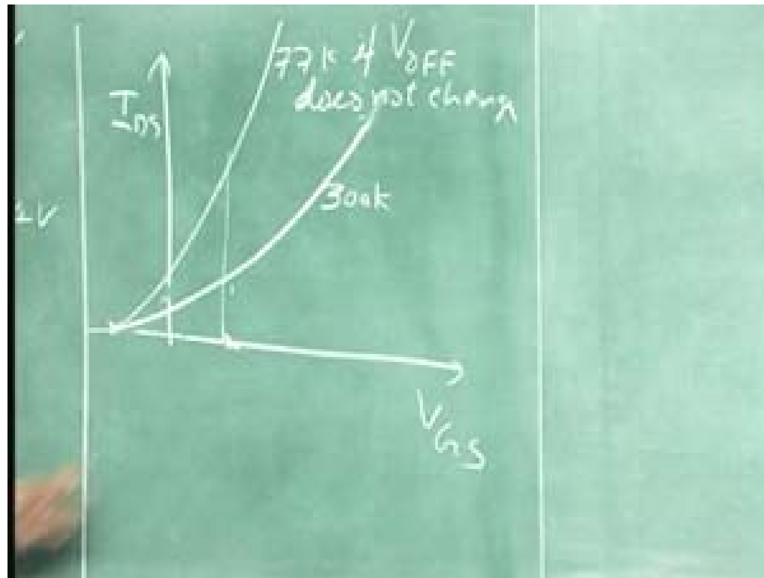


One more thing that we have noticed here is if you go to next slide, we will see that there is a shift in the threshold voltage. These are transfer characteristics. What was shown there was the output characteristic. These are the real devices people have measured. We can see this curve, the red curve is usually transfer characteristics: I_{DS} versus V_{GS} at 300 degree Kelvin. This curve (Refer Slide Time: 38:38) will show at 77 degree Kelvin.

You have to observe two things. One is this is steeply increasing, indicating for a given voltage, current is larger, g_m is larger because mobility is larger. The other thing is that there is a shift in threshold voltage to the positive side. The shift in threshold voltage is because of some of the trapping of the electrons in the AlGaAs layer at lower temperature and slight amount of carrier freezing also takes place in AlGaAs. The improvement in drain current observed could be much larger. See what I am saying is if this threshold value remained there, same value, when you apply a gate voltage, if we shift this entire curve there….

(Refer Slide Time: 39:49)

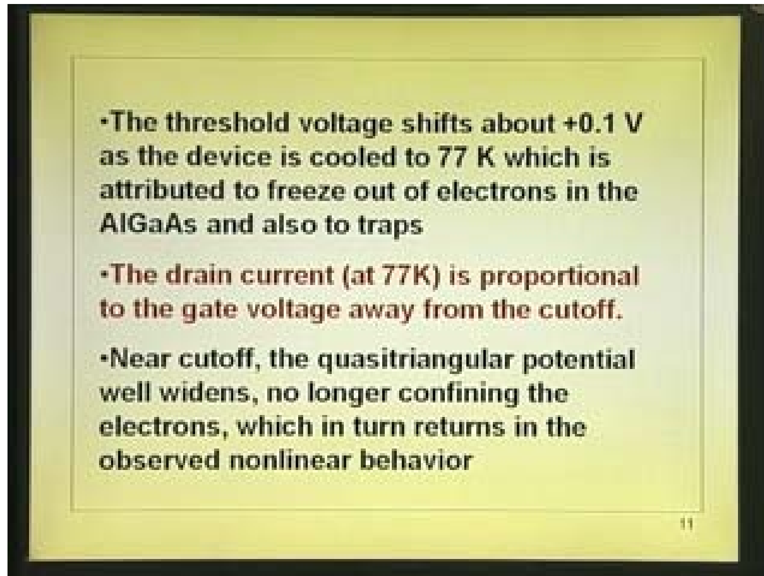


Suppose I take V_{GS} versus I_D saturation. In the first curve, we have got like that; let me just put it slightly differently. If I have got, that is square law. If the threshold voltage remained the same, you would have got it like this (Refer Slide Time: 10:11), because for the same change in the gate voltage, the current is much more. V_{GS} minus the threshold into the mobility, V_{GS} minus $V_{threshold}$ square into mobility, all other terms. Mobility is better, so, V_{GS} minus $V_{threshold}$ remains same and I would have got better current. But what happens is that the threshold voltage…. This is at 300 K and this is at 77 degree Kelvin if V_{OFF} does not change. If it does not change, that is what you will get. That is the meaning of that particular term that we have put there.

But in practice, when you go to lower temperature, you do not have all those electrons available, because some of them are trapped (Refer Slide Time: 41:27) in the AlGaAs or (Refer Slide Time: 41:30) also you can say (Refer Slide Time: 41:31) shifted down here so that will go like that. What is mentioned here is you would have got better current there if the threshold voltage had not changed, because it has become positive. The current is only (Refer Slide Time: 41.48) changing; that is the meaning of that here. There is some portion where it is even lower, but when you go to some other portion…. In fact, it is better to take a look at this real curve that they have given (Refer Slide Time: 42:00). At this point, if you see, the current is smaller because the threshold voltage has

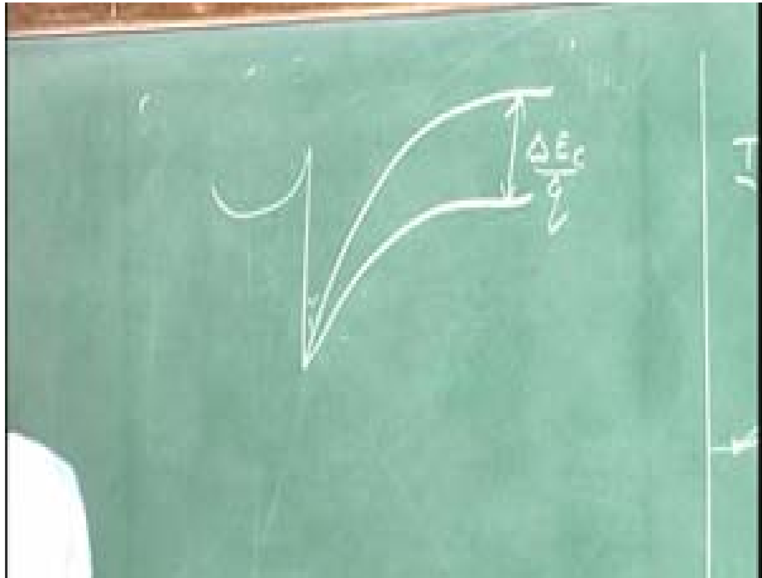
shifted to the right because of the non-availability of the electrons there. These are some of the things that people have observed and seen (Refer Slide Time: 42:19) that the high electron mobility transistor is not a myth, it is a reality; way back, they have realized it.

(Refer Slide Time 42:25)



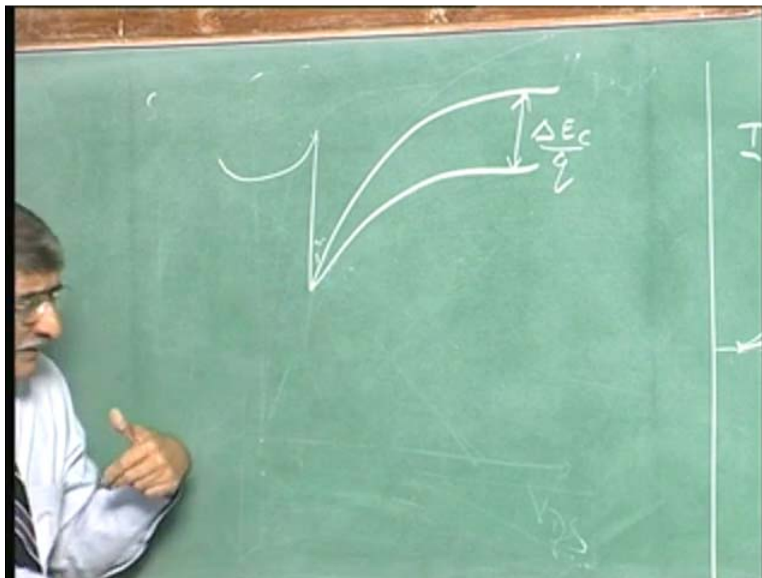
The other thing we can see is the threshold voltage shift is not only due to the defects, it is also due to some carrier freeze-out in the AlGaAs layer. The carriers have frozen out; they are not available for transfer onto the two-dimensional gas. The drain current is proportional to gate voltage away from the cutoff. Near the cutoff (Refer Slide Time: 43:00), actually, if the well widens and we get… you get much (Refer Slide Time: 43:06). The meaning of the statement there is you get the regular (Refer Slide Time: 43:09) characteristic, but here, we have got much more non-linearity, because as we go near the off state, what happens?

(Refer Slide Time: 43:29)



You have got that layer like this; that is the fully on state. This is a perfect quantum well that confines these electrons, but as we go to the off state, what happens? This is brought down (Refer Slide Time: 43:43) forward voltage. This is on fully and this is the off state.

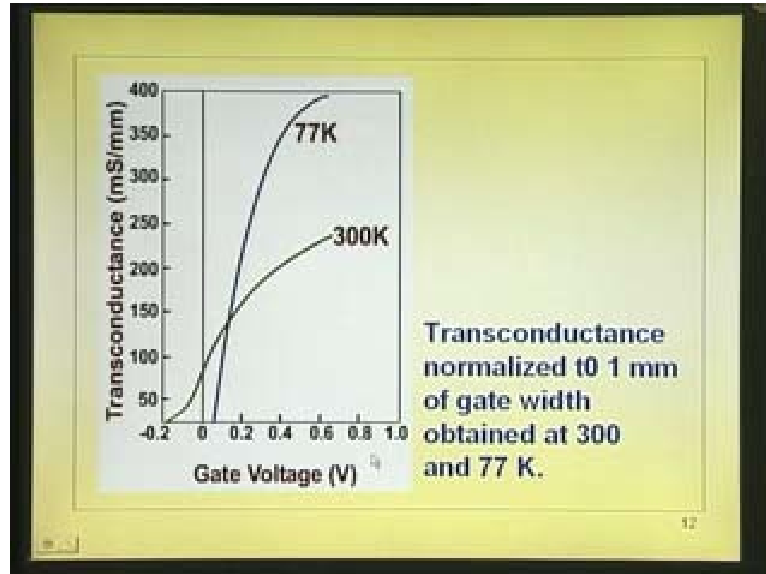
(Refer Slide Time: 44:00)



It is brought down by an amount… Let me draw it slightly better. Off state is this. This is delta E_c by q. This is spread out here. The confinement is not good as in this case; they

are spread out there. That is why a deviation from the regular characteristic comes up and more nonlinear behavior is seen around this portion; that is the meaning of that. That should actually be given as the figure caption for this and is given on the next page. Confining of electrons in the notch is not as good; that is the implication.

(Refer Slide Time: 44:47)



From the transfer characteristics…. From this (Refer Slide Time: 44:54), we extract the transconductance g_m delta I_D by delta V_{GS}; that is this (Refer Slide Time: 45:01). You can see that the threshold voltage has shifted to the positive side, just like in the transfer characteristics; it is actually deduced from there. The threshold voltage is shifted to the right because of electrons not being available due to trapping and also carrier freeze-out. This is steep and this is not as steep.

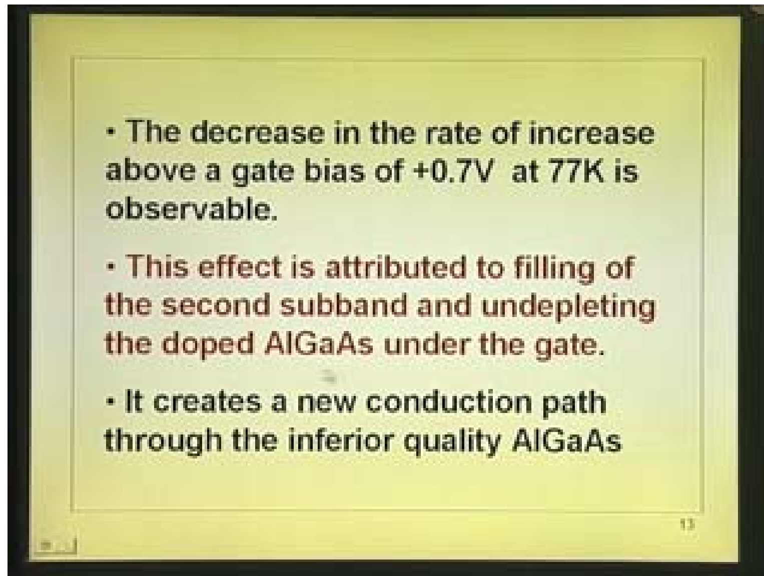
The transconductance is 400 milli-Siemens per millimeter and here, transconductance is about 225. What we are trying to point out here is that whatever we have said now originally, we have got this in the form of a figure. In the output characteristic itself, it was evident that spacing between the characteristics is more, which would mean the delta I_D by delta V_{GS} is more. That is why this is large and we do not have to explain further the shift in the threshold voltage. We have explained that already as due to carrier trapping and carrier freeze-out.

One thing that one should note here is as we go up here, larger and larger voltage, the transconductance increases because V_{GS} minus V_{OFF} is increasing and the number of electrons are increasing but then, afterwards, it does not increase that steeply. Gradually, it tapers off. It tapers off because the mobility of the electrons tends to fall down. In the case of MOSFET also, you will see that because of high field effects in the vertical direction. In this case, there is an added effect. We are talking of this portion (Refer Slide Time: 47:02) applied tapering off or the rate of increase of the transconductance reduces. That is because electrons that are usually present….

(Refer Slide Time: 47:21)

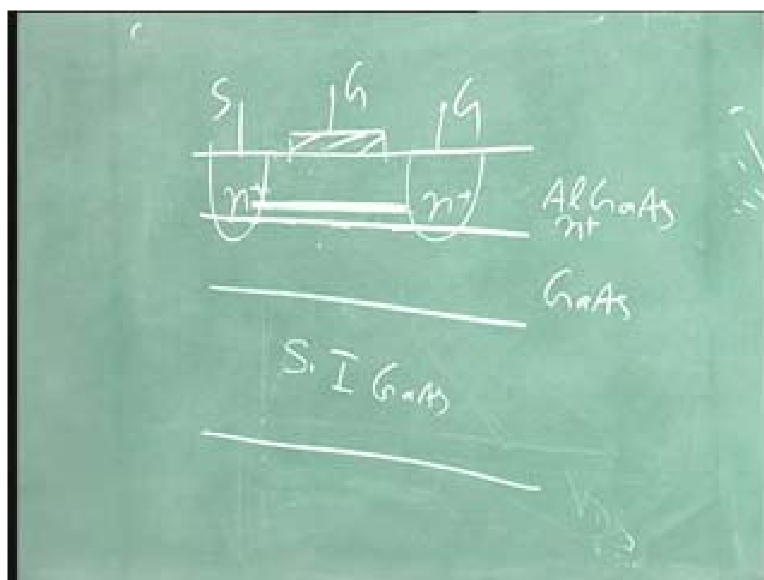
As we go on to higher and higher V_{GS}, what is happening is we are going closer and closer to that and the electrons have got two subbands. It will fill up these levels first and will go to these levels afterwards. More and more will get filled up here as you go to more and more voltages – gate voltage (Refer Slide Time: 47:45). In these levels, the electron mobility is slightly smaller than this; if you go to higher energy, you have lower momentum. In fact, you can see the curves that go up in a momentum curve; their effective mass slightly falls here and because of the fall in mobility, the transconductance is not as high.

(Refer Slide Time: 48:15)



What we are telling is if you go to higher concentrations, the second subband gets filled up. When we go to higher voltages near 0.7 Volts gate voltage, the second subband gets filled up and there, the mobility is lower. Number two: if you go on increasing the bias in the forward direction, what will happen? This statement: undepleting the doped AlGaAs under the gate may happen. I will have to point that out to you.

(Refer Slide Time: 49:00)



If you see here, I have this AlGaAs layer and I have the gallium arsenide layer, undoped. This is n plus. I call this n plus to ensure that it is rather highly doped. Now, semi-insulating gallium arsenide. Those are the electrons. This is n plus and n plus. That is the gate. I keep on making it more and more positive. What happens? If you keep on making it more and more positive, there are more and more electrons here (Refer Slide Time: 50:00) but at a point, what will happen to the depletion layer of this?

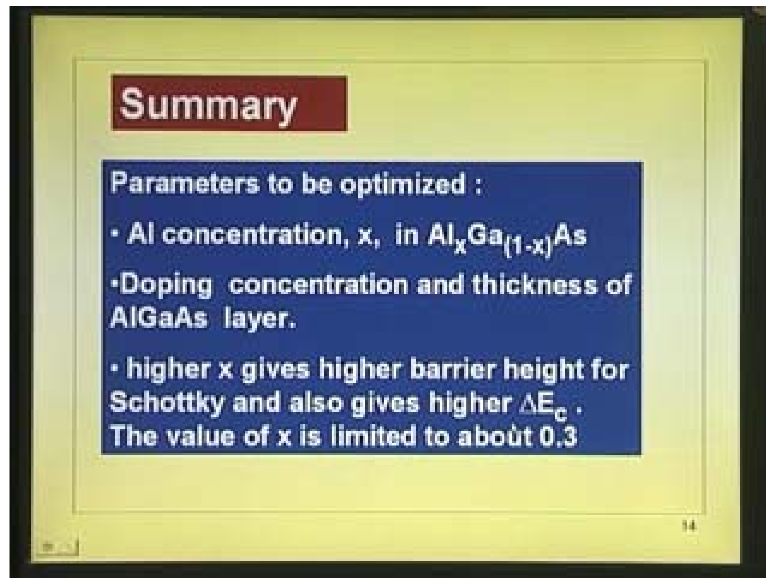
There should be a minimum voltage across this layer – negative with respect to the substrate so that the entire layer is pinched off. We keep on making it positive. I had only this particular layer (Refer Slide Time: 50:21), V_{bi} minus V_{p0} is the voltage that is required to pinch off and I have (Refer Slide Time: 50:28) certain voltage to remove these charges here. What we are doing is in the opposite direction, making this voltage more and more positive. As you keep on making it more and more positive, a situation will come where the depletion layer will open up here (Refer Slide Time: 50:44) till we have charges here. We will have a situation where.… Let me just draw it side by side.

(Refer Slide Time: 51:01)

That is there. I keep on (Refer Slide Time: 51:03) the voltage, make it more and more positive, this will keep on moving up but this will actually keep on becoming flatter and flatter. This is plus here and minus here. I am making this positive with respect to the

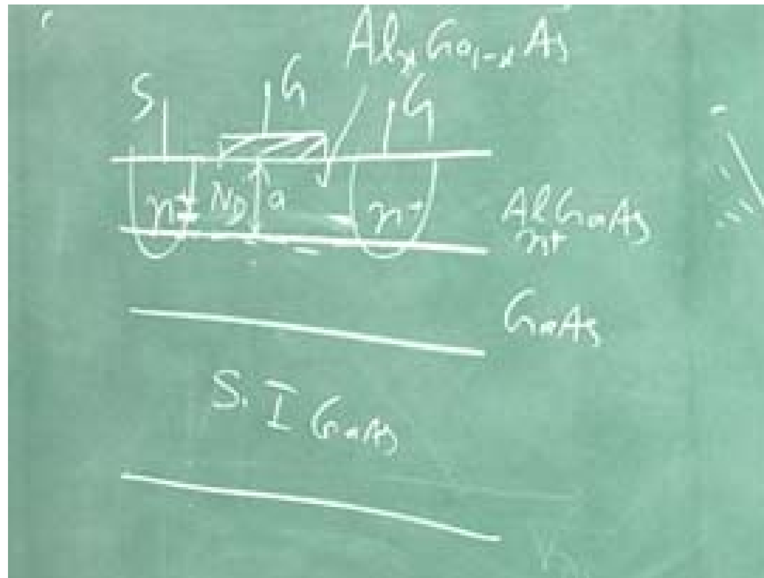
whole thing. So this will keep on coming like this, coming like this and at a certain point, it will open up here (Refer Slide Time: 51:23). It will just open up here like that. If it opens up, that is bad news because the current transport will take place through that layer that is opened up. If that is the opened up layer, there will be channel for current flow (Refer Slide Time: 51:42) through the heavily doped layer. The mobility of the heavily doped layer is low. That is what is implied, if I say…. In fact, since we have discussed in detail how the depletion layer moves with the applied voltages, we can easily grasp that when I apply plus voltage, ultimately the channel will open up. When it opens up, the conduction will take place through the undepleted portion and this creates a new conduction path through the inferior quality AlGaAs, that is, inferior quality compared to this notch, electrons in the notch.

(Refer Slide Time 52:28)



In summary, parameters that you can optimize. Today, I think we will wind up with our discussion on AlGaAs/GaAs system. Maybe, we may have to do the phosphide-based system in the next lecture, but now, we will summarize a few things. Aluminum concentration is one thing that we have to optimize, then doping concentration and thickness of the AlGaAs layer. Aluminum concentration here…. Let me just remove this and keep it all the time in perfect view.

(Refer Slide Time: 53:07)



That is the layer. This is the thickness a and that is the doping and this is…. (Refer Slide Time: 53:23) x, a, and d are the parameters that we have to optimize. For x, there is an upper limit of about 0.3 or so; people do not use beyond 0.3 because of the (Refer Slide Time: 53:39) produced because of the difficulty making Ohmic contact onto this layer. For doping, there is an upper limit, because Schottky will start conducting. The maximum doping is about 10 to the power of 18.

Correspondingly, you can go down to lower a for a given threshold voltage. There is a lower limit of a and upper limit of N_D; the upper limit is 10 to the power 18. Now, depending up on your threshold voltage, we choose this a; you cannot go beyond that for N_D. Higher x gives higher barrier height (we have discussed all those things) for Schottky and also gives higher delta E_c. We need higher x because it gives higher delta E_c and better carrier concentration, but you cannot tolerate that because of the traps that are being produced and band gap. So x is about 0.3.

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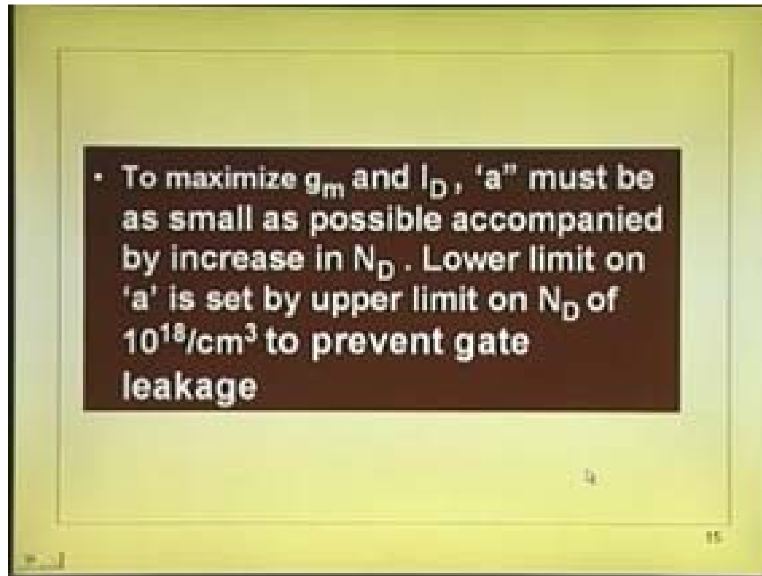
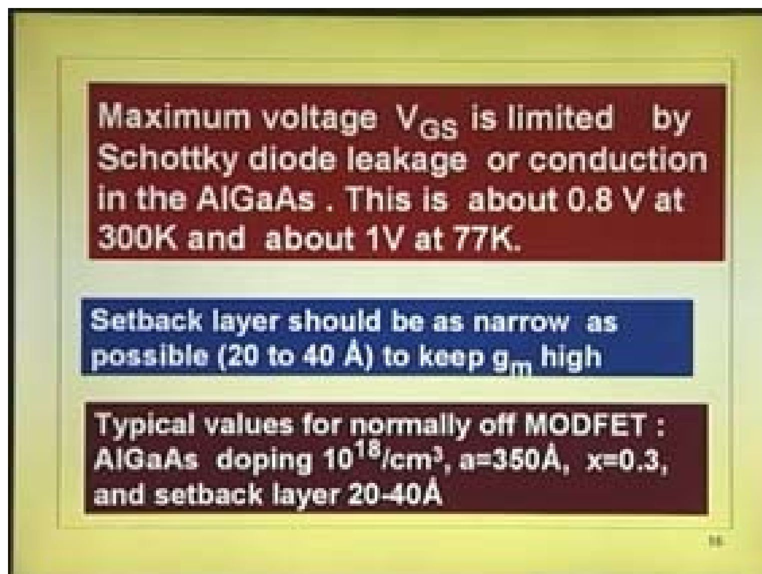


To maximize g_m and I_D, a must be small as possible accompanied by increase in doping. The lower limit on a is set by upper limit on N_D. The moment we say that 10 to the power of 18 is the upper limit of N_D, then the lower limit is set by that for a given threshold voltage.

(Refer Slide Time: 55:04)



The maximum voltage V_{GS}. What is the maximum voltage that you can apply to V_{GS}? This is what we have been just now telling. If you go on applying more and more voltage to V_{GS}, you will get of course more and more charge, V_{GS}. But at a particular point, the aluminum gallium arsenide layer will open up. At that point, do not tell me control beyond that point. The transport will take place through that doped layer. This is about 0.8 Volt at 300 degree Kelvin and 1 Volt at 77 Kelvin.

In fact, the limit can be 2. The V_{GS} that we apply upper limit is for two reasons; one is that the AlGaAs layer conducting and number two is Schottky barrier forward bias condition. That also can happen; any one of them can happen. So, about 0.8 Volt, the (Refer Slide Time: 55:56) is set for the depletion type of devices. If you go to enhancement mode type of device, the limits are lower because the Schottky will start conducting easily. Setback layer should be 20 angstroms to keep g_m high, that is, at undoped spacer layer. The spacer layer is also called as setback layer (Refer Slide Time: 56:18).

Typical values for normally off MODFETs are 10 to the power of 18 centimeter cube for the AlGaAs layer doping, thickness about 350 angstroms, the mole fraction of aluminum x is 0.3, and the setback layer is also 20 to 40 angstroms. We will wind up this discussion on HEMT based on AlGaAs today, but we will take a look at materials like indium phosphide. We will explain why we should go for that, etc., in the next lecture.