Lecture - 12

Metal Semiconductor contacts for MESFET

In our last discussion, we saw or we tried to see whether you can make MOS field effect transistors with gallium arsenide and indium phosphide and it so turned out that it is a tough task because you do not have very good native oxide for gallium arsenide and indium phosphide.

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This problem becomes compounded because of the different vapor pressures of the oxides of the element. For example, oxides, gallium trioxide and arsenic trioxide; those have different vapor pressures. All these put together, it is difficult and also if you try to do extend the technology further by annealing etc., you find that there are elemental arsenic at the interface in the case of gallium arsenide which actually leads to very high interface density and it gives improper CV characteristics which would imply FET is not

giving proper performance in terms of good transconductance. What we are looking for finally is a good g_m.

At the very beginning we said g_m by c is the figure of merit, g_m must be large and for g_m must be large, the drain current change must be large for a given change in gate voltage that will not happen because for all the gate voltage changes, what response will not be the channel charge, it will be the interface charge. It just does not give rise to drain current. So with that, we said it is not possible to make those devices with MOS.

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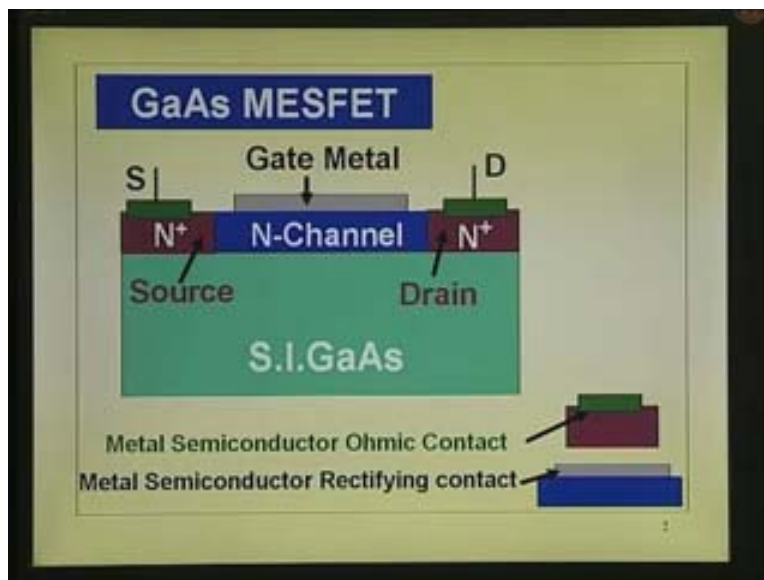
So, the solution they do not worry about the native oxide. Make a JFET or metal semiconductor field effect transistor that is MESFET, metal semiconductor field effect transistor. Now, we also just flashed this light in our last presentation. This has Ohmic contact to the n plus region source, Ohmic contact, metal semiconductor contact, both of them to the drain region because after all you must take external connection to reach electrically to those regions and then you have this metal semiconductor contact which is rectifying contact.

Now we will see, what are the requirements to make these devices, these contacts? So, we will get into. Before going to that few things I want to clarify. So, you have Ohmic Contacts and Rectifying Contacts (Refer Slide Time: 03:50). These are encountered
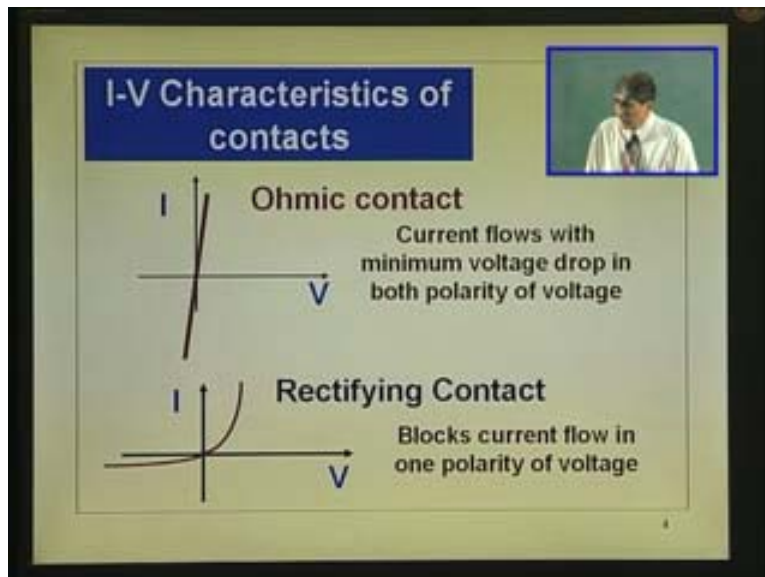
everywhere, not merely for gallium arsenide or high speed, we encounter that in the case of silicon devices also.

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So, a bit of understanding of these devices, how to make them etc. we will just open up. This is just like an illustration of the Ohmic Contact.

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After all, Ohmic contact should have the current to flow through that and you will have a linear characteristic in a forward and both directions. So, delta I by delta V is the slope of this line. Ideally that slope must be infinite, vertically going up but you can never have a current for nothing. We should have voltage drop across the device that should be minimum. When you say Ohmic contact is good, you see that it is more and more vertical in characteristics. Now other one is Rectifying Contact which all of us talks about it and concern worry about it throughout our discussion so on devices and circuits. So that actually will block current flow in the one direction, ideally, ideally a rectifying contact, an ideal contact should be like this (Refer Slide Time: 05:01).

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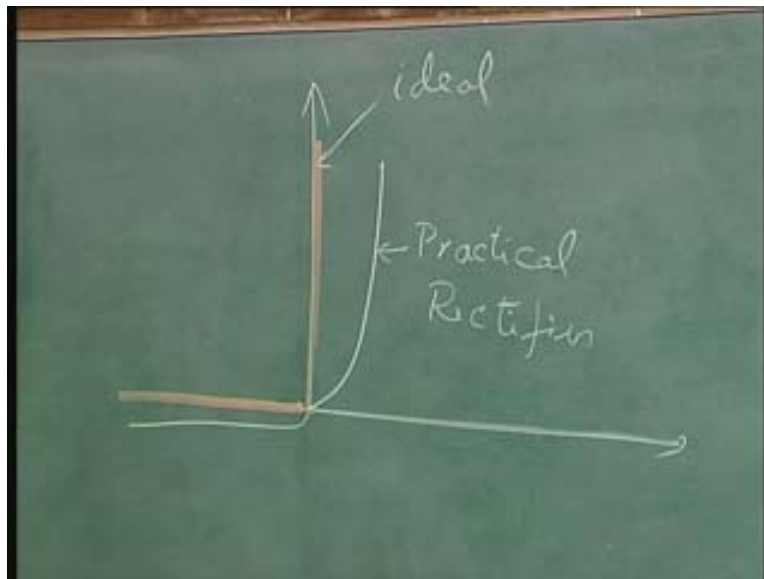
Ideal contact, rectifying contact should be, it conduct 0 voltages. It will block with 0 current, we never get that. So what we get in that is, this is ideal. What you get in fact is this. All of us know that is the forward and in the reverse close to this, but the difference scale it will show like that. So this is the Practical Rectifier.

Now, we will get around and see how to realize this in practice (Refer Slide Time: 05:57). So after all, you need that the source and drain that type of contact. At the gate you need this type of contact. It can be junction diode. But now, what you are talking of

is a metal semiconductor contact which will behave like a pn junction. So, now you are on to the energy band diagram of the metal semiconductor contact.

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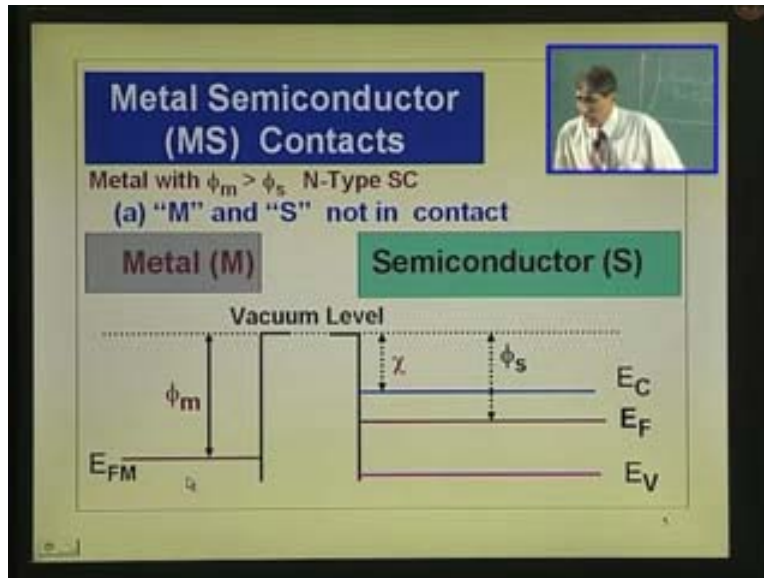
We talk of this diagram shows you the two materials. That is the metal and the semiconductor which are not in contact and they are separated in space. No electrical connection. Now, on the left hand side here right below this point, I have shown the Fermi level of a metal EFM, Fermi level of a metal and I have shown the vacuum level.

So this phi$_m$ what you have put there with an arrow is actually the work function of the metal. To talk in terms of energy, it is the energy difference between the vacuum level and the Fermi level. In terms of physical phenomena, it is the energy required to remove the electrons from the Fermi level to the vacuum level outside the metal that is the indication of that. So that is the energy band diagram or the energy level diagram. This is for the case of the metal.

Now if you take semiconductor, I have put entire energy band diagram, conduction band edge EC, Fermi level EF, and valence band edge EV. The very fact that I have drawn the Fermi level closer to conduction band tells you it is n type material. We were talking of a metal and a semiconductor and an n type semiconductor. In general, whatever we are talking of is true for silicon, gallium arsenide, indium phosphide, and gallium nitride. So

now here, _____ few things are there, a phi$_s$ is the work function of the semiconductor. Again you talk of the electron, the energy required to remove the electron from the Fermi level to the vacuum level. There are no electrons in the Fermi level but conceptually you have to have landmark to see from where you measure, so that is the work function of the semiconductor and here one more term chi, it is a usual symbol that you use chi is the electron affinity of the electrons in semiconductor. That is energy difference between the vacuum level and the conduction band edge. With those definitions we can proceed further. So we can see there is a gap this dotted line that have I put there (Refer Slide Time: 08:50) here it shows the vacuum level.

Now next what we will see is bring them into contact. I will not move them closer. They are just close by enough, but I will connect them through external wire. This is all the definition that we have said just now. So we do not have to go through that. That is work function is energy difference between vacuum level and the Fermi level.

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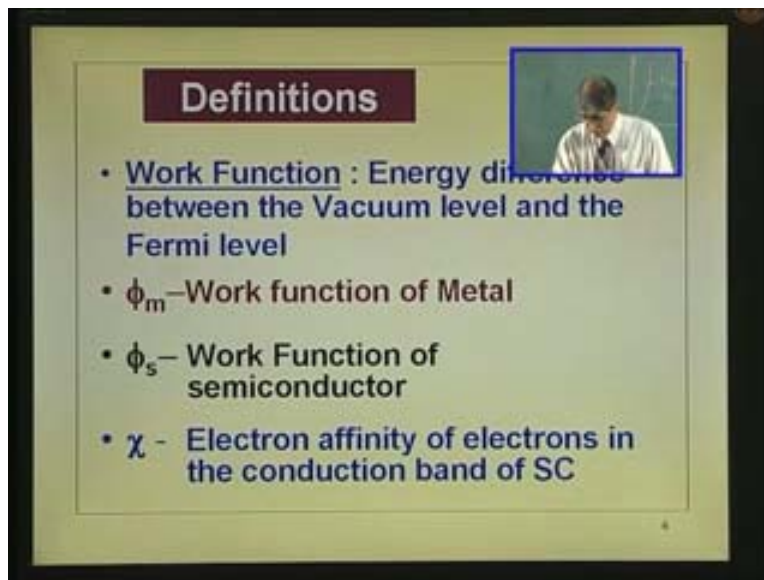
Phi$_m$ is the work function of the metal, phi$_s$ is the work function of semiconductor, energy difference between the vacuum level and the Fermi level in the semiconductor. Chi is the electron affinity of electrons in the conduction band of semiconductor, pre EC and vacuum level. So when you bring them contact all that I have done is I have not moved anything. I have just connected them together.

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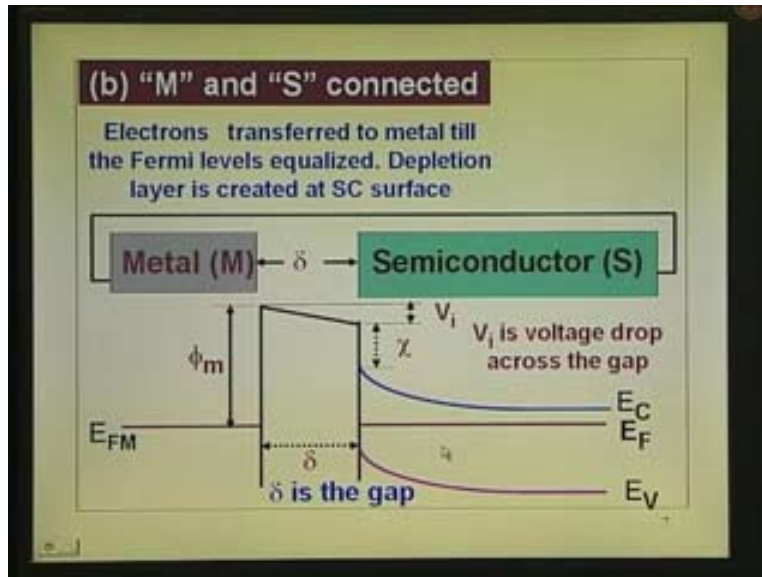
Now let us go back to this diagram see, and original diagram and see, what is the situation? If you connect them together externally what would happen, we will see? The actual diagram we will see afterwards. See here, the Fermi level here is above the Fermi level here. The moment you connect them together need not join them, bring them close enough and connect a wire between them.

Now, just like in the case of pn junction when the transfer of electrons from the semiconductor to the metal because Fermi level is higher above the Fermi level in metal EF is above EFM. So result is the probability of occupation when a system must be the same thing with reference to the Fermi level. So the Fermi level will immediately equalize and to equalize the Fermi level, the electrons will move from here to here (Refer Slide Time: 10:36). In fact what is happening is you find that there is lot of electrons here much higher than this level where there is energy available.

So, if there are energies available, the electrons will go and occupy that level. That is what happens. Electrons from this level get transferred on to these levels which are available in the metal. So once the electrons are transferred, what happens? That is what we are seeing here (Refer Slide Time: 11:10). The electrons from this region are transferred through the metal here on to the other side. That means the metal is negatively

charged and the semiconductor is positively charged and from the Coulomb's ____11:19 ____ law of force, we can see that whatever happens, happens to the closest points, minus charges will be present on this side and a plus charges would be present on this side. So if you just see the diagram there, what happens is?

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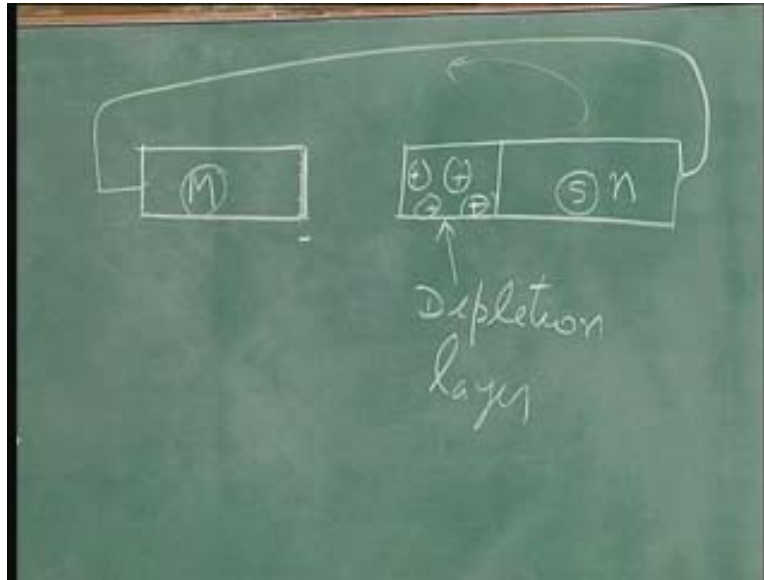
I have the metal; that is the metal. I have the semiconductor. I am just drawing that because some of the things are not clear there. This is n type semiconductor s, this is metal. I have connected them together. So what has happened is, this has acquired negative charge because of transfer of electrons from there to here to equalize the Fermi level. Now this has plus charge. The number of electrons are the doping concentration in the n region 10 to power 15, 16. Here electron concentration is metal 10 to power 22 and above. So if you put in few electrons here, it is not going to occupy space. It will just be a monolayer of that will give that negative charge.

So, you have negative charge here. The net positive charge will come from a finite width. So, there will be depletion layer. So, the moment you connect because of transfer of electrons from the semiconductor to the metal, because Fermi level is above so electrons will get transferred till the Fermi levels are equalized. I have drawn this diagram which

has finally equalized and the equilibrium condition, we have drawn that. So when you do that, there is a depletion layer. In fact this diagram I have not shown there.

But if you look at energy band diagram (Refer Slide Time: 13:24) the Fermi levels have got equalized because of transfer. The whole thing is because now the energy diagram has tilted with this side positive and that side negative. Wherever the band bending is there, there is potential change. So there is potential change from this into that. This is plus and this is minus. So the charges which originate over this region, they terminate here. You just see this is here. If you see this gap which I have marked there (Refer Slide Time: 14:02).

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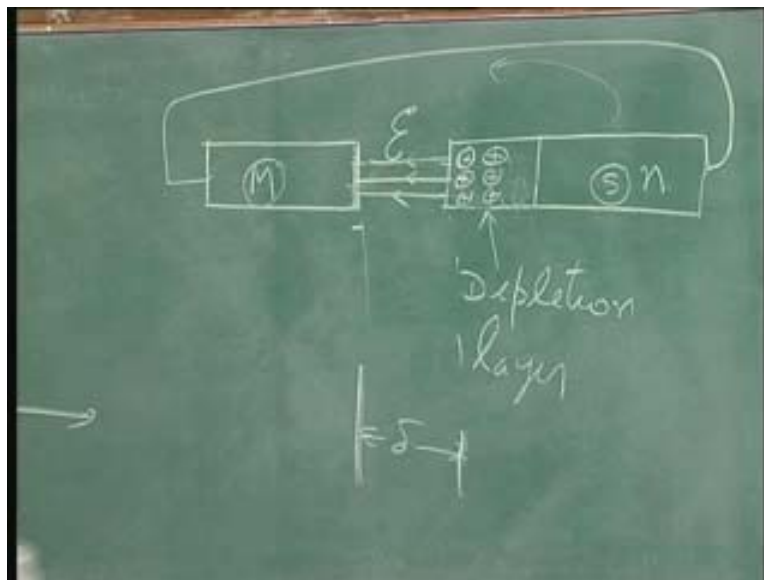
There are electric fields like this. There is electric field like this. Electric field goes into that. For that, we draw it better. I will draw 3 here; 1, 2, 3 if I put here, they will come down like this. That is electric field. Number of electric field which crosses will be equal to (Refer Slide Time: 14:35) how many electrons have moved from here to here. For one electron which has moved from here to here through the outside wire, we have got one positive charge and one negative charge.

So that one field line is there. So, once you have connected them together, the charge here and charge here is fixed. That means the electric field here is fixed. How much is the

potential drop here depends upon how much is the gap. Electric field into the distance here is your potential drop linear that is what is put here, that is the vacuum level. The vacuum level itself tilts now. So this slope here indicates that there is a constant electric field.

Therefore linear voltage dropped across that point. So the conduction band or the vacuum level here is going linearly like that and you can see that is the particular portion here. That is not linear because you know that whenever there is abrupt junction, wherever there are there is depletion layer, the voltage is parallel. So that is what is shown by this portion. So you have got the voltage change here (Refer Slide Time: 15:47). That is shown by the change in conduction band variation and beyond a certain point it is flat and it is flat beyond this portion because this is neutral region there is no voltage drop. When there is no voltage drop, band diagram for flat that is shown in that portion. Here, there is a variation in the band diagram because there is a potential change from here to here. This is positive, this is minus. So there is a drop V_i in the intermediate level and there is a drop in the semiconductor corresponding to this position and this position. Whatever is the slope like this, (Refer Slide Time: 16:29) if I have slope like that, there is a drop in the semiconductor. So, what I want you to note here is that the voltage dropped V_i for these two semiconductors depends upon how much is the gap. This band bending is fixed. Because number of electrons, which I have moved are decided by how much is the difference between the phi$_m$ and phi$_s$. Go back to that (Refer Slide Time: 17:05), this phi$_m$ and phi$_s$; this difference between this level and that level. That is the total potential change that you get from one end to other end. So now, let us go back to this (Refer Slide Time: 17:15). So when you move into this particular thing, this if I reduce the delta that drop will be reduced.

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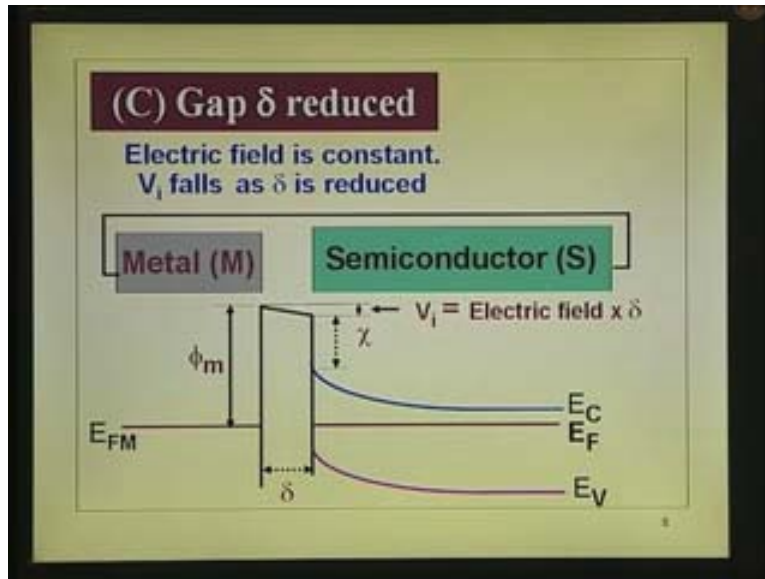
That drop will be reduced but the charge within the particular region is the same thing, because number of electrons which are moved is the same thing. Otherwise, the energy band diagram has remained the same practically. All that has happed is this drop has changed and reduced. I am keeping on reducing it because we are talking of not MOS or MIS. We are talking of MS further reduced.

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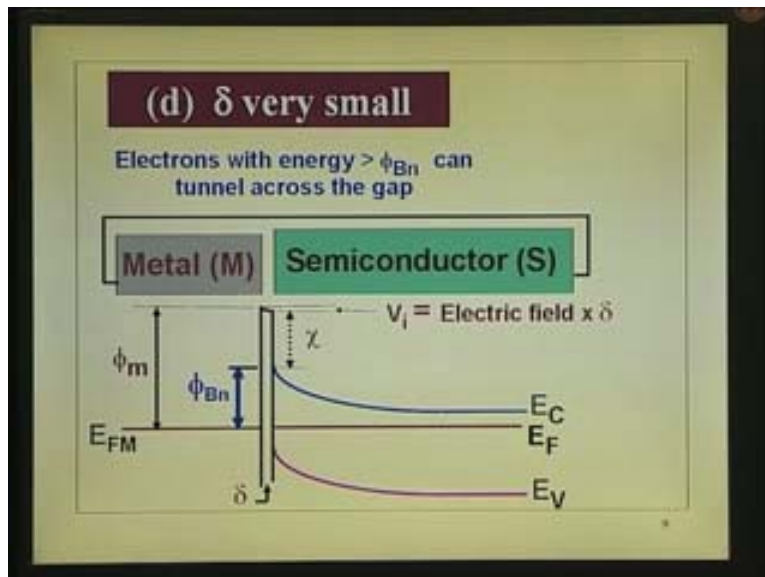
Now you can see the entire drop is in the semiconductor and the drop here is very, very small. So, if I have electrons here up to this point here (Refer Slide Time: 18:07). There is a possibility that they can cross this when it is thin. Because when the oxide becomes very thin and if there are states available on the other side, which actually is present here. This is conduction band of the semiconductor. Electrons can cross if they have enough energy. So, there is chance for that to flow. Now what we are talking of is not even that layer present. Electrons with energy greater than this phi_{Bn} can cross this way or that way. Thermal equilibrium of course, of course, there will not be any net current flow because what crosses from this side to that side will balance each other. Now look at what we have done. We have removed even that layer. So far, we are doing the whole thing with a contact; removed that, I removed that contact now. That is I have removed that external connection and just put that.

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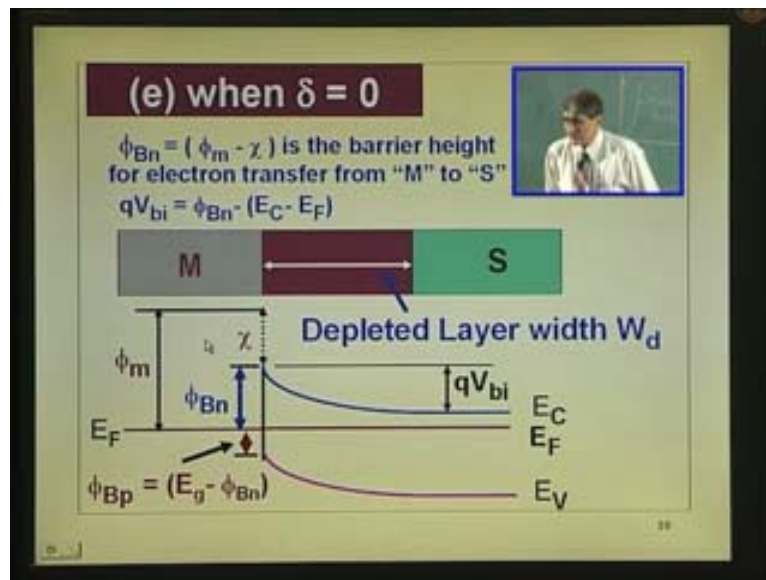
Now that it is in intimate contact. The metal M is intimate contact with that. There can be exchange of electrons directly through that. You do not have to go through external path. So all that happened has you have shown for finally with this. With the metal contact itself you have got it together like that, that is the diagram.

Now, if you remove the metal contact also there is no problem. So, now you can see the vacuum level phi_m. This is the conduction band there chi up to the vacuum level and

what else phi_s is from here to that point from here to that point. But just one thing I want to point out here, I have not drawn the vacuum level on this side. How will be the vacuum level will be on that side? See you have not shown even here (Refer Slide Time: 20:07). I have not shown the vacuum level at that point. So, the vacuum level will show wherever the potential change is there, it will follow the same path. So, I just draw that for completeness sake.

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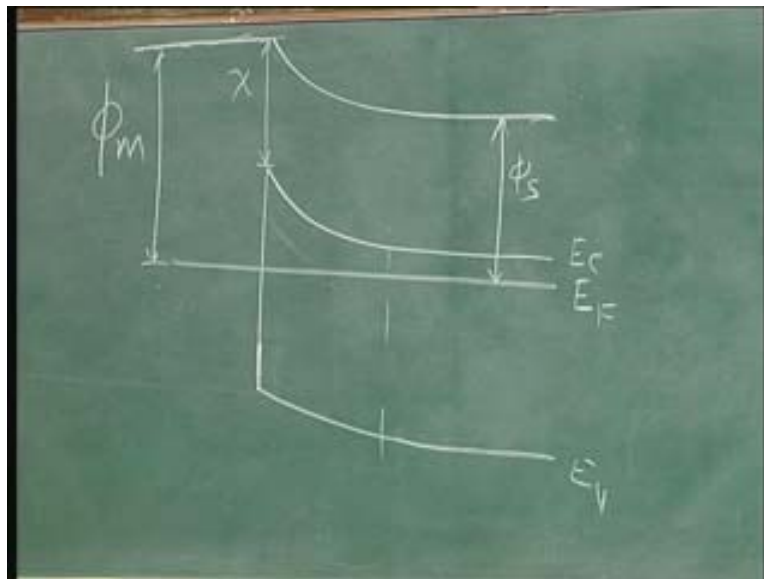
So, what we are trying to see is, you have the contact like this. I am redrawing the diagram, the conduction band, valence band etc. This is up to where the depletion layer is present. When I am putting this Fermi level here, in contact aligned with their respect to each other, just like the case of pn junction EC, EV. Now what we are showing there is, the vacuum level. That is the vacuum level and this is phi_m, redrawing it here for clarity and this is actually equal to chi. Wherever potential changes take place except Fermi level all other energy levels follow the same path. So this level also will go, from here will go like that.

We have taken the situation where phi_m is greater than chi, phi_s. You go back to this diagram and see starting diagram (Refer Slide Time: 21:52), if you go back just notice here. Right at beginning I have put it there phi_m I greater than phi_s. That means actually this Fermi level is the difference between the vacuum level and Fermi level here is more

than the difference between the vacuum level and Fermi level which means the Fermi level is here, it is above the Fermi level there.

Now finally what happened is; this Fermi level has come down because of transfer of electrons and the potential has appeared. So that is what we have shown there. So phi_m is greater than phi_s. Now this level, this quantity is phi_{Bn}. That is the quantity which we are looking for because that is actually the barrier for electrons from this side (Refer Slide Time: 22:56). If there are electrons in the metal to cross from there to here, it has to go up this barrier. Because, if there are electrons here if there are levels on right hand side it can cross. There are no levels. So, if at all it has to move to the metal it should have sufficient energy so as to go into the region where energy levels are present, conduction band. Now we look at the semiconductor portion. Between this neutral portion and the surface, there is a potential change and there is a potential change and that potential change is V_{bi} which you can call it as built in potential like in the case of pn junction, it is exactly like in the case of pn junction.

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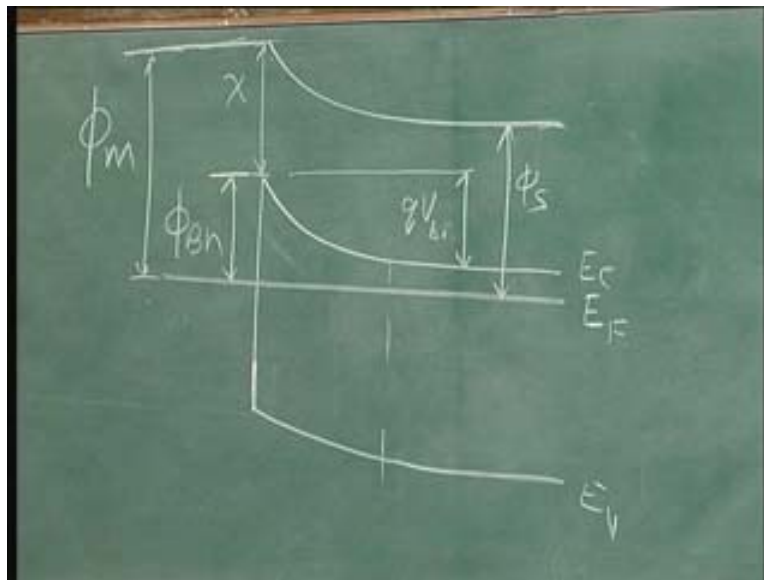
You have the built in potential V_{bi} and that V_{bi}, in terms of energy q V_{bi} is equal to that is this V_{bi} that is the q times V_{bi}. Because there is energy like band diagram that you are

showing out q times V_{bi} that is equal to phi$_{Bn}$ minus this. Phi$_{Bn}$ is this quantity minus this, EC minus EF that is q V_{bi}.

So now what is phi$_{Bn}$? Phi$_{Bn}$ is actually phi$_m$ minus chi. this quantity is this minus that, phi$_m$ minus chi. so once you have fixed a semiconductor and a metal, phi$_m$ is fixed. When a particular semiconductor once you choose a metal phi$_m$ is fixed; once if you choose the metal and semiconductor that is fixed, because phi$_{Bn}$ is actually equal to phi$_m$ minus chi. I have just had redrawn the thing so that the further clarity is there. That is this phi$_m$ minus chi is phi$_{Bn}$ that is there. Chi is fixed to the semiconductor. It is independent of doping. You can see that. It is only dependent on the work function. Then this built-in potential in addition to that phi$_{Bn}$, it depends upon EC minus EF that is actually a doping level. If the doping is increased Fermi level goes towards the conduction band. So that is actually built-in potential. So, we will have slightly if it moves up, we will have slight reduction in the V_{bi}. That will be we will come back to those discussions.

Right now, what I am focusing is this quantity mainly and that decides what is the built-in potential guided by doping of the material. Notice here, this is the barrier height for electrons to move from the metal to the semiconductor and correspondingly can mark a barrier height here for transfer of holes in this direction that is phi$_{Bp.}$

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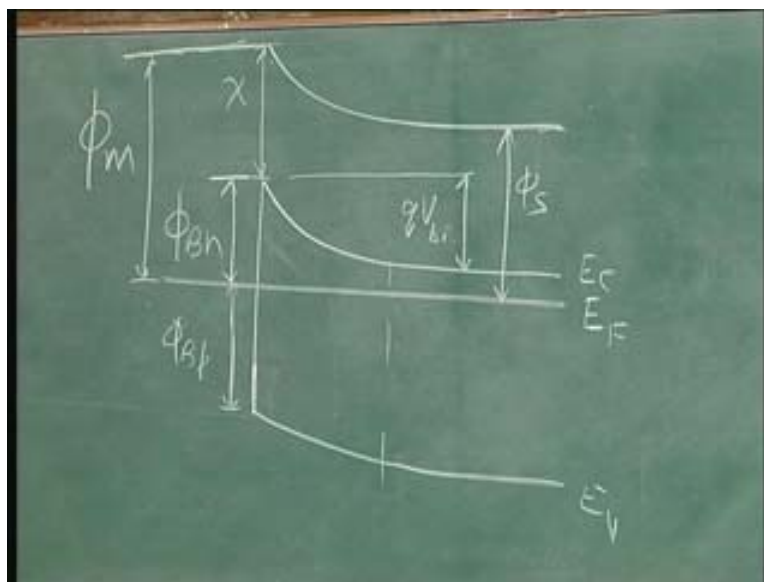
Phi$_{Bp}$ is this quantity, that is phi$_{Bp}$ and that quantity is, what is this much bg band gap minus phi$_{Bn}$ is phi$_{Bp}$. So, the moment you fix metal phi$_m$ is fixed. Moment you choose the semiconductor chi is fixed. So phi$_{Bn}$ is fixed and once you fix phi$_{Bn,}$, phi$_{Bp}$ is given by that bg minus phi$_{Bn}$. Because for a semiconductor bg is fixed. These are fixed quantities, independent of doping. So that it looks from here that the main player in the game is phi$_m$, metal work function because that is the one which decides barrier for electrons and barriers for holes. Why are you worried so much about barrier? The barrier is the one which allow or not allow the electrons to flow. Take a look at that.

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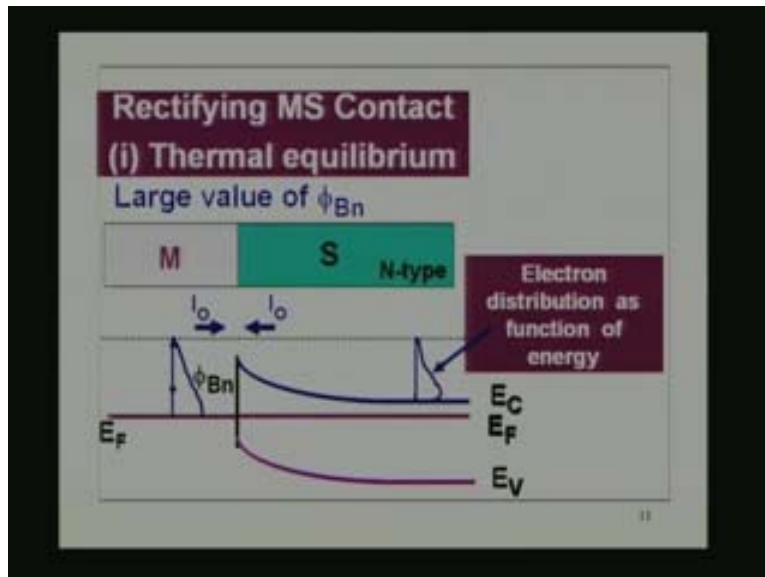
Now this is diagram which I have just redrawn that removing all other unwanted things just only the main particles which participate in the conduction mechanism. So this is the phi$_{Bn}$ and we are still talking of n type material, because p type, we can work out same way. So this is the phi$_{Bn}$ from there to here. This is the phi$_{Bn}$ whether it is a not very clear. Phi$_{Bn}$ refers to this point, not the whole thing. This phi$_{Bn}$ should come, I will just redraw that, I mean it become can clear that.
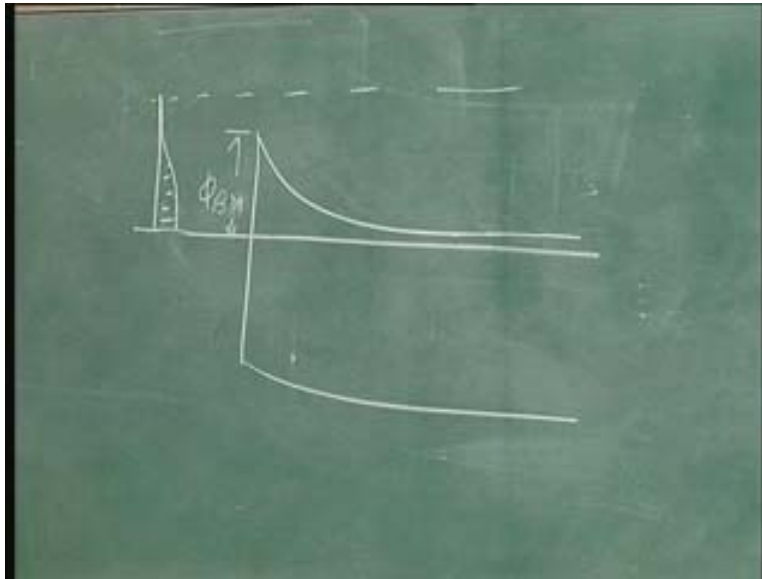
So, what we have drawn there is like this, simple diagram like that and the Fermi level here like. This is of course parallel to that. That is what we have done again. Now what I have drawn is this distribution, this is phi$_{Bn}$. Somehow that point what I put there is referring to this barrier end. That is known by now that is the barrier end. So this is the phi$_{Bn}$. What I have put here is that line correspond to tip of that. What is this mean? This is actually if you closely observe I will just draw it like that. This is the electron distribution, distribution of electrons in the metal as energy goes up. After all, Fermi level is defined as the level up to which electrons are occupied at 0 temperatures.

When you raise the temperature at room temperature many of electrons point them through the energy above the Fermi level and this is the distribution. The probability of occupation goes on decreasing as you go up. This is actually the probability of distribution. In a metal, there are number of levels which are present there but the whole thing is guided by the probability. It is virtually the probability distribution of function that I have plotted. So this does not go into that, does not become 0 is there. So, what I am telling is you will have electrons energy above this barrier, some of them. These electrons have energy over and above the barrier.

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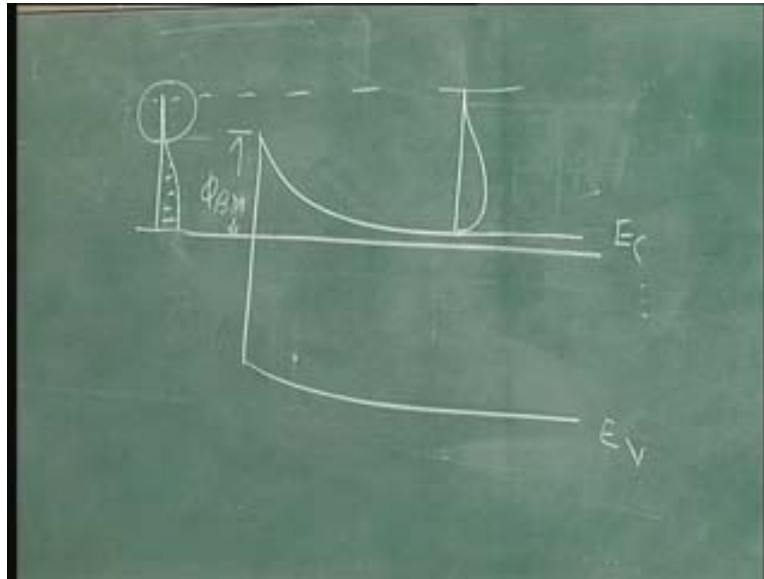
Now look at the semiconductor, there also I have plotted that, like that. What does it mean? That means this conduction band is here, valence band is here. This is the product of density of states available in the conduction band multiplied by probability and how does it come? This quantity is coming like this (Refer Slide Time: 30:56) density of states actually is going like this square root of E minus EC and probability function goes like this.

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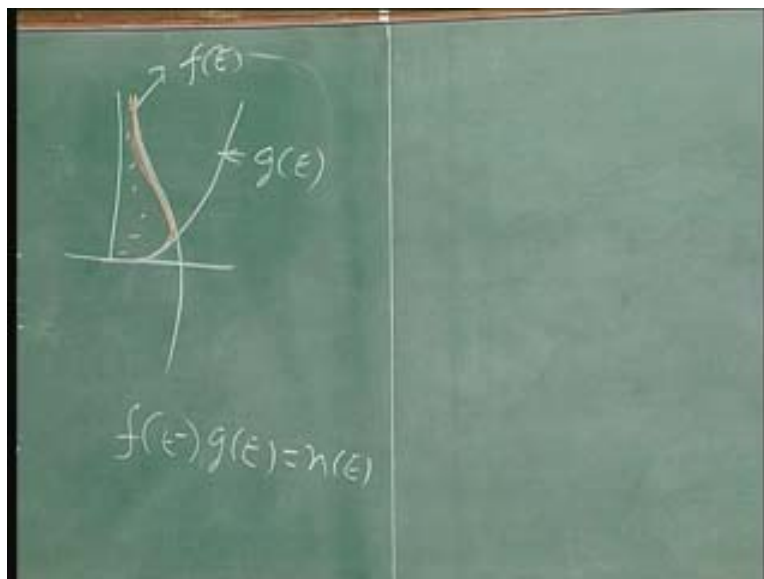
So, this is a FE Fermi graph distribution function and this, what symbol do we use? It is GE density of states. Product of those two FE into GE gives you n as the function of energy that is what you are plotting here. Product is product of these two will be this 0 multiplied by something is 0. So it goes up like that. That is how it is. That is what you are plotting there. So, this is actually the distribution of electrons. Now that is what I put here. So you have electrons like that.

Now you can see the Fermi level has adjusted itself ultimately by transferring electrons from this semiconductor to the metal in thermal equilibrium such that the distribution tip here, distribution tip there almost match which would mean under thermal equilibrium conditions the number of electrons above that if you integrate and number of electrons if you integrate above that they should be same to you. Because these electrons can cross this way like this, they can cross this way like this, number crossing from metal to semiconductor will be equal to number crossing from semiconductor to metal, thermal equilibrium situation. Thermal equilibrium means you do not apply any voltage, do not put light. It is energy exchanges between _____ temperatures is the guiding line, nothing else is there. The semiconductor is in equilibrium or the entire system is in equilibrium with the particular temperature. So that is what I have put there. So just note that this phi_{Bn} refers to this height. Now, what I have put here is I_0. What is that I_0? If you understand this, we can quickly go through the whole thing.
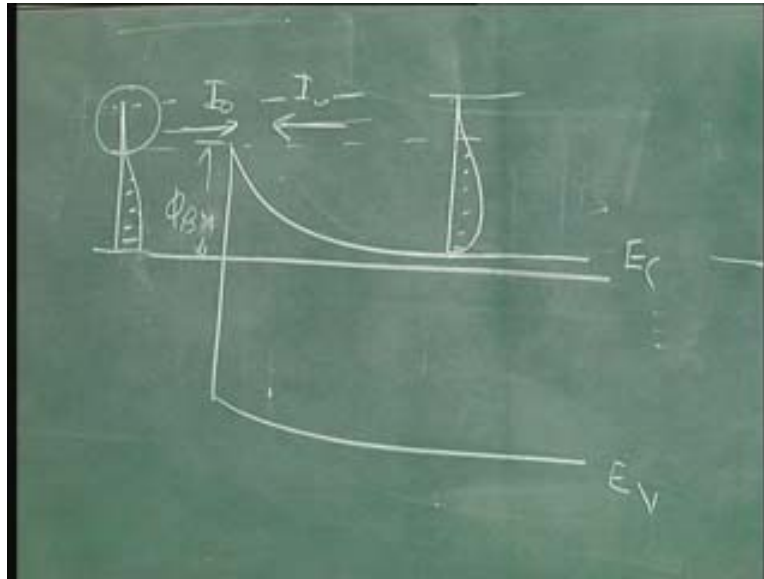
This quantity gives rise to current I_0 here and this quantity gives rise to current I_0 here that is what I have marked. All those electrons which have energy above this barrier that is on the left hand side that portion what I have circled here, they will be crossing this barrier; if there is no barrier that will give rise to current I_0. These electrons which have energy above that could give back rise to current I_0 to compensate. In other words, what we are telling is net flow of electrons is 0, I_0 from there; I_0 from here. If you disturb that if you are disturbing that current injected from left hand side and right hand side. So this is the situation in thermal equilibrium conditions. Now if you apply bias to the semiconductor what will happen?

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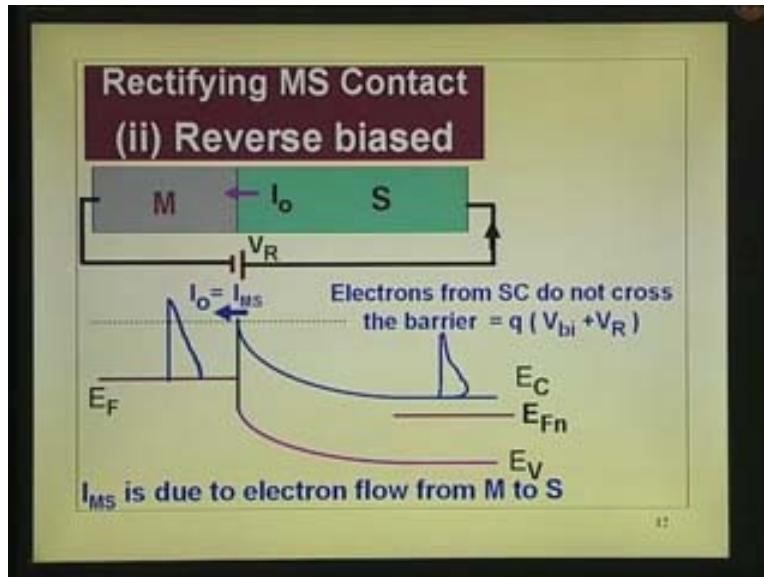
Just notice that was thermal equilibrium, I just applied a reverse bias. I made this region positive. This is thermal equilibrium. If I make this region positive, what happens?

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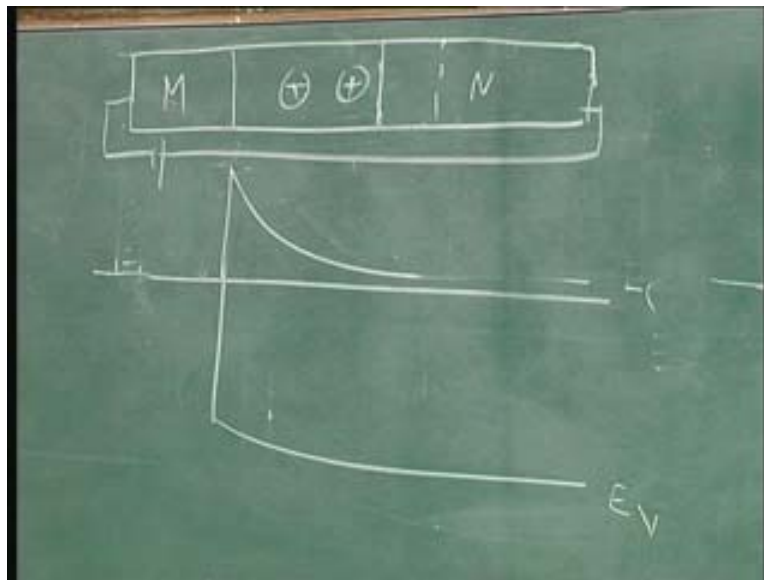
Let us just remove these things now. I just put this diagram here that is the junction metal semiconductor junction if you want to call, metal and this is the n type. So originally you have this that is the depletion layer. When I apply reverse bias what happens? Where

does the potential go? It will appear only into the space start region. It will appear only in the semiconductor because the charges here will be right on surface available minus charges. So it will actually widen and if it widens what happens to this height. Whatever was V_{bi} will become more. So that is what has happened, so that is what you have seen here. Here the Fermi levels are same. Now this portion as it is the entire things come down. So the Fermi level here in the neutral portion will come down that is shown here.

We will come back to that. See what is happening is the right hand side electrons here they have been taken out in this direction. A moment to switch on there is a transient which will pull from here to here. These electrons are there, they will open up. Depletion layer is widened by removing the electrons from here to that side. When you apply a battery, what you do? When your depletion layer is moved here, you have removed the negative charges from here more and those negative charges have gone from this path like this to this side. So your field has gone up there. The peak field has gone up here. The potential drop has increased. So, I have however answered your question. So that is why you have got the potential change from here to here have increased. This is what was originally that potential qbV_{bi} has now become equal to qV_{bi} plus V_R, V_R is supplied voltage. What is the consequence of this? That is the diagram which I do not have to draw, you can see here. What you have to see is the neutral portion whole thing has come down and this portion has slightly widened. So when the neutral portion comes down what happens? I have drawn it there already. So originally it was here. Now, it has come up to this point.
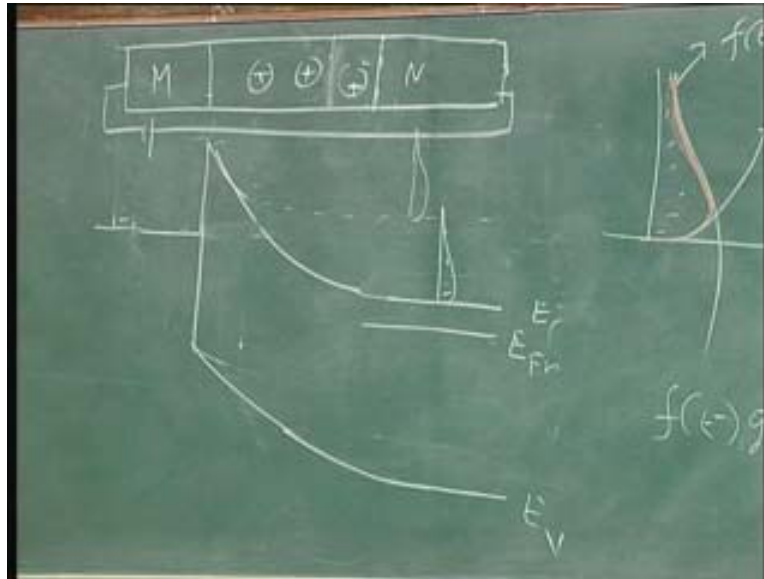
So, what was here originally has come down to some extent like this. I have drawn it magnified that has come down like that. That is the neutral point has come down like the conduction band and valence band correspondingly has gone down. So EC and EV in the neutral region remains the same thing, the gap but only its energy has lowered down because of plus charge on other side. Now what about this portion? What was originally here which was going above that like that, because some of them were able to cross, this level. This is the kinetic energy of the electrons. The kinetic energy is 0; the entire energy is potential energy here. So, as you go up that is thermal energy because of that kinetic energy. When you push this conduction band down you are bringing the potential energy down. The kinetic energy remains the same guided by temperature.

So, this distribution in the neutral region remains the same thing. The whole level has come down and from here, it is coming down like that and you cannot draw the Fermi level now here, you cannot draw the Fermi level here, you draw it only there and call it as cozy Fermi level means actually you can still compute electron density using this Fermi level with respect to conduction band that is the meaning of cozy. You do not talk about that here and from here the whole thing comes down. So that is the new energy band diagram. What is the consequence of that? You know these are just basic concepts which once are cleared we can move further. What happen to this barrier? That barrier has not

changed because there is no depletion layer there. There is no potential drop across that, so that barrier remains the same. Phi_{Bn} does not change. So now, let me just draw this here once again whatever you have got there. This phi_{Bn} has remained the same thing.
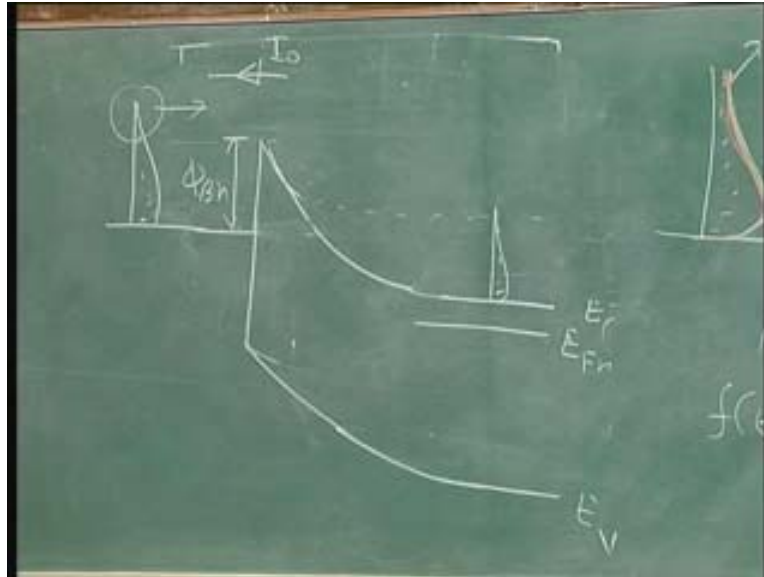
So, as far as the electrons are concerned, distribution is concerned here, what does happen? We have drawn it earlier like that, thermal equilibrium situation. Whatever electrons are there, they can cross the barrier still, if that barrier does not change. Whatever was giving rise to current electron transfer from left hand side metal to the semiconductor remains the same thing that we called it as I_0. If that is continuously transferred, we will get a current I_0 and the direction of the current is actually transfer from (Refer Slide Time: 40:53) here to here, actual direction of current flowing like that, semiconductor to the metal that is what I marked there.

This is actually due to the extra electrons which have energy above this barrier. They can cross from this side to that side because that is the conduction band and that will give rise to current I_0 which we call it as I_{MS}. I_{MS} is actually due to the electron flow from metal to semiconductor. It can be continuously flowing. So that is why you get a current in the external circuit. It has got to be from positive terminal of the battery while that is the one which is driving the current. It goes from here to there and from semiconductor to metal.

I have marked it I_{MS} because MS telling you direction of electron flow from metal to semiconductor, I is the current actually which is flowing there that is the direction. What happens so that the current which was flowing from semiconductor to the metal. You have pulled the potential energy down here. Originally when it was here, there was having energy like this (Refer Slide Time: 42:03).

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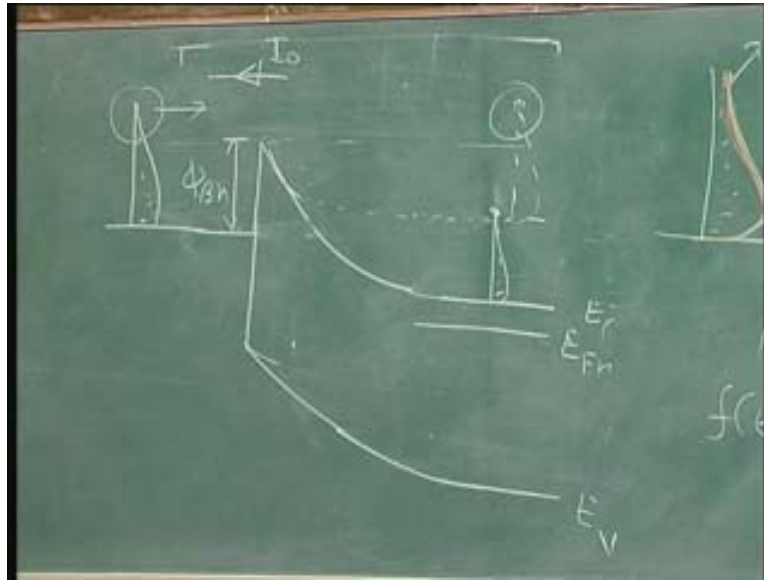
Let me draw it by dotted line before that. You had this energy band diagram like this. You had it like this. Those were the ones which were compensating for that thermal equilibrium condition to make the current equal to 0. Now this current has not changed I_0. What about this transfer of electrons from semiconductor to the metal? That has dipped down because these electrons, the maximum energy that these electrons have in semiconductor is up to that point. Beyond that point they cannot cross the barrier. They do not have energy to climb up the barrier, so they stay there.

So the entire electron flow is due to the transfer of electron from the metal to semiconductor which is actually I_0 and there is no transfer of electrons due to from the semiconductor. So now how much is I_0 decides how much is the current now flowing here. How much is I_0 depends upon this barrier. If that barrier height is small, let me just draw that. Suppose I have a barrier like this.

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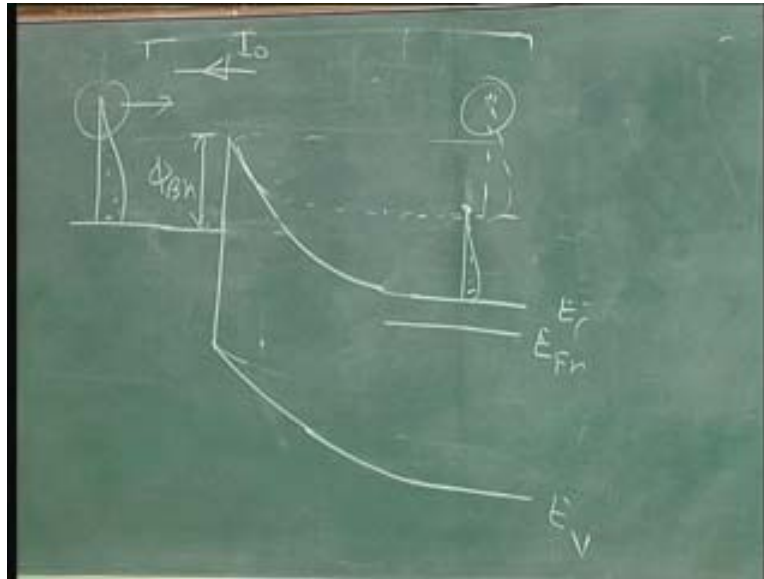
A barrier, I think you can figure it out right here. These electrons have energy above that. Suppose these barrier was smaller, this point is shifted up more number of electrons will be having higher energy. So if you shift the whole thing up, more electrons have the higher energy. So phi_{Bn} if it is smaller I_0 will be larger. The current when you reverse bias will be larger if the phi_{Bn} is smaller because if the phi_{Bn} is smaller you are lifting the left hand side up all the way, so you will have more electrons which can cross that. You can look into it either way. You can just hold this here, pull this fellow down the entire thing down, all these electrons will have energy up. Supposing I have the barrier only this much, all these electrons have that energy.

So what I am trying to point out is, if you want to cut down I_0 we must have higher I_{Bn} or phi_{Bn} that is what you have to do. So these are key things whether you want to decide a rectifier or an Ohmic contact. Now let us see what happens and this barrier now you see. How much is this barrier depends upon? V_{bi} plus V_R. V_{bi} was just enough to compensate for I_0. Once we have put V_R sufficiently large I_0 is not compensated at all. You have the net current flowing through that. Forward bias metal made positive with the respect to a semiconductor. What happens now?

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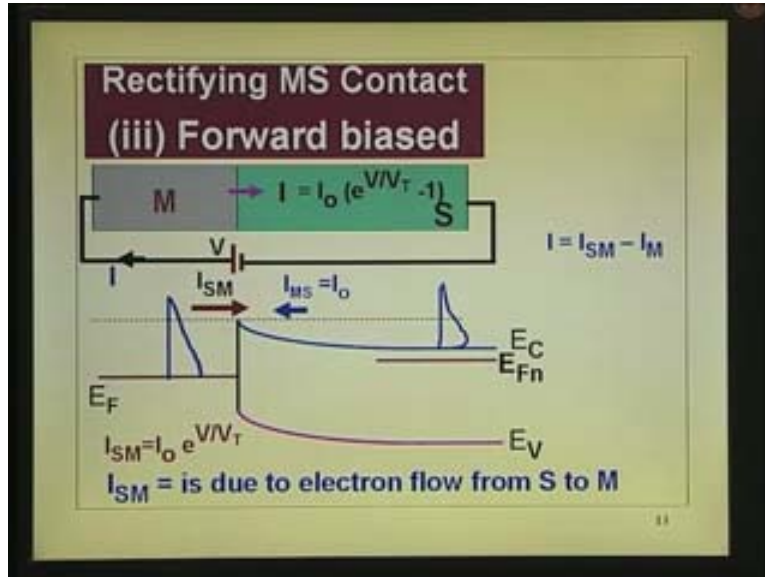
Now, let me remove this point. Let us redraw that. I have drawn that already there. We just want to illustrate to you with that. You have here this barrier. Whatever you do, that side is not changing. So thermal equilibrium you had the situation where the Fermi level was here and we have the energy band diagram like this (Refer Slide Time: 45:42) that is thermal equilibrium.

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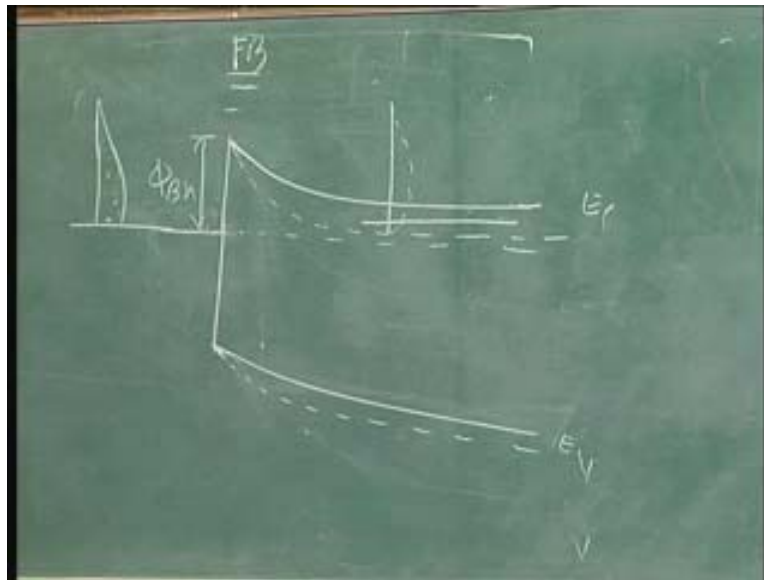
I am drawing dotted line because when you forward bias FB whatever barrier was there having a potential plus minus. If I apply plus minus there like what you have done in forward bias you are reducing the potential across the device. So whatever this Fermi level was equalized that whole thing will now move up just exactly opposite to the reverse bias, so this will be now like that and this will go like this. Let me just draw that bit, like that go up (Refer Slide Time: 46:33). So EC will go up from thermal equilibrium. EV also will go up and I can draw the Fermi level bit up there that is a new diagram. What happens to the energy distribution? Originally it was like that. Please understand dotted line was originally there. I do not want to repeat now. So when you apply forward bias V, the whole thing will get shifted by an amount equal to V

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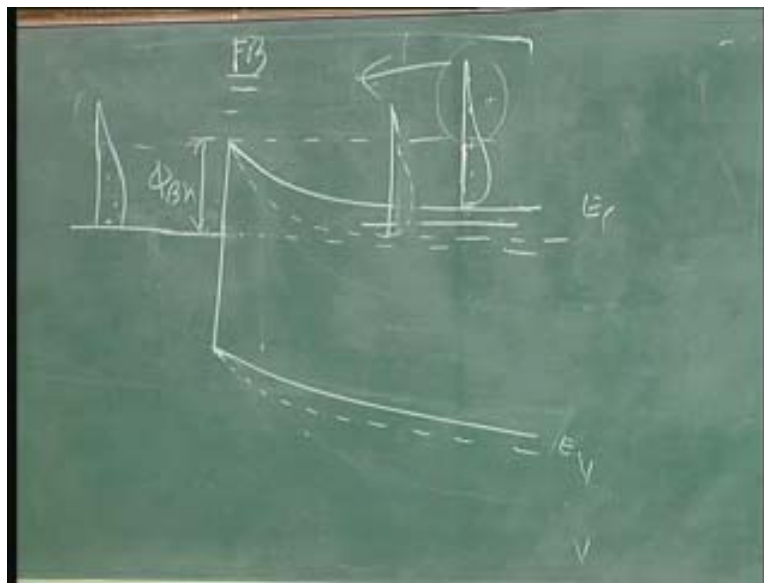
So, the barrier will reduce by an amount V forward bias. So, what will happen to this distribution? What was like that? This distribution that will become like this now; same thing but it has gone up. That means originally these were balancing each other, thermal equilibrium. Now, since the potential energy has gone up here, more number of electrons have the energy across the barrier from right to left, more number of electrons have come across.

In fact, the electron concentration goes up exponentially as the voltage by V by V_t, that we will see it little later but it is known that the carrier distributions vary from Boltzmann's law as proportional to E to power of E by Vt. So if I increase the voltage here, the carrier concentration go up as E to power E by Vt once which have energy above this. So that means actually you have the current which is flowing from right hand side to left hand side. Due to the transfer of electrons from the semiconductor to the metal I have put it as I_{SM}. The symbols I_{SM} means the actual current flow direction due to electron transfer from semiconductor to the metal. In order to avoid confusion I have put the arrow as actually the actual direction of current and I have put it in the metal. The I_{SM} I have put in the metal region because the electrons which have got transferred on to the metal which give rise to current in the metal I_{SM} that current will flow through semiconductor also and I_{MS}, what is I_{MS}? Current due to electrons which can cross the barrier from metal to semiconductor that does not change that does not change because that remains the same thing. So you have I_0 due to transfer from here to here and I_0 into E to power E by Vt due to the transfer of electrons from there to there. It is I_0 into E to power E by Vt because the carrier concentration has gone up by a factor E to power E by Vt. Quantitative � will do later so that is the thing. So this is I_0 and this quantity is I_0 into V by Vt.

So, net current flow is from the metal to the semiconductor which is actually equal to here. Net current is due to I_{SM} in that direction minus I_0 in other way I_{MS} in other direction, so that is what is put here. So, we have got this equation governing the metal semiconductor contact. So to see it once more, thermal equilibrium I_0s are same. Reverse bias, the electron injection from semiconductor to the metal goes down, barrier is increased. So the current is only due to the transfer of electrons from the metal to semiconductor I_0 and the direction is semiconductor to the metal because this side becomes positive. So the current flow in that direction.

When you forward bias in the case of n type semiconductor; metal is positive, semiconductor is negative. Just like pn junction, p type region you make positive. Then I_0 from here is not changing but the other one is increasing. As a result, you have got the current like that like exactly like the diode, but the I_0 that we are talking of in the case of

metal semiconductor contact is will be different in magnitude compared to the I_0 of the pn junction. That makes all the difference. So you can see that, reverse bias it blocks the current because nothing is there control by I_0. Forward bias it allows the current to flow because lot of electrons are available to cross.

Now let us see I just rewritten whatever I have been telling so that you can have it here I_{MS} is current due to the electron flow from metal to semiconductor which is I_0 fixed for all the bias.

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I_{SM} is current due to the electron flow from semiconductor to metal which is I_0 into e to power V by Vt. When you forward bias, of course we are talking of forward bias that is much large compared to I_0. So that current is I_0 into e to power V by Vt minus 1 and the direction is from metal to semiconductor. When you make actually V, when you reverse bias that V made is negative and then this turn goes off and you will get I_0 you put minus because you are putting the direction of current like this. When you write this equation; you write V as metal positive and the current direction as current entering into metal as positive. So, when you reverse bias that, that becomes minus I_0 telling you that current direction is reversed. This is the key thing what we have started. So, if you take a look at the equation of that metal semiconductor contact, I have drawn two characteristics, metal

and n type semiconductor and I have marked it here, the diode and IV polarity, I is in that direction

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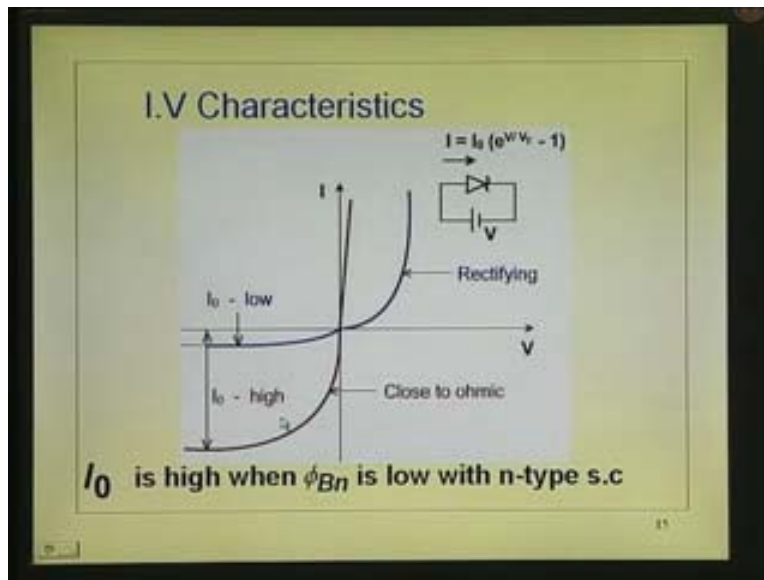
So, this is the I_0 e to power V by Vt minus 1 and this is I_0. If I_0 is large how will the characteristics be? That is this one. I_0 is large means the whole thing comes down here. What happen to the forward characteristics? I_0 is very large with small values of V, I get the same current. So the entire things move like that, the characteristics. Now, it tells you the entire information that you are looking for. If I want to make a rectifying contact, I must have a pn junction or a metal semiconductor contact whose I_0 is very small. It will block the current in reverse direction. If I want to make an Ohmic contact, I must have a metal semiconductor contact which will have I_0 large. When will I not be large? (Refer Slide Time: 54:00) That must be small

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If I have a device or a metal semiconductor contact with a low barrier rate, I_0 will be large that will ohmic and what is that phi_{Bn}. In fact, these all we have just said orally in the discussion now that is I_0 is that and V is negative, it is minus I_0, all that. So, you need for ohmic contact I_0 should be very high that is what we saw.

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Now let me just go back to this curve and discuss before I wind up everything. So, ultimately what we are talking of in the case of n type substrate. We will talk of p type

substrate in the next lecture because we cannot cover that. So here what we want to make is ϕ_{Bn} small for ohmic contact so that that is large and ϕ_{Bn} actually is governed by (Refer Slide Time: 55:04) ideally that is the situation. So, I must choose metals appropriately so that ϕ_m minus chi is smaller. So generally people say the ϕ_m of the semiconductor, ϕ_m must be large compared to ϕ_s. What matters is the difference here between ϕ_m and chi. Smaller it is, closer it is to the ohmic contact. Larger it is, closer it is to the rectifying contact.

So, we look for to it is seeing what type of impact these metals really have in making ohmic contact and rectifying contact. We also will see in the case of p-type material what will happen? In the case of p-type material you talk of ϕ_{Bp} rather than ϕ_{Bn}. So, if ϕ_{Bn} if I increase, you get rectifying in the n-type material. If I increase ϕ_{Bn} what happens to $\phi_{Bp,}$ it decreases. In p-type sub state exactly opposite to what we see. You must have if ϕ_m is large in the case of p-type material that will become smaller, so this becomes larger. So we will have ohmic contact there. That is all we have want to see. I think more about this thing we will see in our next discussion with energy band diagram for p-type material and today, we will stop on this discussion.