High Speed Devices and Circuits

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Lecture - 11

GaAs and InP devices for Microelectronics

We have spent about ten lectures on seeing the various aspects that are first, required for high speed circuits and then devices. What we arrived at is that we need devices or materials which should have high mobility or high velocity.

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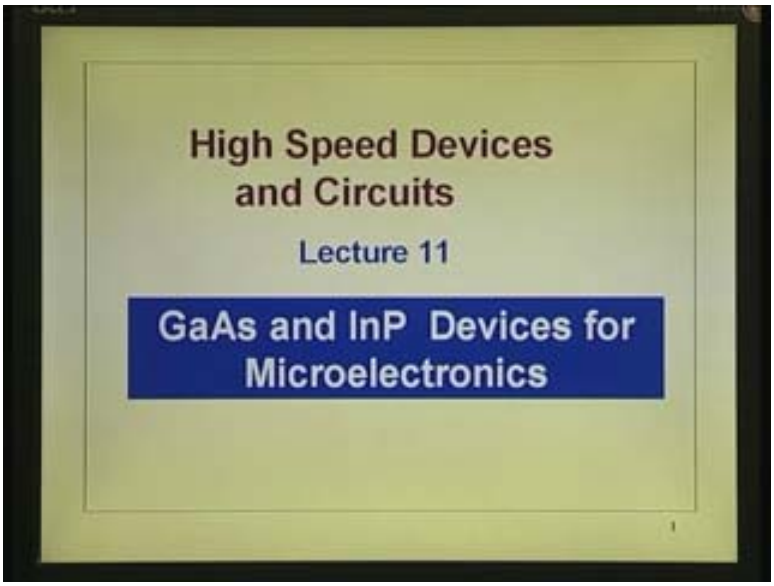

We compared the various materials. Finally, we came up and said that gallium arsenide and indium phosphide are the two materials. This is because of better mobility than silicon and better band gap than silicon; both put together. Then, we saw the dopants in these III - V compound semiconductors from second group, sixth group, forming acceptors and donors. Fourth group behaves in an amphoteric way, but mostly going to the gallium side and indium side.

Then, we took a look at another aspect, that is, the semi-insulating material which is important for high speed circuits. Then, we can integrate the devices on a semi-insulating substrate, so that, the rooting capacitance can be reduced. Theno, we saw how to realize layers on the top of the semi-insulating substrate at once. So, that is the ‘epitaxial layer’ which ultimately will be the one which we use for making our devices.

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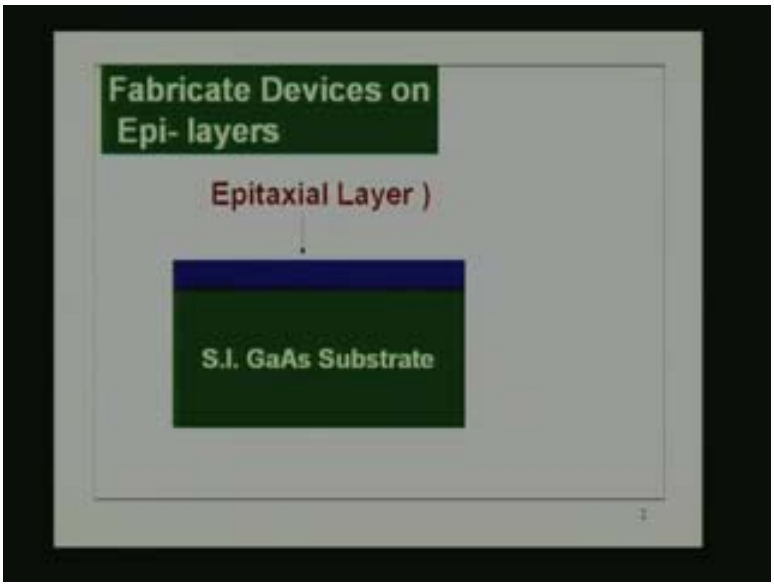

Now, when we want to make the devices integrate to circuit, what you need is not merely the ability to make device. You must be able to isolate the devices from one another in integrated circuits. For example, in case of silicon integrated circuit, very popular technique is pn junction isolation. When you want high performance, there also we go for semi-insulating substrates.

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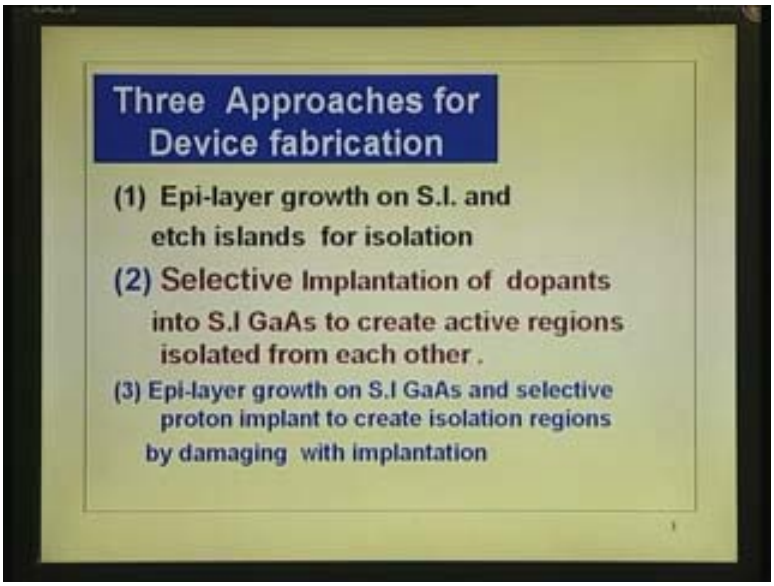

Now, let us see what are the methods which are used for isolation in gallium arsenide base mainly. Very popular techniques are the Epi-layer growth on semi-insulating substrate and etch islands for isolation. I just go into that, it is very easy to understand in the form of figure; semi-insulating gallium arsenide wafer cross-section and on the top of that, grow epitaxial layer, mostly n type layers are grown. This is because n type materials are used for devices which operate on the transport of electrons.

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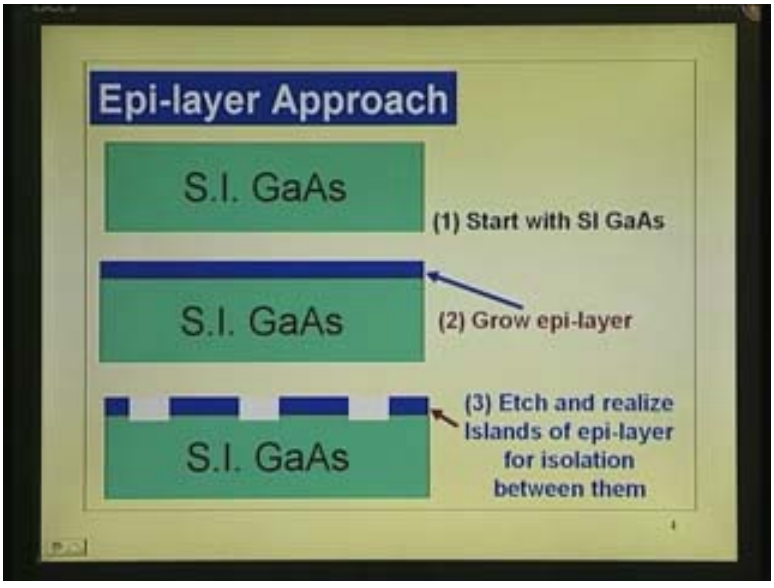

Then, using a photolithographic technique and etching, you remove the materials from these portions, so that, each one of them is isolated by the other one. Each one is an island separated by this gap. This portion which is connecting them is semi-insulating, it is not insulator but semi-insulating. Therefore, the isolation between these two layers is very good. Now, you can make one device in each island. Put them together, so that, they are isolated from each other. This is the first method which is very popular. Sometimes, people may object to a structure like this, because the wafer top surface is not planar. It is varying like objectionable, if this layer becomes too thick.

If it is say, 0.5 micro ohm of that order, we do not have to worry much. This is because that step anyway, you get in the oxide itself in silicon technology. However, even there, when you want to go for more and more packing, reduce dimensions. Then, you do not like these ups and downs at all. You have to do some _____(5:23) techniques. Here, there is a totally different approach. The second approach is selective implantation of dopants into semi-insulating gallium arsenide to create active regions isolated from each other.

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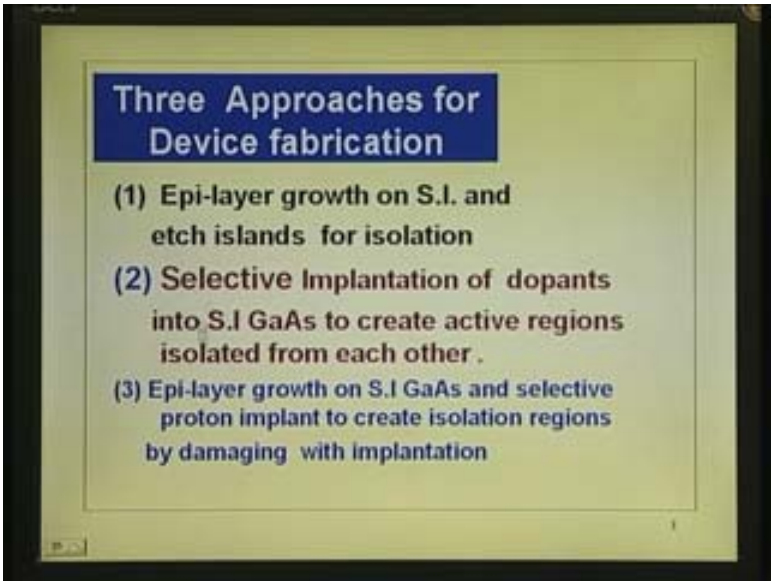

Let us take a look at the diagram which is the second approach, what we just now read. Semi-insulating substrate masks all other portions except these regions that are these arrows where we implant n type impurity in our silicon.

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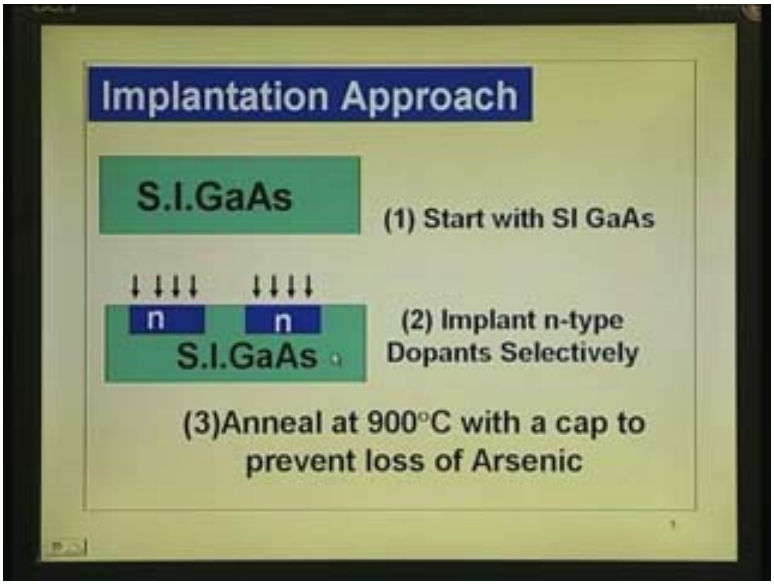

When you do implantation, you have total control on the number of atoms that we are putting there and we can virtually count by measuring the current. In implant, there is a beam current. So, if you implant for 10 seconds, i into t gives you total charge, divided by q gives you the number of atoms that you have implanted. The atoms come in the form of ions but when it comes and implants on the wafer, the path for the beam is in the interlaced ionized path

But if it is neutralized, it does not remain as positively charged; it is neutralized by electrons coming from back door. So, current flow is like path complete. So, you have the electrons coming and neutralizing them. What you have finally? Even though you are implanting ions, what you have finally is the atoms themselves neutral. This is one question which sometimes comes in mind, that is why, I just mentioned that its electrons coming from backside. So, you have this n region which is implanted and each one of them is isolated by this perfectly planar. You can put oxides in between or dielectric layers in between but that may not be necessary at all in this case.

This is because, this is semi-insulating material and it is a very popular technique. In fact, you do not need any other equipment virtually because you have the implant or you can implant whatever you want. One single machine can do implantation of Beryllium in the case of silicon, phosphorous and so on. Here, you can implant silicon or sulphur and whatever you want, you can implant. So, same in the single machine by controlling a path of trajectory of the implanting ions, but the mass is different that governs the voltage and the path. So, we can choose particular implanting species at a time, of course, you can implant only one. But, after choosing the material, you have to make certain adjustment, so that the particular curvature is the path to be followed. I want to go into details of implantation. So, that is more involved into and may be couple of hours we will need for that. Let me skip that. But, general idea seems than these ions. You get planar structure. Now, the story is not over there. We implant the dopants selectively here and leave it; you do not get anything.

Because, this implantation is done at particularly implanting with gallium arsenide; you need high energy. Implanting onto silicon, it requires certain energy. It requires more energy to implant at a certain depth because silicon is lighter compared to gallium, arsenide gallium and arsenide atoms. So, when you have the host atom coming in, it will lose its energy with each collision and it will not move forward. If you remember the particle dynamics, m1 and m2 product is the one that the energy is proportional to product of masses and energy transfer with these collisions. It is like elastic collisions or inelastic collisions, atoms coming and colliding depending upon angle. While maximum energy is on, then head on collision is there. So, that is proportion m1 m2. That is why, heavier masses, you lose energy and on deeper implantation, more involving. So, higher energy implantation systems are used for gallium arsenide implantation. Now, because of that as I said now, when implantation takes place, the guest is not kind to the host. This is because, it has lot of energy and it knocks out host atoms from the lattice.

Once that is done, it is damaged thoroughly, this is number one. Number two: these atoms which are implanting do not go and sit in a place where it is supposed to go and sit. It is supposed to go and sit in the lattice. It will go and sit, wherever the space is there. It is testacies. So, what you must do to recover the damage and also to recover the dopants

which we have implanted into lattice sides? You have to give some energy. After all, the tendency of the crystal is that crystal structure that we have discussed. Why the crystal structure is there? That is the minimum energy which takes to occupy that position. Anybody will take minimum energy position, if you allow. So, many are the crystal atoms. Now, if bombarding atoms have knocked them out from lattice to push back to the lattice side, what should you do? You give some energy for that to go back to natural side, that is, thermal heating.

So, you have the heat in this case; annealing at temperature like 900 degree centigrade to remove and recover the damage and also to recover the dopants into the lattice side. You cannot think of annealing, silicon annealing will not care; 900 is okay. That is perfectly alright. There is no problem because the vapor pressure of silicon is very low and will not lose. In the case of gallium arsenide, we have got two species: gallium and arsenide. I keep on repeating this and reminding you that this is a compound semiconductor with the two elements which have different vapour pressures. You tend to use more of arsenic. So, we must put a cap. That is what is meant by cap. Say, you must put the cap on the gallium arsenide surface. That is, put a cap of dielectric material preferably, the nitrites or phosphosilicate glass is supposed to be a very good cap. So, we put the cap on the surface to prevent the loss of arsenic or you can use some arsenic over pressure during annealing.

These are the tricks which are done to prevent the loss of arsenic. So, you must remember this one. Again, it is not over just by implantation. It is the beginning of the whole thing because you have to anneal and suffer from the loss of arsenic unless you take care of it. Then the third method which is done is again epitaxial. See epitaxial layer when you grow, their benefit is you can get a nice layer. When you do the implanted layer, the doping profile is not uniform and it has a drowsing profile. There are damages which are created; you have to recover. However much you recover, there are some damages left out. You cannot go to 1000 degree centigrade and all that, for annealing.

So, what people do is, there is another approach which is used. That is, epi-layer growth on gallium arsenide, semi-insulating. Instead of selective dophite implantation which forms the active region, you implant or you create the isolation region but damaging the

implanted layer. At the diagram, it had been very clear that diagram semi-insulating gallium arsenide, epi-layer step is same as the first one. There you were etching and now instead of etching, what you do is, you implant proton.

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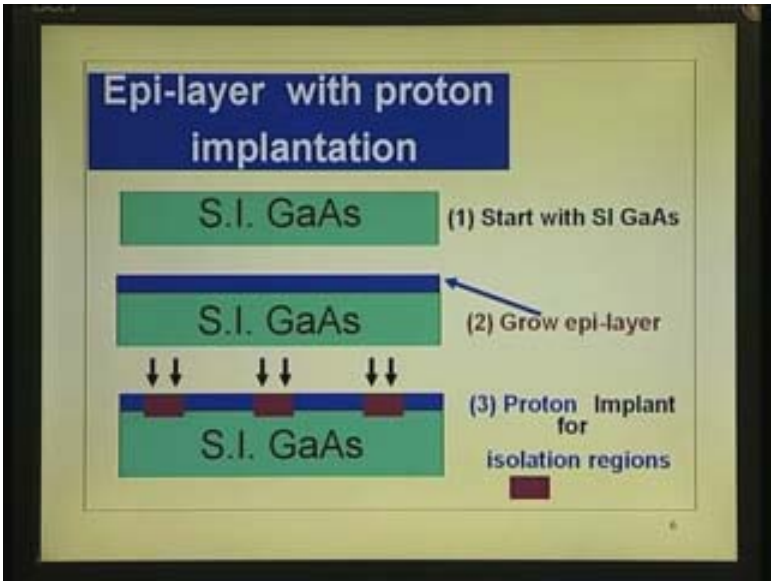

100 kilo electron volts will give you a micro proton implantation. Proton is nothing but, h plus. h plus ions you implant, implantation energy is from 100 kilo electron volts right upto 3 million electron volts depending upon how much depth you want the damage to take place. So, those atoms actually what they do is, they are damaging the region. If this region is damaged, whatever dopant was there in that epi-layer is knocked out and total chaos is virtually amorphous, not even polycrystalline. That has got very high receptivity. In fact, these in between regions, we can turn them into regions where the carrier concentration is something like 10 to the power of 11 per centimeter cube. That is virtually semi-insulating. So, we can get 10 to the power of 11 electrons per centimeter cube; that level, you can go bombarding with proton.

Do not think of annealing it now. If you anneal it, we need to have much higher temperature. Then, you have to recover and the epi-layer will come back. So, do not anneal it; you bombard it though temperature will not too much. So, these are the three different approaches used. Very popular technique still is this. This is one type of

implantation species which are used. In India, for information for all of you, there is one company called GAETEC gallium arsenide technology in Hyderabad. There they make MMICs Monolithic Microwave Integrated Circuits for giga bit logic circuits. Gigahertz frequency range is done mainly by implantation. I am not sure whether they use proton implantation also. But they do not have epi, so naturally, they do not use proton implantation unless they import epi-layers and do the thing. However, this is implant to do this particular aspect and definitely I know that the one of the projects they have used. They have made devices mainly for defense applications. Now, we know how to make these layers isolated from each other on the semi-insulating substrate, on which you can make the devices. What are the devices that you will make on that?

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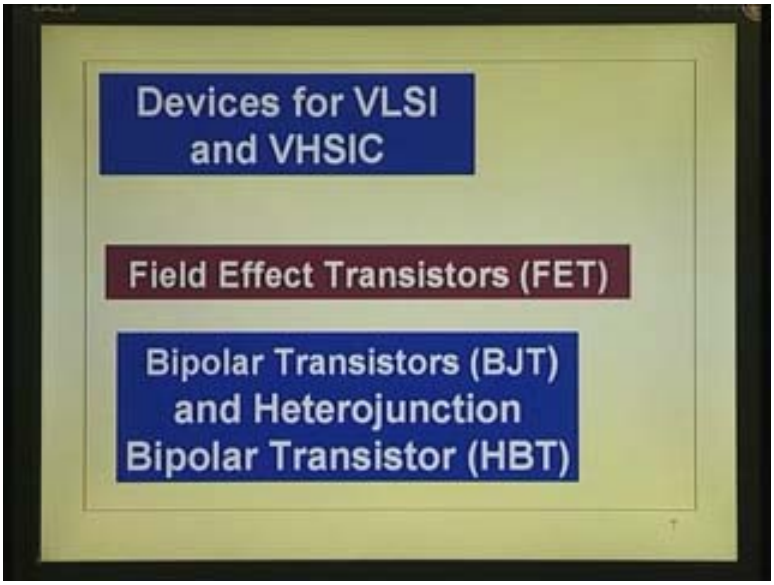

If you think of your silicon guy, you will immediately tell a MOS; MOSFET and Field Effect Transistor. At least, one will say Field Effect Transistor. Today, the MOS logic is dominating, that is the CMOS logic. So Field Effect Transistor we will say, the other devices which are used in circuits like: emitter coupled logic or some linear circuits or the bipolar transistors. When you have the ability to grow Heterojunctions with III - V compound semiconductors with turneries and you can have Heterojunction, Heterojunction Bipolar Transistor (HBT) very popular in III - V semiconductors. It is not really III - V, it is IV - IV silicon germanium with silicon and you make HBT. All that

you need to do is to make the emitter region with the wider band gap compared to the base region. So, there they will have silicon germanium and base silicon emitter because after you know that germanium band gap is smaller than that of silicon. So, silicon germanium will be somewhere in between; that is the base. So, HBT will have ample occasion to discuss these things during this course of our discussion. Now, let us see Field Effect Transistor were might say, we can see options open up, MOSFET Metal Oxide Semiconductor Field Effect Transistor; whereas, they are very popularly known as MOS Field Effect Transistor. You would like to do that.

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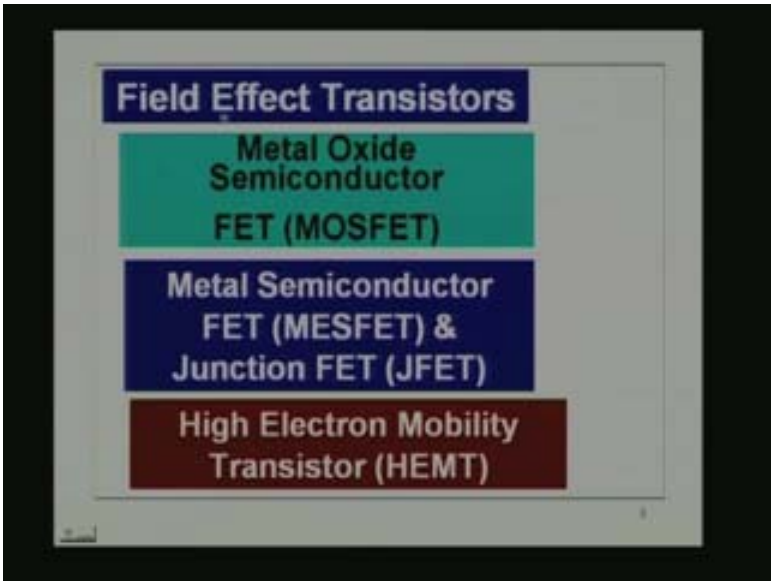

Since, that has a success story for silicon. Do you like to do that in gallium arsenide? That is the question, then Metal Semiconductor of Field Effect Transistor (MESFET) where metal – ME, S for Semi conductor and FET for Field Effect Transistor. However, Junction Field Effect Transistor is JFET. The moment you say FET, there are three options: MOSFET, MESFET and JFET. Which one will you choose? Choice depends upon your ability to make those devices. The other one, of course, which is completely proprietarily of these III - V semiconductors is HEMT, High Electron Mobility Transistor. People call this by several names: two dimensional electron gases, FET, TEGFET that is another name jargons are enough; flown out that you too. But, very popular name is HEMT because it tells you what to get out of that. You get electrons

which have high electron mobility. Now, let us go to ask our serves among these FET's. Can MOSFET be realized with gallium arsenide and indium phosphide?

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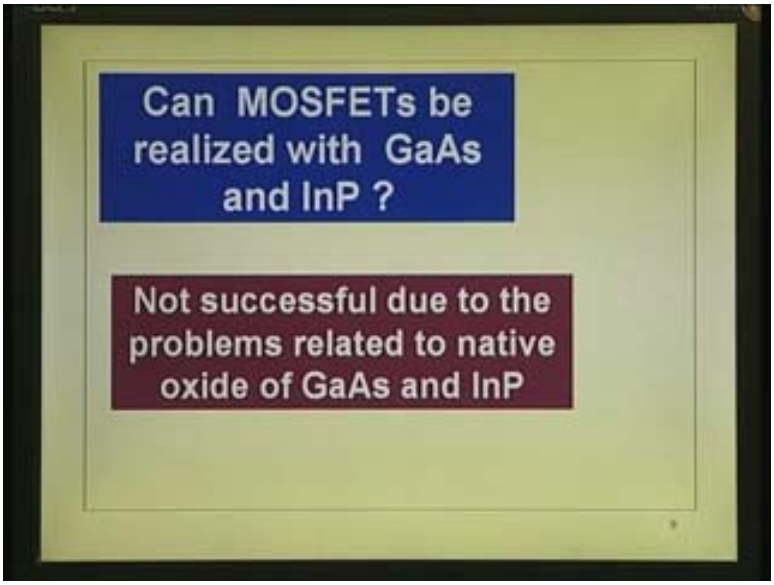

The answer is straight forward and not been successful due to the problems related to native oxide of gallium arsenide and indium phosphide. What is native oxide? Native: you convert that substrate into its oxide, it is native oxide. Silicon, SiO_2 is native oxide. Whatever way you do, it need not be thermal oxide. Just convert that silicon into silicon dioxide which is native oxide. If you convert silicon into silicon nitrite, it is the thermal process and that is the native nitrate. If you deposit nitrite, that is not nitrite; it is just deposited nitrite. Silicon dioxide also can be deposited by plasma enhanced chemicals deposition by break, cracking, filing, and making for forcing it to react with oxygen, you get SiO_2. That is deposited and that is not native. Native is true conversion. Now, the success story with silicon is, you have been able to get the oxide using native oxide. Just to make it more where why I want to bring it out is, you will have a p-type material and then, you can see everywhere you have got these.

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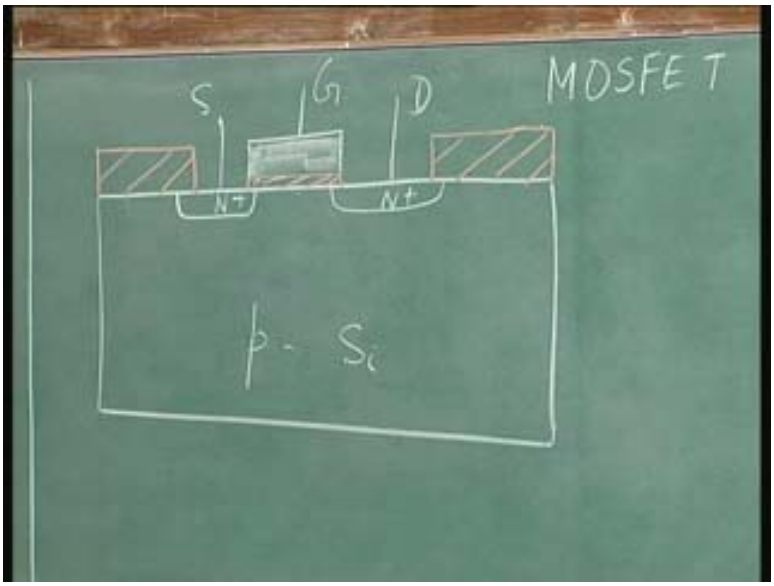

I will show one device which you all are familiar. There you got the native oxide, red colored one that is field oxide. So, for silicon, silicon dioxide; this is silicon. Then, you got a thin oxide which I am putting it here after all the lithography and everything that is the gate oxide. Then, you have this gate and then you have this for completeness sake and I am drawing this. Find that I am trying to make out is, you have the source, you have the drain and you have the gate that is the MOSFET. What are we looking here? We are getting different performance because of this oxide. The entire is successive because the interface between this oxide and silicon is very clean. The charges in the oxide are less, that is, it is close to the ideal insulator; not exactly ideal. What is an ideal insulator? That means, zero charge within that and a very clean interface, there is no charge which is staying at the interface. That is out of here.

So, when you say due to the problems related to native oxide of gallium arsenide indium phosphide, the problem related to this property of this oxide and the interface first time, when they made MOSFET. I think, you should know the story behind how the transistor was invented. Shockley Brattain invented transistor; it was not deliberate. In the sense, it was sort of accident. They were first to find the first device that we are supposed to MOS, the MOS Field Effect Transistor. What are conceived was: you put a dielectric material, they were trying germanium, put a dielectric material and on that put a metal gate on the

top and then you must be able to control the region below that. By applying voltage between these two, we can control the regions between these. For example, if we apply plus, we can deplete; we apply minus, we can accumulate plus charges. That was the idea but when they made the devices like that, it never worked and not even a sign of current flow. Immediately, Bardeen came up with the theory that the entire problem is due to the interface between the dielectric that we have put, it is just dielectric which is deposited and the substrate. That was the theory characterized by a parameter called 'interface states'. These are all relevant for our discussion.

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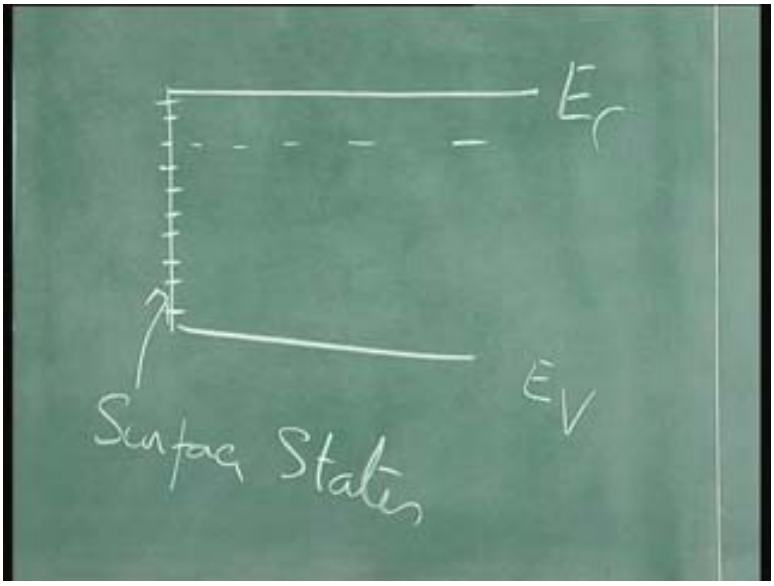

When you put conduction band and valence band, if I have a level here like this that is only one level only throughout this bulk material. But, if I have levels like these continuous levels, this is surface and those are here. We can see one level there which can create havoc in a performance of this particular device either beneficial or not beneficial. One layer you put, donor level it donates electrons. If there are many levels, what will happen? For example, if you take a free surface of semiconductor, how many atoms will be there per centimeter square? There will be almost about 10 to the power of 15 per centimeter square. Then, how many states will be there? As many states will be there, many into two: spin up and spin down, if you take. So, those are the states which are

present. Those states are represented here. I will come back to this again later when we discuss about the circuit barrier diode. So this is the idea and that was the problem.

You put a deposited material, you have a problem. You grow a thermal oxide that was auto diode immediately. In fact, the transistor was invented because when they said there were surface states here, these are the surface states. If it is in the free surface, you call it as surface state. If it is between oxide and silicon or between a dielectric and semiconductor, you call it as interface state. It is the same. These interface states are the problems, when they try to make these transistors. Now, they were trying to analyze, when they were analyzing that what they did was, may be it was with one of the sentences I mentioned to you, n type germanium was there and they put a probe onto one end. They applied the voltage between the substrate and the probe. I do not know whether you had heard the story before. If you are not, just try to spend on this.

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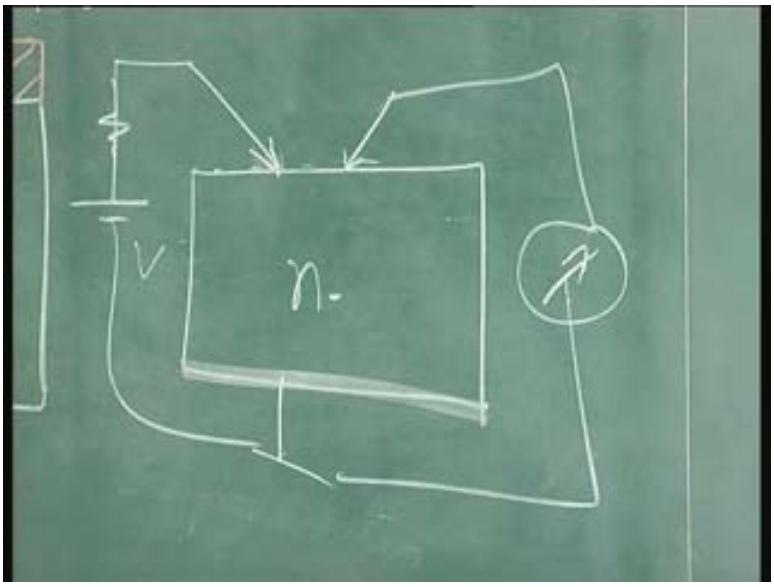

They put n-type germanium. Then what they did was, they put a contact here on the back side and then they put a probe. Heat it locally; it becomes a sort of pn junction like a point contact diode. In old days, all detectors are point contact diodes and that type was this. So, this is actually like a p-type material. Then, they apply a voltage between the two. To get a small voltage, they put a resistor in series at least current. Now, this is a

surface. What they theorized was that there is a potential distribution on the surface due to the potential established here. So, they are trying to probe emitter, this is a very interesting story that is why I am just telling you as how things have come up in the transistor. They were moving this probe and seeing whether there is any current. They want to see whether there is any current. So, they found that when you move here closer and closer, there the current increased. Then, they found in various efforts, there is a current change. There is a pnp transistor, emitter base collector.

That came because of the desperate study on this MOS device. Now, it is very short. I am sure they have spent months together doing that experiment and trying it out. That is what happened. That is the whole benefited industry is electronics industry because of that on this surge. Now, we will praise Shockley, Bardeen and Brattain. I think Brattain is still around but Shockley and Bardeen are no more. So, this is the idea. Now, let us see. So, in a free surface, problem is there in a deposit oxide and there will be still problems. If it is thermal oxide, problem is not there because those interface states. After all, what are those surface states due to? The atom within the bulk is surrounded by 4 neighbors. When it comes to surface on top surface, it is 1, 2, 3; 3 neighbors and there is no neighbor up. So, there is a tangling bond. Tangling bond is the one which gives rise to such levels. To put it in a very simple way, any loss of periodicity gives rise to a level. If you add impurities that are loss of periodicity gives rise to a level.

You go to a surface, loss of periodicity that gives rise to such multiple levels because that is a two dimensional affair on the surface. So, you get those levels because of that. Now, you oxidize that surface with a good native oxide, do that those tangling bonds have saturated this oxygen and silicon oxygen bond. Immediately, you do not have the tangling bonds and we removed those levels which I showed you. Minimize them and there may be 10 to the power of 15 per centimeter square states on surface, if you take bare silicon semiconductor. You reduce it by oxidation in the case of silicon and you are able to get down to 10 to the power of 10 of that order. If not, 10 to the power of 10 even in poor presence liberty, you can get 10 to the power of 11 today. By intend was 10 to the power of 10 you can get then we turn of course, quite bit more involved. So, we get down to that level surface states in silicon, gallium arsenide those problems are there.

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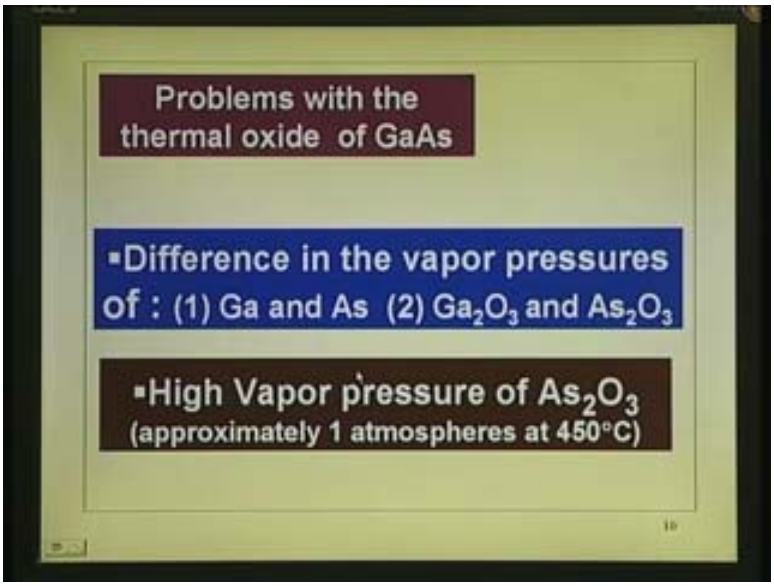

What is the reason for that? We will see first quickly run down to that. So, what are the problems related to native oxide. Thermal oxide or gallium oxide after all, if you succeeded with silicon with thermal oxidation; why not gallium oxide and thermal oxide? Put it into furnace, remove it and see what happens. Problem is multiple and you now have not only gallium and arsenic which have different vapour pressures, you have also arsenic trioxide and gallium trioxide. Gallium trioxide and arsenic trioxide, those also have different vapour pressures. So, you have multiple problems. Arsenic trioxide has approximately high vapour pressure. Arsenic, when you oxidize, arsenic trioxide has got a vapor pressure of one atmosphere at about 450 degrees centigrade which is tremendous.

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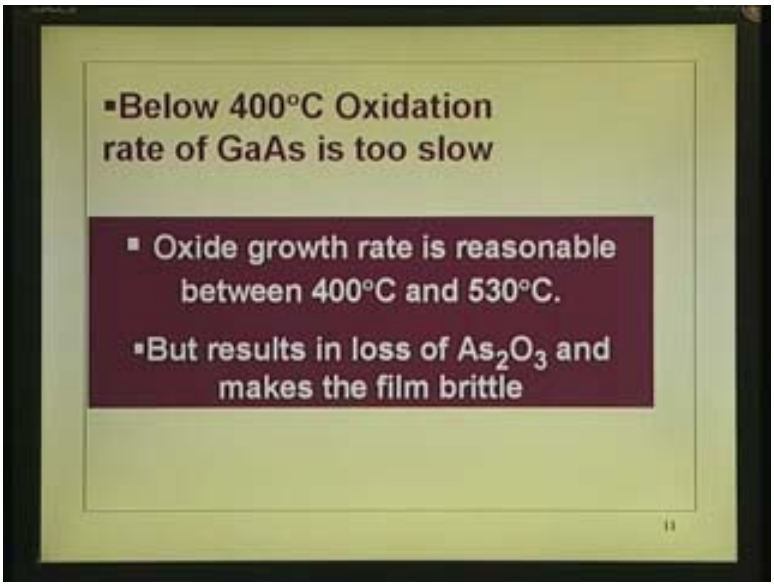

That means, if you oxidize gallium arsenide, oxide growth rate is very slow that is below 400 degrees centigrade. So, you have to oxidize at temperatures from at least 400 to 530 degrees centigrade. I am giving 530 because this is the number that people have been using. What we are trying to see is where this hurt does? It would hurt, if the temperature is high. If you are able to do the oxidation at lower temperature, you would have got it. But the oxidation rate is very slow at temperature below 400 degrees centigrade. So, they would try 450 to 100 degrees centigrade to deoxidize. They got reasonably amorphous oxide but result is as you grow oxide, arsenic trioxide and gallium trioxide, both of them grow and you lose arsenic trioxide. So, you end up with gallium trioxide alone. There is a non-stoichiometric oxide that particular oxide is brittle and also it is leaky; its band gap is low and not as high as silicon dioxide.

What is the band gap in silicon dioxide? 8.8 electron volts, you might lower them; some like 4 or 5 electron volts. That is why film is brittle and leaky, if you make brittle, then there may be force surrounding that because of cracking. When there are cracks all around if you put a metal and you know it is a short circuit. That is why this is one of the problems that you have got in hand. Now, people try to overcome that problem. Let me just go back to this one more. So, you have one problem which is the loss of arsenic trioxide. Now you will say, I will control that by doing the oxidation in arsenic vapor

pressure or arsenic trioxide vapor pressure. Put it in a sealed tube on one end of the tube, you put arsenic trioxide and oxidize it.

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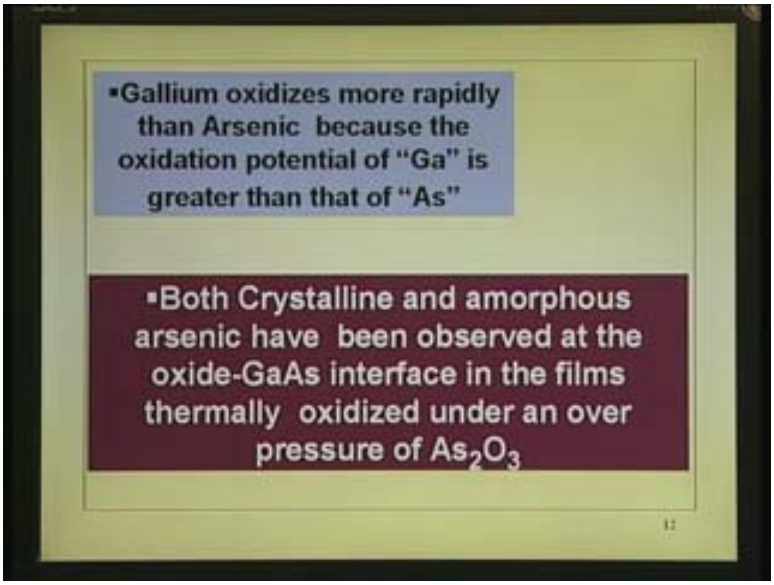

You do the oxidation but when you examine that what they have seen is both crystalline and amorphous arsenic have been observed at the oxide-gallium arsenide interface. Two things happened; one is it oxidizes; you prevent loss of arsenic trioxide. But, your bulk oxide is good; you have got stoichiometric gallium trioxide and arsenic trioxide. You probe using electrons flow, you see that. You go right up to the interface at the interface; you see amorphous arsenic and also crystalline arsenic. The time is for the crystalline, that means what you have is a layer here. If I have gallium arsenide here and if I oxidize it like this with arsenic over pressure which I thought is the solution for the whole thing, you will get arsenic at the interface.

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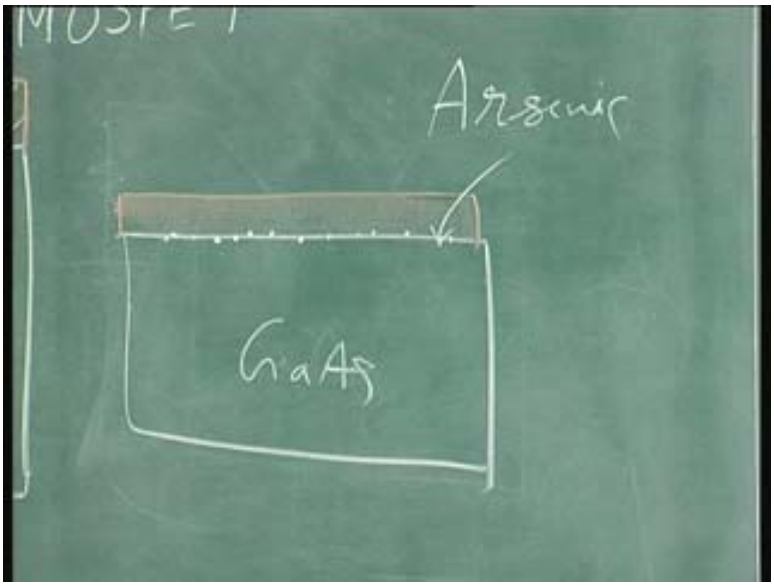

You get arsenic, the reason stated there is when you oxidize then gallium tends to oxidize better compared to arsenic. We cannot get into more of chemistry for that. Simply, we can say pretty that in gallium and arsenide, the oxidation potential of gallium is higher than that of arsenic. Therefore, its ability to oxidize is better compared to ability to oxidize arsenic. So, your gallium arsenide and if arsenic gallium oxidizes, arsenic does not oxidize and what are we left with? That is arsenic, you see here and that is arsenic that you get at the interface. That is real bad news. If you have arsenic as your interface, not because it is poisonous for you, it is because it is like putting a metallic layer between that. If elemental arsenic is present there and it is like a metal layer. What will be the result electronically? Levels not even loss of periodicity, you have just arsenic sitting there is our extra interface densities. So, high interface densities are observed because of this excess arsenic at the interface. These are the problems which people faced. Now as a result of that, you can see whatever I have said and I have put it here, so that, you have to write black in white or white in red. The presence of arsenic at the interface is due to or it is a cause of high interface state density. It is due to arsenic, you get high interface densities in gallium arsenide MOS devices with native oxide.

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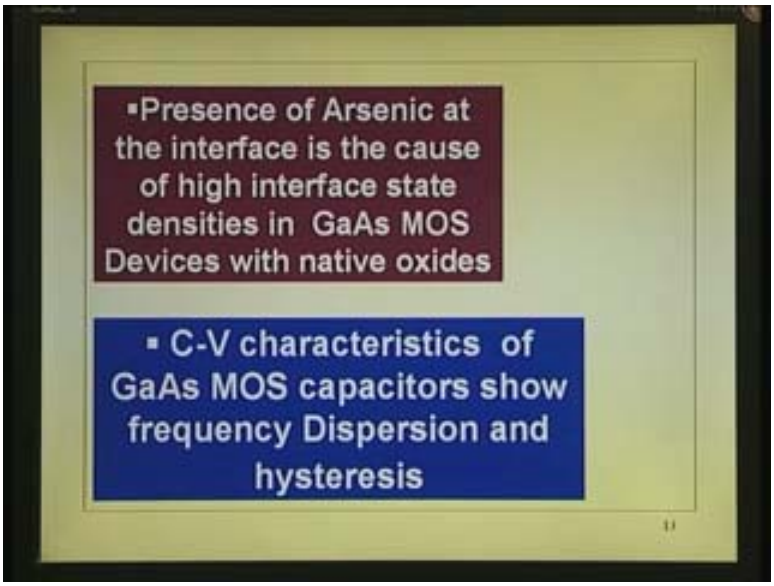

Now, you will say, thermal oxide is bad because of high temperature and so on. Why not I go and do; these are the themes people were following in 1980s. 80, 84, 85 if you see, they drag out the paper and they said we have got the room temperature. Do the oxidation at room temperature. How do you do oxidation at room temperature? Anodic oxidation, dip the gallium arsenide in an electrolyte. In fact, it is water, OH. Use the OH ions for oxidation of gallium arsenide. Put two electrodes dipped into that while all that you need is: take a beaker and put the electrolyte which contains OH. In fact, H_2O virtually or you can take ethyl alcohol or things like that which contains OH.

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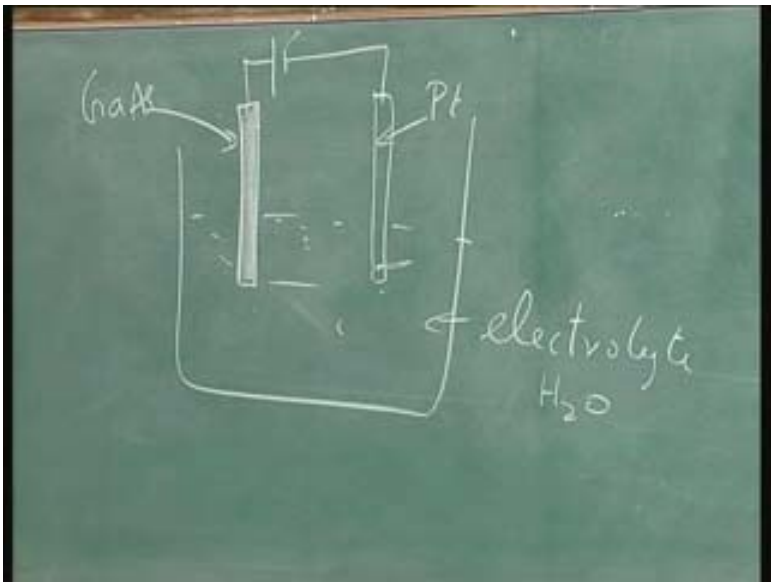

Then, dip your electrodes and you make this gallium arsenide. This is platinum and makes that positive, make that anode. That is why it is called anodic oxidation. You make the sample which you want to oxidize as anode which is anodic oxidation. Reverse the polarity and there will be etching. So, this is the one when you do that. These OH ions actually get into this surface, reacted with gallium and arsenic to get gallium trioxide, arsenic trioxide, fumes of stoichiometric oxides. No loss of arsenic trioxide because of room temperature. No loss of arsenic trioxide but the interface you can guess. Interfaces contain arsenic because gallium oxidizes better than arsenic. So, you have recommended arsenic.

Now, people said that arsenic is there; so I do not have any problem and I can drive it out by slightly raising the temperature. This is because, it is more volatile. Now, what happened was; in the process of annealing, what was there on the surface started becoming crystallite? People observed afterwards that there are crystallites of arsenic which is actually a still bad news. They never got good C-V characteristics. The C-V characteristics in thermal or this oxide was so frequency dispersion and hysteresis. What is the meaning of these two? Let us just see that before we go into many other things. In fact, talking of these thermal oxides, in the EEE department also we have done some experiments way back in 1986-88 in that range using high pressure oxidation. This was

the PhD thesis of one of my students who is a faculty member in the EEE department, Nandita Das Gupta.

She did on high prior oxidation of gallium arsenide and got some good result. However, it is not comparable to that silicon. All that you get is some publications out of it who thought well than that. But, at that time frame, that was one of the best oxides that have been available. People have sorted out the problem in different ways and they go to HBT, we will discuss that. They have sorted out problems that we have subsequently. A PhD came out in our department with emersion using that approach. That is into 1998; that also we will discuss later. Now, what we are trying to tell is the capacitance versus voltage. That is one of the most important diagnostic tools for evaluating the oxide like a Metal Oxide Semiconductor. Do not act like transistor.

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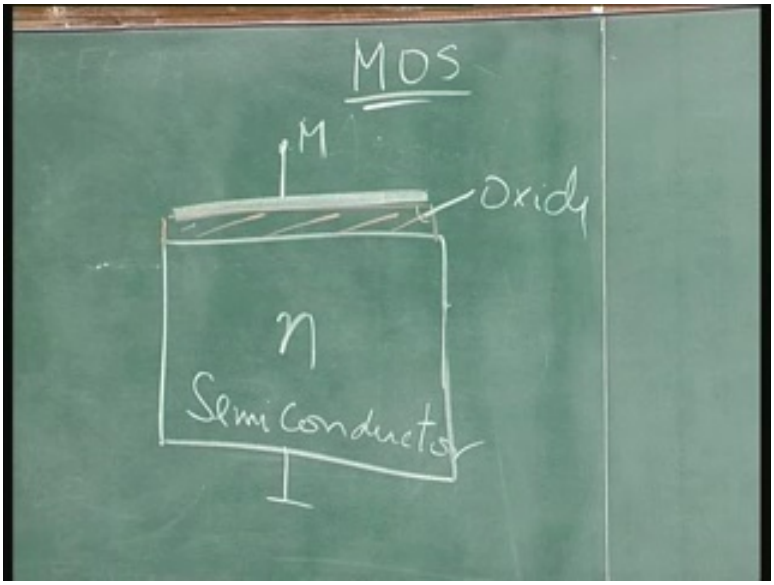

Take the n-type region and have an oxide here. Then, put a metal. So, Metal Oxide Semiconductor that is the MOS structure, MOS capacitor. MOS capacitor is this one. This is n-type substrate. If I apply plus voltage, negative charges will be accumulated on surface. Capacitor is in the exact side of oxide. So, when we apply plus voltage, ideally that will come flat because of capacitance of the oxide.

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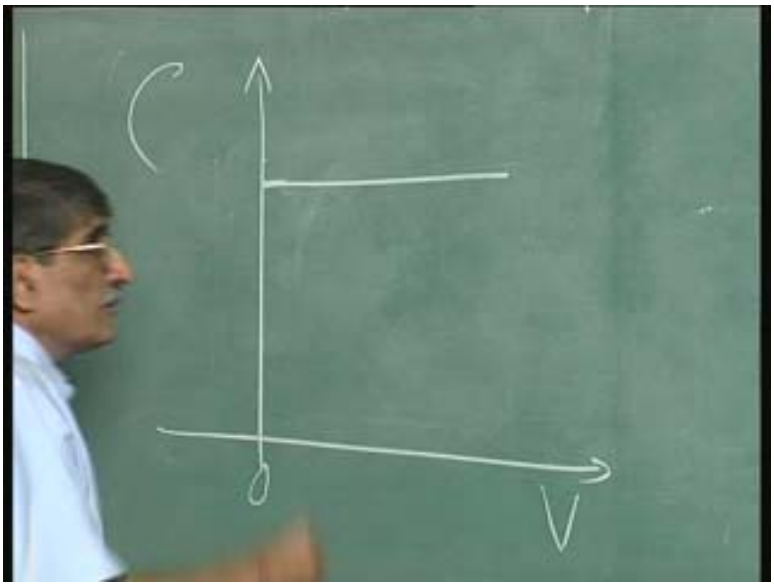

I am just drawing that to explain that. Now, when you apply negative voltage, it looks for plus charges. So, you get depleted layer there. The capacitance is capacitance of the oxide in series with capacitance of the depletion layer.

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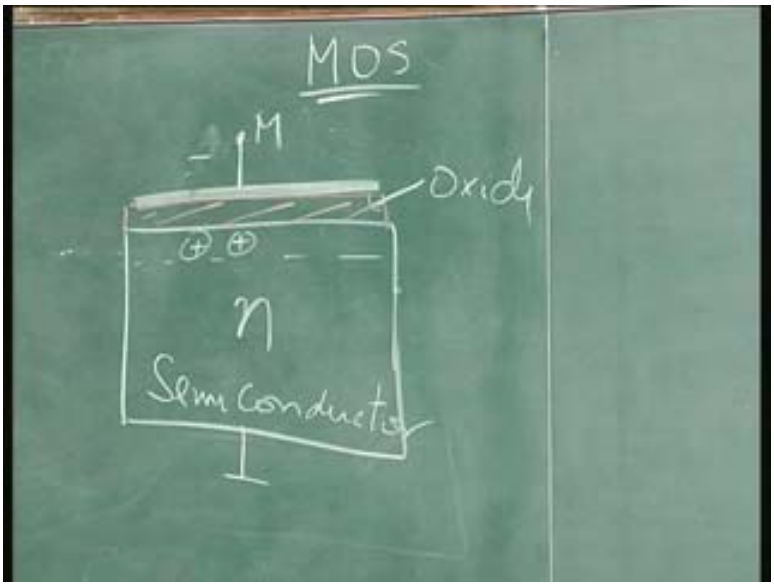

Depending upon the negative voltage that you apply, you get this. Till some maximum capability, the depletion layer reaches. Let me not get down into that. Now, what I say, if you take maximum value then the capacitance reaches a minimum at high frequency.

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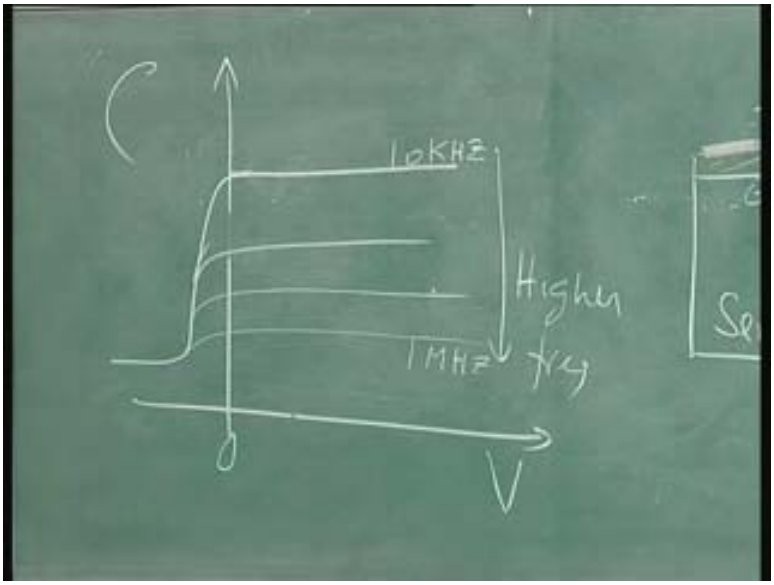

Now, when we make a gallium arsenide MOSFET like this, measure the capacitance; there will be two things happening. One is the capacitance. This is of course, is ideal one at zero, it starts stopping. This may shift that does not matter. We can always move it up and down. This capacitance instead of giving 1, they give higher frequency 1 megahertz, 10 kilohertz; there is frequency dispersion. Measure the C-V at different frequency; capacitance is different which is not supposed to be ideal.

Ideally, capacitance must be equal to one and high frequency itself should go through this. That should be the capacitance of the oxide. Let me right now skip that the reason for this frequency dispersion is the high interface state density. We will come back to that later, if necessary. Right now, we are not going to do mass, we are just throwing out our mass out of range. This is the thing and that is due to that. The other thing that is what is meant by the frequency dispersion? What is hysteresis? This is frequency dispersion; multiple curves for different frequencies. Hystrtrsis, that is, I will show at one frequency, this is capacitance versus voltage and this is zero.

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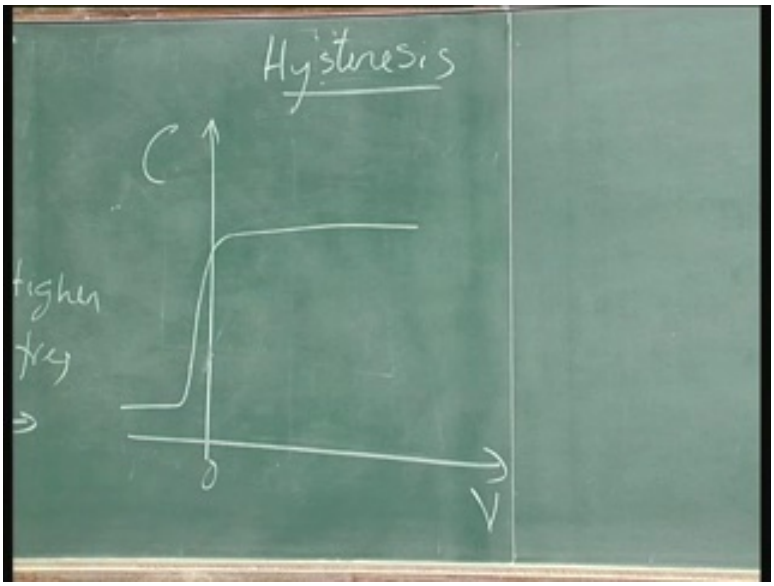

We expect it to be like this. You have taken the low frequency one; we expected to be like that flat. Now, what happens is, go in one direction. For example, you should go up like this, at this point, you get certain capacitance. Now, let me just try to figure out. Suppose there were mobile charge in the oxide when I apply plus voltage that mobile charge like sodium ion will move to the interface. So, actually, what will happen to the plus charge in the interface? It will shift the threshold voltage to negative. If I am sweeping from this side to this side, if there were mobile charge when it is here, when it is negative, where does the mobile charge go? There is an interface like this. If I apply minus here, mobile charge will move up and field is in that direction. Then, it will go up to the top and its effect on threshold voltage or C-V is low. This is because; there is a plus charge and negative charge induced to the metal itself. The difficulty comes there, if the charge induces negative charges in the semiconductor.

The effect is high, if the charge is near the semiconductor. This is due to the reason that it introduces the equal amount of charge. If I move mobile charge here when you apply negative voltage, it will move to the metal and there is no effect. If I come from this side, it will go like this. Now, when I reached here then applied the voltage, I kept it there and mobile charges have moved down. The entire curve gets shifted to the left. So, what you would get if a mobile charge is like this? You will go like this and come back. Now, what

you get in this case is nothing like this. That is, you will get like this, one of the two, let me just put it like this.

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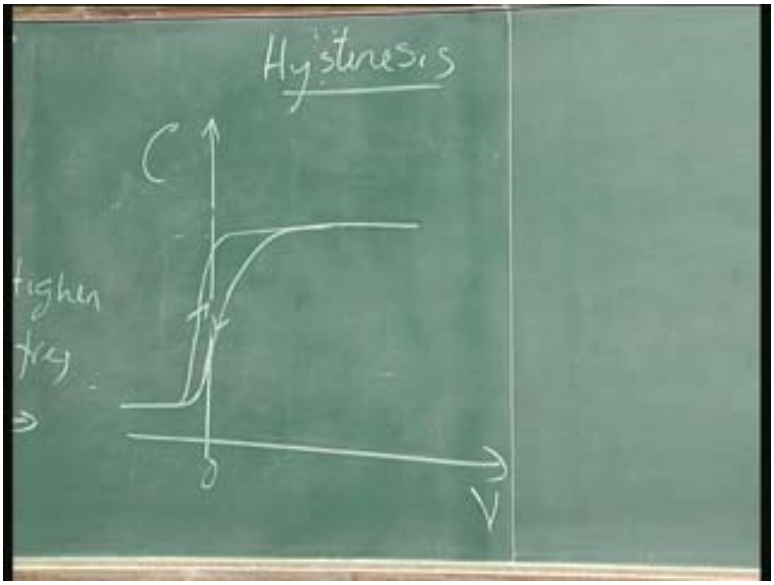

In case of mobile charge, you come back, it comes like that. In this case, it is like that. The hysteresis is in this direction. In the case of mobile charge, how was that? From here, you follow this path when you go this side, which has plus charges there and the whole thing is shifted to left when you come back to this side. But, in this case, it is not due to mobile charge and it is due to charging of interface states. It is just exactly opposite. I just purposely went through that mobile charge to tell you how to figure out. It is not the mobile charge. If it were going like this, sweeping like this then you would have said you got a very bad oxide, there is a mobile charge. Since this is actually clockwise hysteresis, that is, it is not due to mobile charge; it is due to charging of interfaces states. Let me stop at that particular effect. All that I want to point out is the interface state has given rise to slow states here. The states also give rise to this frequency dispersion.

When you make a transistor, thick you end up with low transconductance because after all, it is a substrate which must respond to the applied gate voltage. Now, instead of substrate responding, what is the responding you have seen is the interface charge. Interface charge is not going to give us current. When you make a MOSFET, the channel

should respond. When I have to change the gate voltage, the channel charges responds and drain current changes. Now what is happening is, channel charge is not responding since it is shielded by this interface. So, the response is by the interface. When the interface responds, the drain current is not changing. So, delta i_d by delta b_g is smaller, that means transconductance is small. That is what you are looking for. You are looking for very high transconductance in all these devices. Better driving capability means for a given change in gate voltage, drain current change must be maximum. Then, this is not happening. In spite of your predicted high mobility and that is the problem.

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So, MOSFETs actually need a very excellent gate dielectric material. We do not have it, in case of gallium arsenide. Native oxide of Compound Semiconductors exhibit very poor interface properties. You are summing up of what I have said. Very poor interface states are given by that. So, reliable MOSFETs are not made with gallium arsenide and also indium phosphide. I just did not say indium phosphide, the situation is worse. Why? The vapor pressure of phosphorous is even higher than that of arsenic. So, you are in more trouble with indium phosphide. If that is the thing, what is alternate choice for gallium arsenide FET? That is popularly known as GaAs FET and not MOSFET.

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What is GaAs FET? The GaAs FET is Metal Semiconductor Field Effect Transistor and it can be JFET also. What is that? That is my final slide today.

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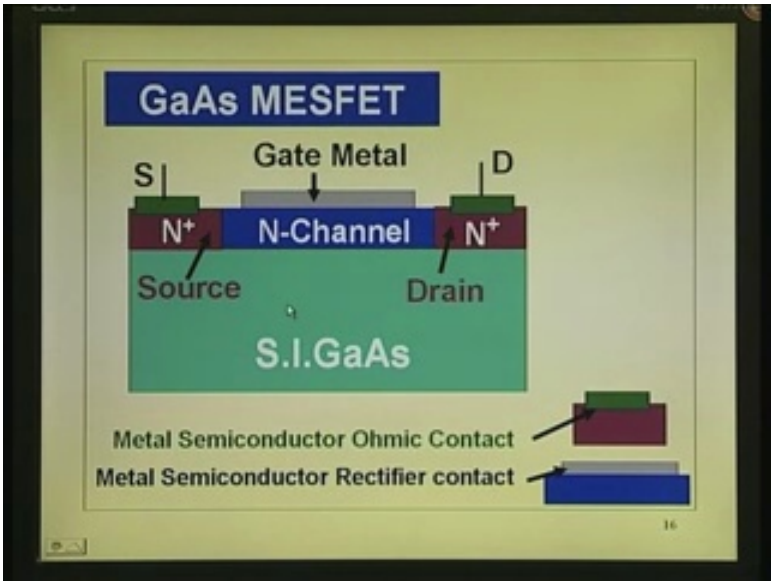

We get down into more details on this in the next discussion. You can see here, this tells what actually it is? It is the gallium arsenide FET or GaAs FET. In this example, that I have shown, the semi-insulating gallium arsenide, I have shown this layer which could be

implanted layer or epi-layer etched otherwise. So, you have got here, source which is N plus, drain which is N plus. Then, metal contact here. You have another metal contact here. This N channel region is in between region and you have another metal coming up. So, you have 3 metals on the surface of this. Two of them behaving differently, this and this behaving differently compared to that. What is the difference between these metals and this metal with the n plus contact or making ohmic contact? You have the I-V characteristics vertically. Ideal ohmic contact is with zero voltage and you must get current. You can never get it.

With minimum voltage, you must get current. That is the ideal ohmic contact. So, that is these two and this is also metal semiconductor contact, it is rectifying contact. So, you have got on the same device and metal semiconductor contacts. Two of them are ohmic; one of them is the rectifying. Now, what we want to see is how we can achieve this particular as a rectifying. What you need is, actually rectifying contact. It is not necessary that you put a metal there. We can put a pn junction there; that is the JFET. Instead of metal, I put a junction p plus region there, that becomes a JFET. I am sure you have studied it way back in several courses even in circuits. So, in gallium arsenide FET, it can be JFET, if you make a pn junction here; it can be MESFET, if you put a metal here. Which one would you choose? The answer is, whichever is easy for you to do, you will choose that only.

In gallium arsenide technology, you prefer lower temperatures processing. You do not want higher temperature processing. If you have to put p plus there either I have to put dopants by implantation or I have to do by diffusion or more sophisticated technology like MBA and all that you are doing. So, those are more complicated technology, diffusion you would like to avoid because that will lead to loss of arsenic and so on. So, what I am trying to point out is because of those problems, it is the metal semiconductor technology.

So, what we say said today to sum up is, we have seen that even though in semiconductor silicon technology, MOS has been more successful. In gallium arsenide technology, MOS has been most unsuccessful. Instead of MOS, it is a JFET or MESFET that is being used

in the case of gallium arsenide devices. But, in the case of indium phosphide devices, you will see that it is not MESFET also. MESFET does not work out in gallium arsenide indium phosphide devices. That has got to be JFET or the last one is the strong that is MISFET, MIS Field Effect Transistor. In fact, there is some drive to get MIS Field Effect Transistor in gallium arsenide also. With that, I think we will conclude today. Tomorrow, we will discuss this and go into the ohmic and metal rectifying contacts with metals.