Electronics for Analog Signal Processing - I
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Lecture - 38
Active Components used in Electronics

So, we have understood how a CMOS inverter functions, both as a logic circuit as well as an amplifier; and now, now let us see an example.

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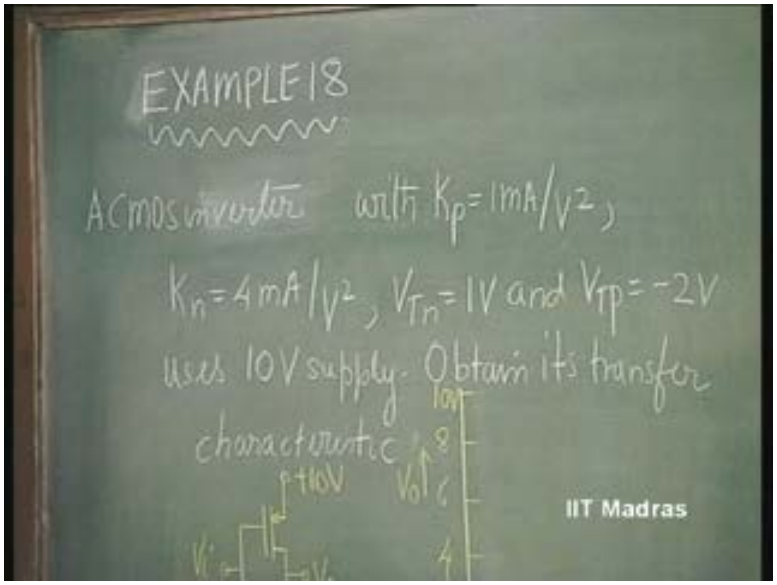

Example 18 - a CMOS inverter with K p equal to 1 milliampere per volts square and K n equal to 4 milliamperes per volt square. V T N equal to 1 volt and V T P equal to minus 2 volts, uses 10 volts supply. Obtain its transfer characteristic. Now, let us proceed with that.

First, this is the CMOS inverter. When V i is zero, output is going to be at 10 volts. The transistor is, T 1 is not conducting. So, this is at 10 volts. This is going to remain at 10 volts up to V i of 1 volt. That is, after that, this V T is 1 volt. After that, this transistor starts conducting. It will come into the current saturation region. So, T 1 is off up to this point. Thereafter, T 1 starts conducting. T 2 meanwhile is in the triode region. So, this is

the region where T 1 is off and T 2 is in the triode region. This is the region where T 1 has come to current saturation region and T 2 is in the triode region. So, this is one important point. One volt.

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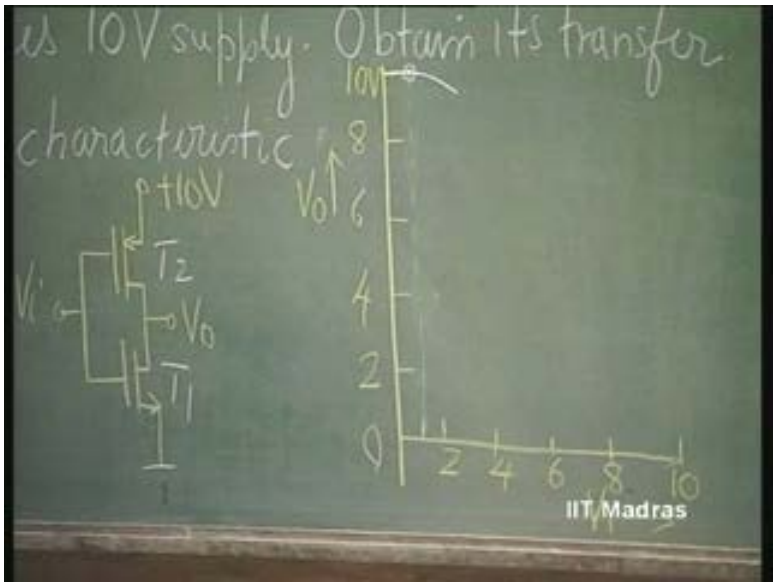

Then T 2 will come into the current saturation region, when, well, this will go on. This is that characteristic curve where I D S 2 is made equal to I D S 1. So, that is the equation that it gives us. I D S 2 is obtained from the fact that it is in the triode region. I D S 1 is obtained from the fact that it is in the current saturation region. And, we have at a point V naught equal to V i plus 2 volts, V T P being equal to minus 2 volts, at a point when V D S magnitude becomes equal to V G S minus V T magnitude.

So, that information gives us V naught equal to V i plus 2, in this case. So that characteristic obviously will start with these two. This is the intercept when V i is zero; and go with a slope of 1 and where will it intercept? When...of course, that we have to find out. When this enters the current saturation region. So we will leave it like that. We do not know where it enters the current saturation region.

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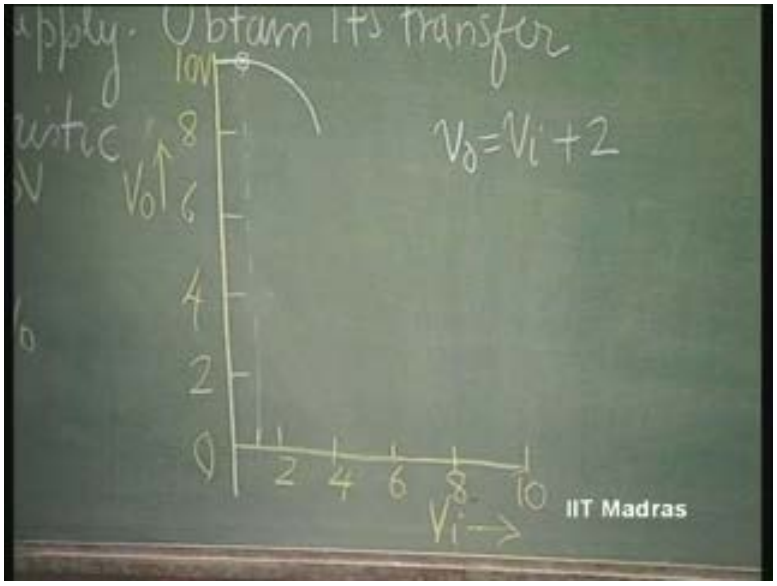

So, the other line is V naught equal to V i minus 1, corresponding to this transistor going to triode region. Again, it is this V D S, which is V naught itself, is equal to V i minus 1. That is the region where it is entering the triode region. Now, in between, we have both transistors in current saturation region. Therefore, we have K P which is 1 into... now, this is important; V G S minus V T, which we are going to always refer as V S G. So, 10 minus V i minus 2 volts.

Otherwise, it would have been V i minus 10 plus 2 volts. So, this square equals K of the other one; 4 into V i minus 1 square, which is nothing but 8 minus V i. Remove the square. This is 8 minus V i. Square root of 4 – 2, into V i minus 1, from which we get 2 V i plus 1 V i, 3 V i; equals to how much? 3 V i equals 8 plus 2 – 10 volts.

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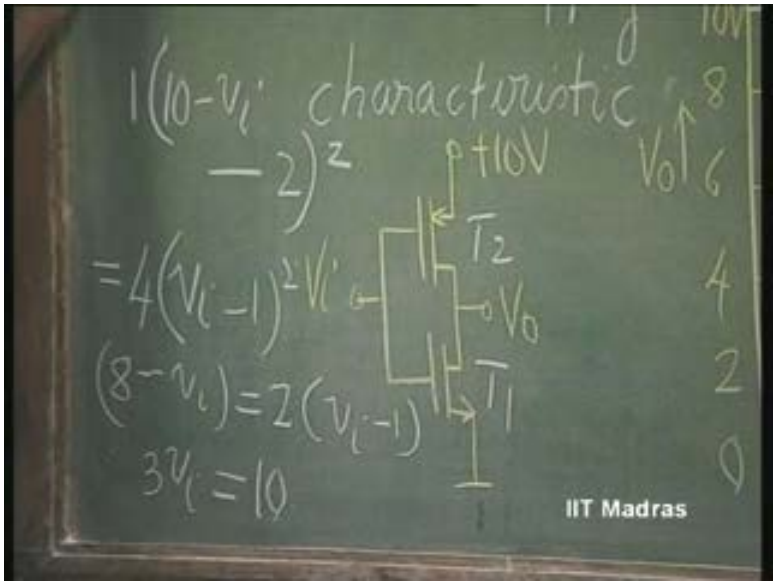

So, V i equals how much is it? 10 by 3. Is this clear? So, this is 10 by 3 is 3 point 33, so on...

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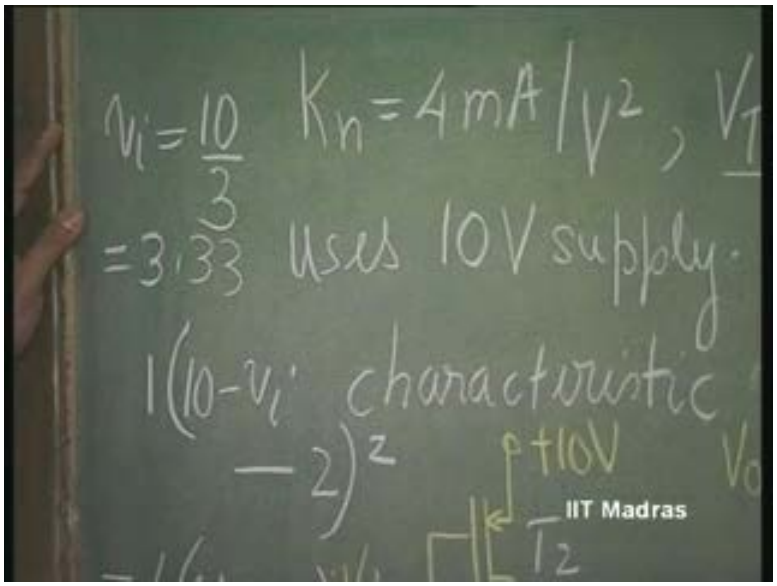

So, somewhere here, this is 3, 3 point 3. So, we can draw that somewhat more carefully. Now at V i equal to 3 point 33, there is a transition and it is having infinite slope where both the transistors are in current saturation region.

So, if V i is equal to 3 point 33, then this voltage at which this transition takes place is V naught equal to 3 point 33 plus 2 volts. That is 7 point 33. This is 7. So, this is about 7 point 33. So, you can see that, from that point to this point, it is going to be a non-linear curve. So, this corresponds to 7 point 33, V naught equal to 3 point 33. Sorry. 5 point 33. V i is 3 point 33. This is 3 point 33 plus 2; that is, 5 point 33. This becomes 5 somewhere here; 5 point 33; and this one is 3 point 33 minus 1, which is 2 point 33. At 2 point 33, once again it is going to deviate.

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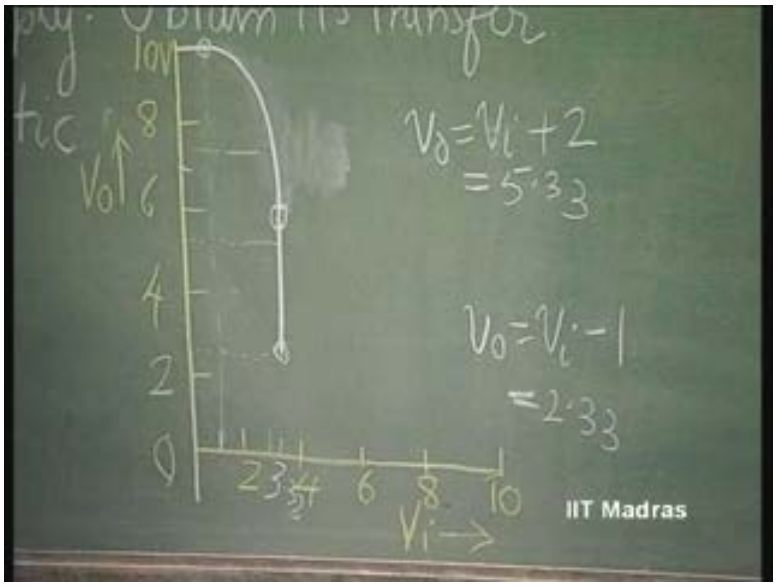

So, this region from 2 point 33 to 5 point 33 - for a region of 3 volts, which is strictly speaking, magnitude of V T N plus magnitude of V T P; 1 plus 2, 3 volts here, it is having infinite slope; thereafter, up to 8 volts... What is 8 volts? 10 minus magnitude of V T P; 10 minus 2 volts - 8 volts. This story will go on. After this, transistor T 2 will go off.

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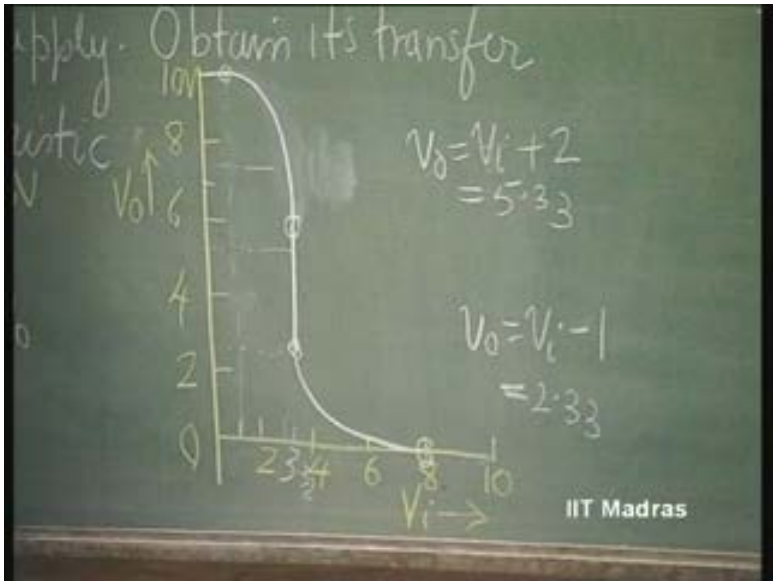

So, this is the complete characteristic of our CMOS inverter where, if you draw a 45 degree line... 45 degree line, what is the slope? Tan 45. That is minus 1 here. You can draw a similar line here. It is within this region that we say that the transistor, CMOS inverter, is in the active region; gain is greater than 1. Beyond this region, it is not in the active region. It has gone into what? One of the two saturation stages: either this or the other one.

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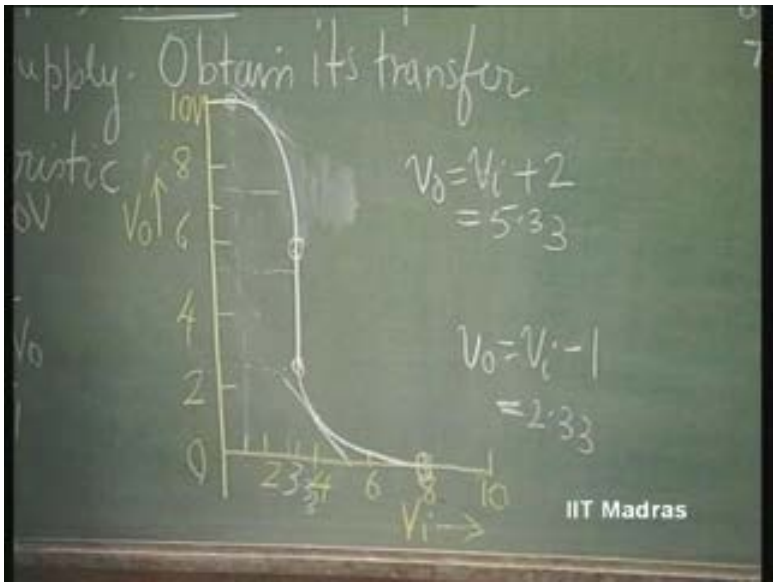

So, these are important in digital circuit in defining what is called as noise margin. So the point at which D V naught by D V i becomes equal to minus 1. You already know V naught versus V i characteristics from the equation of what? - currents being equal. So, from that equation, we can obtain D V naught by D V i equal to minus 1. You substitute that and find out the point at which this occurs. This, I am going to leave as an exercise for you. In this region, find out D V naught by D V i from the expression for V naught versus V i and then substitute equal to minus 1 and find out the point, V naught and V i, at which this happens.

So further, when it is in the active region, what will be the gain? Infinity. That is only when we are assuming that r d s of these transistors are infinity. Now, if you take finite r d s, this, there is an r d s 1 here. This is r d s 2. r d s 1 and r d s 2 - they come in parallel and therefore the gain of this is... this is going to be replaced by a current source which is g m into V i. This also is going to be replaced by another current source g m into V i. As far as signal is concerned, whether you use NMOS or PMOS, it does not make any difference.

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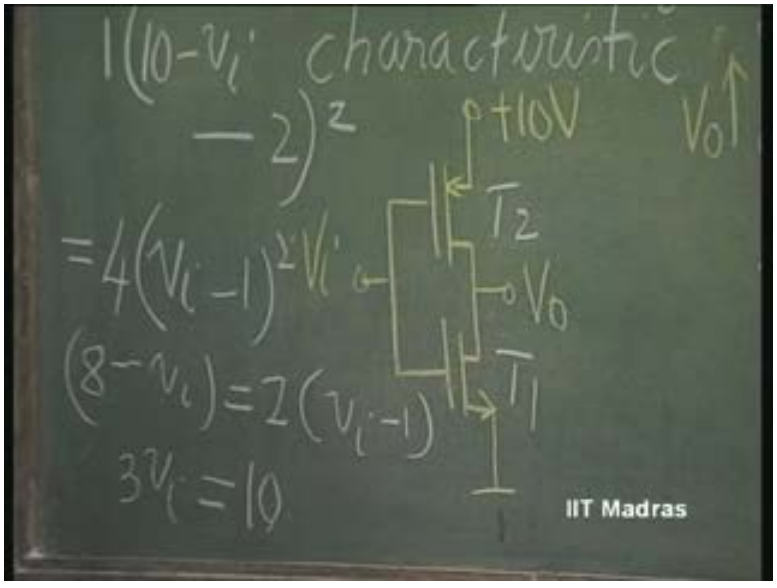

So, these two are working in parallel on to the same load; and the load is r d s 1 parallel r d s 2. And what is the effective current? 2 g m times V i. One g m times V i due to this; another g m times V i due to this; or, assuming that both the transistors are operating at the same current, that is true. So, g m 1 and g m 2 may be different because Ks are different. So, in the sense g m 1 plus g m 2 into r d s 1 parallel r d s 2 is the amplifier gain, when r d s 1 and r d s 2 are not infinite. Is this clear?

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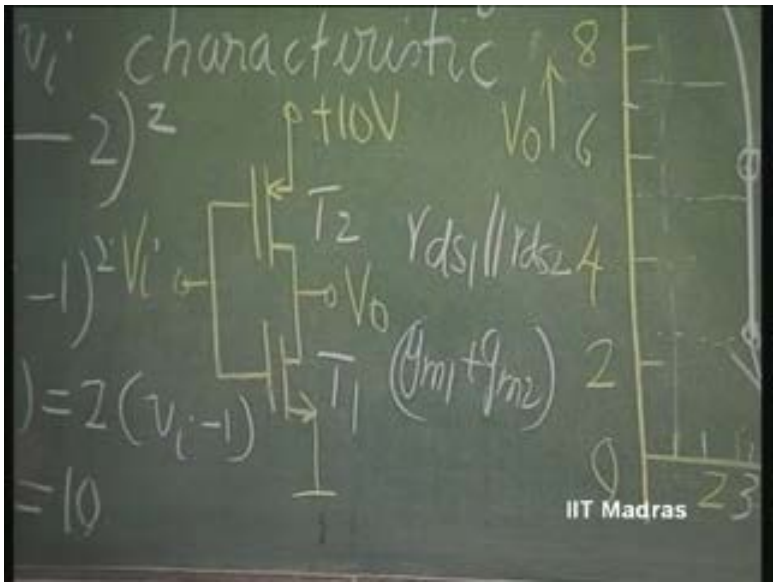

So, these two amplifiers are working in parallel on to a common load which is r d s 1 parallel r d s 2. Since they are working in parallel, the effective g m will be g m 1 plus g m 2 into V i. So, we have understood how this can be used as an inverting amplifier with this kind of gain; how it can used as a digital inverter; and we also know how this current varies with respect to what? – signal, V i.

Now you can see that the current in this, under this situation, is given by this. 1 into 8 minus 2 whole square; or 4 into 8, sorry, 8 minus V i whole square; or 4 into V i minus 1 whole square with V i is equal to 3 point 33. So, that is the maximum current that will flow in a CMOS inverter and gradually it will go to zero on either side. So, this is the point where the current is going to be maximum; we will say current plot. The value of

this is 8 minus 3 point 33 whole square; so many milliamperes. How much is it? 8 minus 3 point 33 whole square; that is 22 point 1 milliampere. So, substantial amount of current flows. So, then again it becomes zero when this transistor goes to off; and again it becomes zero when the other transistor goes to off state. So, this is the nature of current waveform. This is 22 point 1 milliampere.

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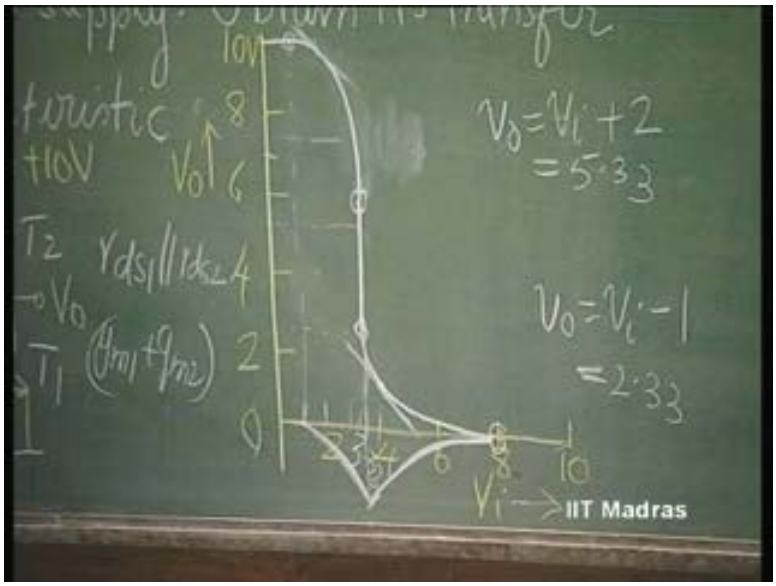

Now I am going to show you the actual components like the transistors; the active components as well as the op amp that we commonly use in our circuit design.

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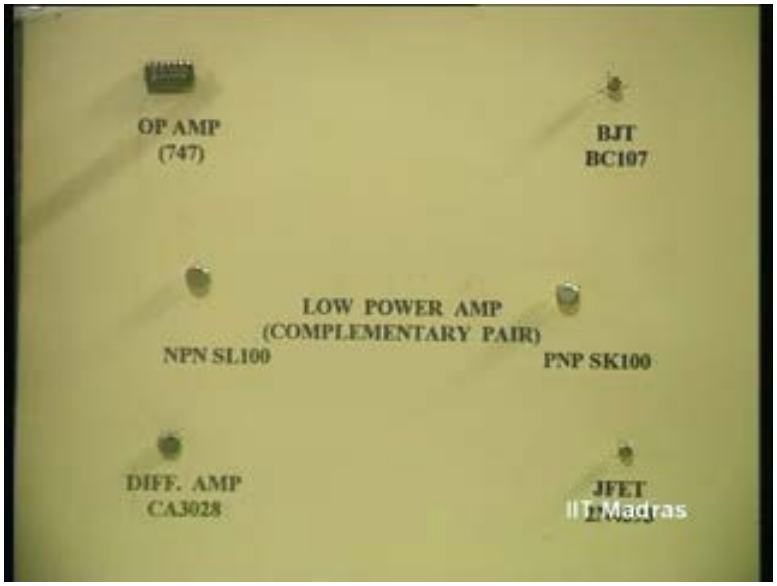

So, we have here an operational amplifier 747, general purpose operational amplifier, very commonly used. This is what is called dual in line package. I mean, this can also come in what is called T O 5 package which looks like this. This is dual inline package. There are 14 pins here. 747 comprises two operational amplifiers, identical operational amplifiers. Now each operational amplifier will have two input terminals, differential input, one output terminal; so, three terminals; and two power supplies terminals for the dual supply to be applied.

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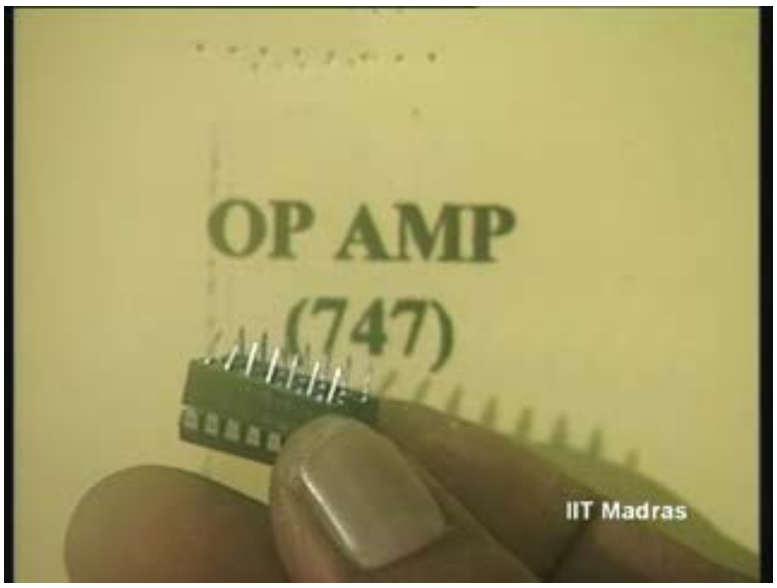

So, two plus one - three plus two - five terminals essentially; and if there are two such op amps, we will have ten terminals taken care of. And in this fourteenth pin, we have possibility of what is called offset compensation, about which we have also discussed. So, two terminals for one op amp and two terminals for the other op amp for offset compensation. So that forms the fourteen pin base and the base diagram we can see here; top view of L M 747.

Two op amps A and B, the two input terminals, one output terminal of A, two input terminals and one output terminal of B; this is the non-inverting terminal. We know how to find out non-inverting terminal and inverting terminal in an amplifier configuration. That means, phase shift from here to here is zero. Phase shift from here to here is 180 degrees and this is the negative supply.

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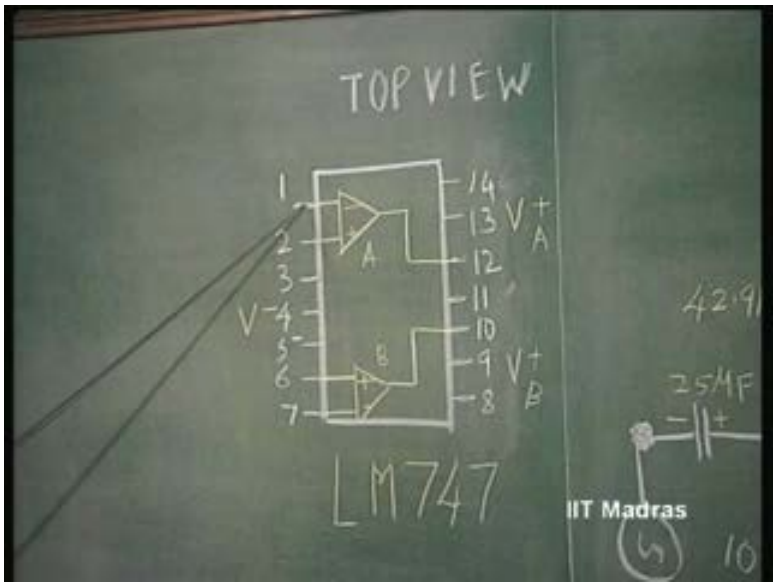

We have two terminals for the... What is that? Positive supply. One for A, one for B; separately. Common negative supply. And then, we have two terminals for offset compensation for each of these op amps.

Now, as far as the other transistors which are going to be used within these op amps, basically these are bipolar transistors. Typically, a single discrete bipolar transistor looks like this. This is B C 107, a small signal amplifier stage we can build using such a transistor. Now normally, the projection is the emitter or the source in the case of a field effect transistor. There is a small projection. I do not think you can see that in this; metal projection in this, which is the emitter or the source in the case of the FET; and you can also identify the base.

Base is the...it forms a triangle; and base is the center or the apex of the triangle. And the other terminal is the collector. That is how you can identify emitter base collector of a transistor.

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These two are NPN and PNP pair which are commonly used for power application, which we will see later. This is called complementary pair – NPN PNP pair; low power amplifier applications, these are used.

Then we have another in it which we had discussed in the class; the differential amplifier. This comprises a pair of matched transistors with a current source with all the biasing incorporated in it. Collector loads are kept open. So, the two collectors are open collectors so that you can connect whatever you want. So, C A 3028 is a very useful differential amplifier used for both video as well as wide band and high frequency IF RF applications. This also, we will see later, how this differential amplifier can be used.

This, of course, is a junction FET. Once again, we have three terminals with projection being the source. Then we have the gate and the drain. So, these are the active devices which have been displayed here. The application of these, the biasing of these, have been discussed and use of these in amplifiers, we have discussed. And how to design a high

gain amplifier and make an op amp out of it also has been discussed so far in our course program.

In the next one, we will discuss further about negative feedback, what is positive feedback, what are filters, oscillators, then modulators, demodulators, regulators, voltage regulators, power amplifiers and things like that. So the...this block is going to be over with this basic knowledge about active devices, diode, use of these diodes in variety of applications, use of active devices in amplifiers, building amplifiers, biasing mainly, design of operational amplifiers, basic digital inverter.

At the end of this part one of analog circuits, I would like to indicate that laboratory experience is part and parcel of this program. On all the examples that have been given, worked out, can be tried out experimentally in the laboratory.

I am, as an illustration, taking a common emitter amplifier as depicted here, this has been designed, this has been wired up for you and we will presently see the amplifier demonstration.

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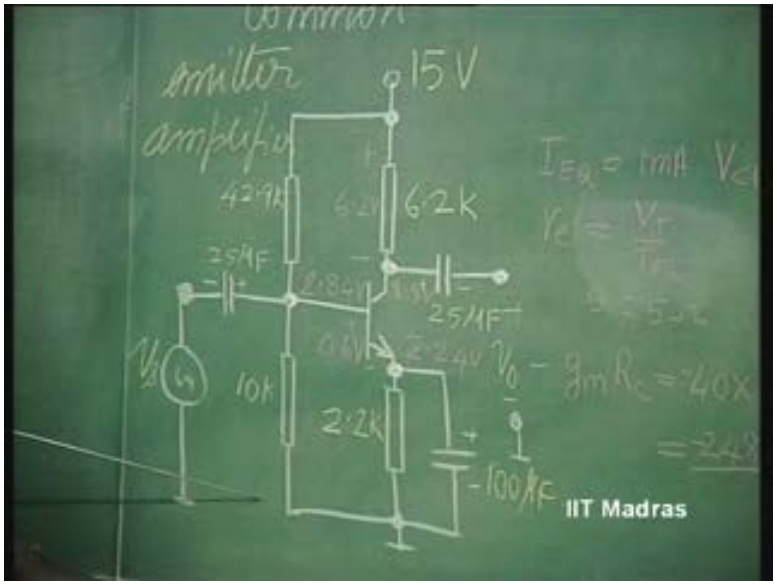

Now 15 volts is supplied to a transistor amplifier with R 1 equal to 10 K; R 2 equal to 42 point 9. So, the voltage at the base, quiescent voltage comes out to be 2 point 84 volts. Calculate it. If you take point 6 as the V B E, the voltage at this point comes out as 2 point 24 volts; and we have introduced 2 point 2 K to ground, emitter resistance, and therefore current in this is roughly 1 milliampere.

So, this transistor has been biased to operate at 1 milliampere. This has been bypassed by the emitter bypass capacitor of 100 microfarad. So, this is common emitter configuration biased at 1 milliampere. Because it is 1 milliampere, 6 point 2 volts drop will occur across R c of 6 point 2 K and 15 minus 6 point 2 volts is roughly 8 point 8 volts.

8 point 8 volts minus 2 point 8 is roughly going to be 6 volts; that is the V C B Q. So, I E Q is 1 milliampere. V C B E Q is 6 volts; r e which is V T over I E Q is roughly equal to 25 ohms; and therefore, g m, minus g m r c which is the gain of the common emitter amplifier is minus 40 millisiemens for 25 ohms, it is 40 millisiemens into 6 point 2 K which is minus 248.

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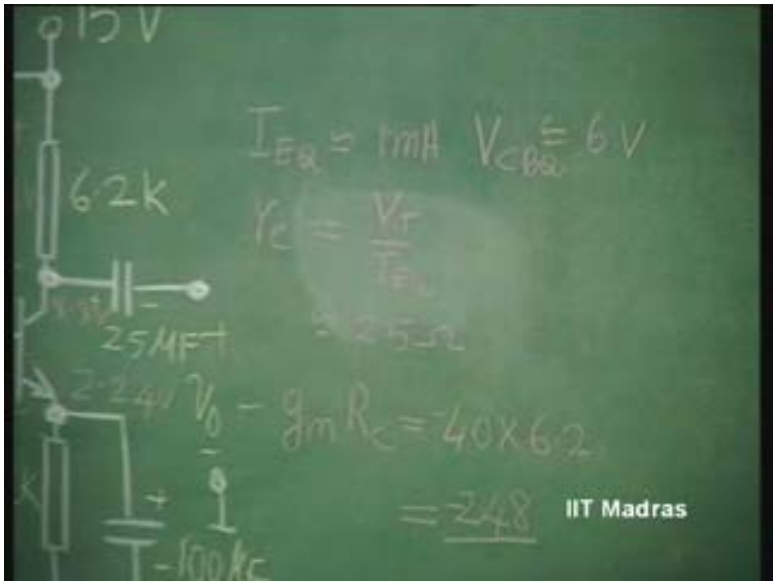

Now we will see whether in our experimental set up we get really this kind of gain and what kind of waveforms we see here and displays to the experimental set up. We have here Padmavathy, who has wired this circuit and we have an oscilloscope to see both the input and the output waveform. You can see the output and input waveform.

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And there is a phase shift of 180 degree. As we can see, when one is going to the...this is the output point; through the capacitor it has been taken; input is here. So, these two points...the waveforms are shown in the oscilloscope there. So you can see that there is a phase shift; when the voltage at the input is increasing, output is decreasing, can you see that?

And also corresponding scale, if you read out, the input is about 2 millivolts; and you have got a gain of about 250. So, output is about point 5 volts, peak to peak.

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So, this is depicted there on the oscilloscope. If you couple it along with the scale given, you will see that the gain is exactly equal to 250. Further, we will check the operating points. Now, Padmavathy will show us using a D C multimeter, the potential at the base which should be 2 point 84.

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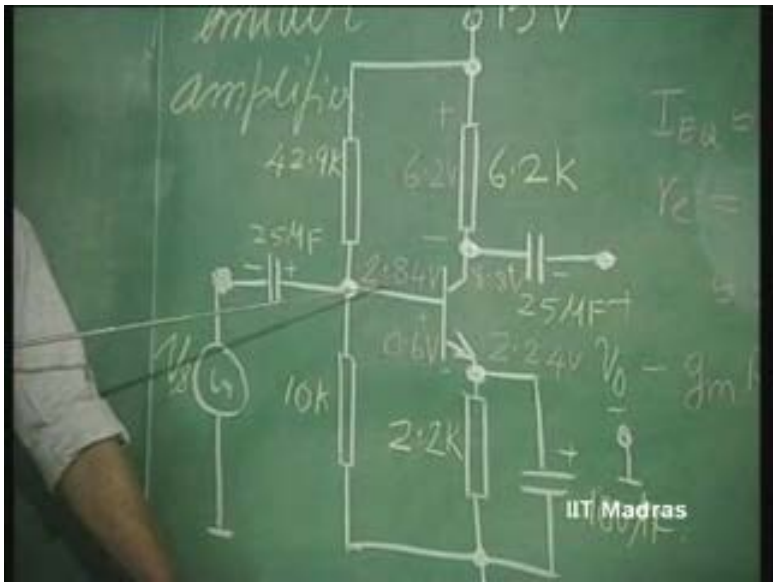

Let us see how much it comes. The resistors are all 5 percent resistors. So, there might be some small variation in this. You can lift it up and show. So, that is the voltage. 2 point 75 instead of 2 point 84, which is acceptable.

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And now, she will connect it at the emitter. There should be a point 6 drop; point 6 volts drop. So, that is the potential at the emitter, at this point in the circuit. Because of point 6 volts drop, we have the potential at the emitter.

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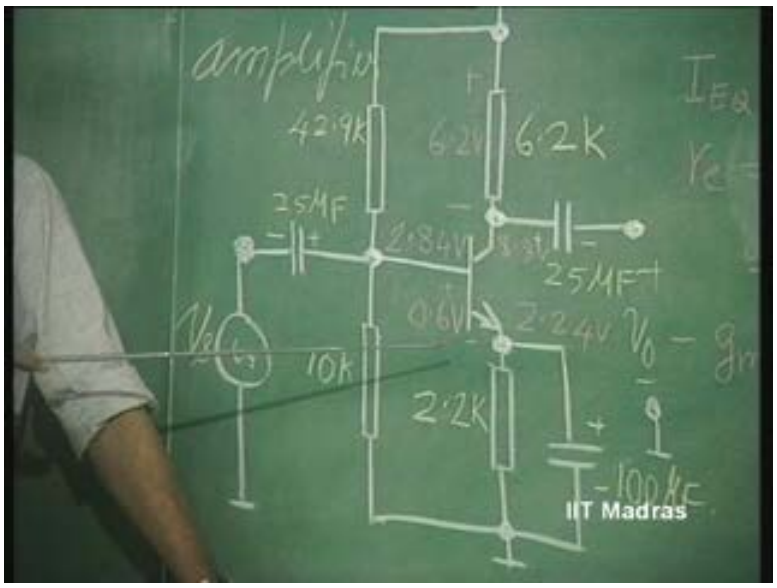

And then, we have the potential at the collector. Once again, she will now connect, connect it to the collector terminal which should be around 8 point 8 volts D C potential. So, you have that voltage 8 point 68 which is pretty close to 8 point 7 volts, which is pretty close to the expected value.

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Now the D C potential, after verifying, you can check the thing for A C signal. Always, first verify the operating point. The transistor should be operating in the active region and it should be operating at the point with which you have designed it. That is most important. Then only you apply the signal. Then you measure the signal gain. That came out as 250, minus 250.

Now, we will illustrate the large signal effect. Now that this is biased to V C B Q of 6 volts here and current I is about 1 milliampere, due to the limits, one is the transistor going to off; that 1 milliampere into 6 point 2 K. So, it is one side 6 point 2 volts; on the other side, it is again 6 volts. See, this almost symmetric swing, possible. That means, both saturation limits as well as cut off limits should begin almost simultaneously. So, let us keep increasing the signal now.

Now, Padmavathy will increase the signal level slowly and show you what happens to the output; distortion will occur. You will see that distortion is going to occur. Yes, you can see that the top portion of the waveform is broadening out. Lower the signal level further. Too much signal. Further reduce it. You reduce the signal level. That is thing you can now... you can see the distortion. This is the exponential waveform.

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Because the current is exponentially related to the input voltage, we have the top portion broadening and bottom portion narrowing.

Now, please increase the signal level slowly so that...slowly... There you can see just decrease it little bit.

You can see the lower portion going to saturation; upper portion corresponds to cut-off. So, that is the signal limit; actually, the signal swing comes out as 1, 2, 3, 4, 5 very nearly 5; about 10 volts. So, around 10 volts or so. I mean, actually, signal can be further increased.

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Now, I would like you to also see the effect of opening the capacitor. This is similar to the circuit that we have discussed in the case of differential amplifier, where the emitter resistance was increased. Apart from this 25 ohms, now it is equivalent to putting 2 point 2 Kilo ohms in series.

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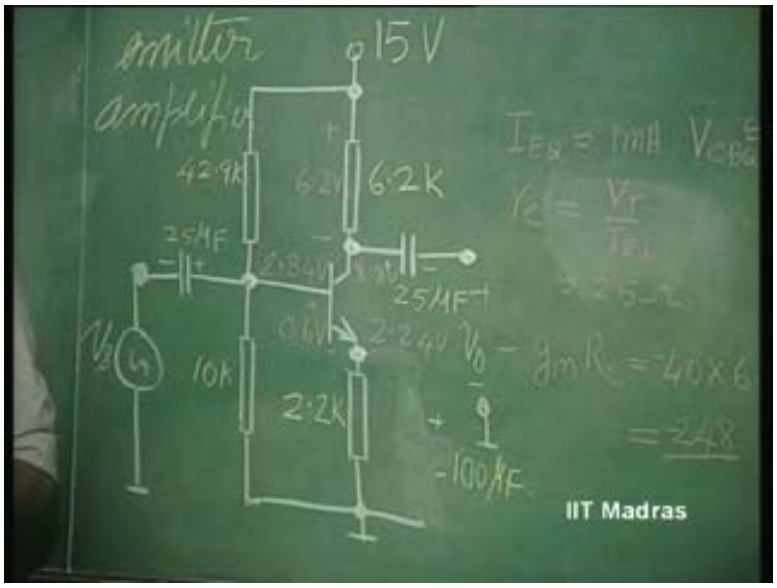

So, we will open the 100 micro farad capacitor and see the same effect. Now, the gain will be much reduced because instead of g m as 1 over small r e, we will have 1 over capital R E coming into picture, which is 2 point 2 K. So, that is 6 point 2 K and that is 2 point 2 K, very nearly 3; gain of about 3 you get. So, this we can see. Here, we will also notice that the transistor takes very little of voltage. Most of the voltage, input voltage is taken by 2 point 2 K; and therefore, there is very little distortion. This we will interpret in a different manner later in our lecture on negative feedback.

So, when the input voltage V i is applied now, that is part...partially falling across the transistor and partially across the 2 point 2 K; and what is coming across 2 point 2 K is the considerable part of signal because the transistor takes only corresponding to 25 ohms and this takes corresponding to 2 point 2 Kilo ohm, in series with 25 ohms. And therefore, most of the input signal is dropped here. That is what we will see.

Now, Padmavathy will connect the input; the same input voltage has been connected and you will see the output is going to be not 250 times the input, but about 3 times the input. Let us see the experimental; see on the oscilloscope very carefully, that...

The input signal level; she has put both the knobs at the same, almost same sensitivity; and therefore, you can see the output and input are almost of the same magnitude except for one scale difference which indicates that there is gain of merely about less than 3. And the phase shift is 180 degrees.

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Now let us increase the signal. Now you will see that there is very little distortion because the voltage, input voltage, has dropped across 2 point 2 K, instead of across the transistor, which is a non-linear device.

And this has become almost linear. So, the D C voltages remain the same. Now, we do not have to bother about the D C voltage that remains unaltered. There is no distortion.

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D C voltage, whether it is small signal or low, low signal, remains the same. Unlike the other situation, the D C voltage is going to change because of distortion. Here, the D C voltage will remain the same. Now, input signal level - she will increase. Oscilloscope. You please concentrate on the oscilloscope; focus on to the oscilloscope; increase the signal level until the distortion starts; further...

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Now you see... No distortion. No distortion at all. Now, distortion will occur only due to cut off and saturation. Other distortion which has earlier occurred due to non-linearity of the device, disappears. This is because it has been made linear by putting a series resistance of 2 point 2 K in series with 25 ohms of the transistor. So, just increase the signal level here. Decrease now.

Now you see, when it goes to saturation, the transistor is a point. Therefore the input signal simply comes at the output. Earlier also it was coming; but input was very small compared to output. But now, input is comparable to output; and you will see, at the point of saturation, the phase shift is the same as that of the input. Do you see...at the bottom line, you will see the top of the signal appearing, making an appearance, so that is when the transistor has gone to saturation. At the cut-off, of course, supply voltage is going to remain...

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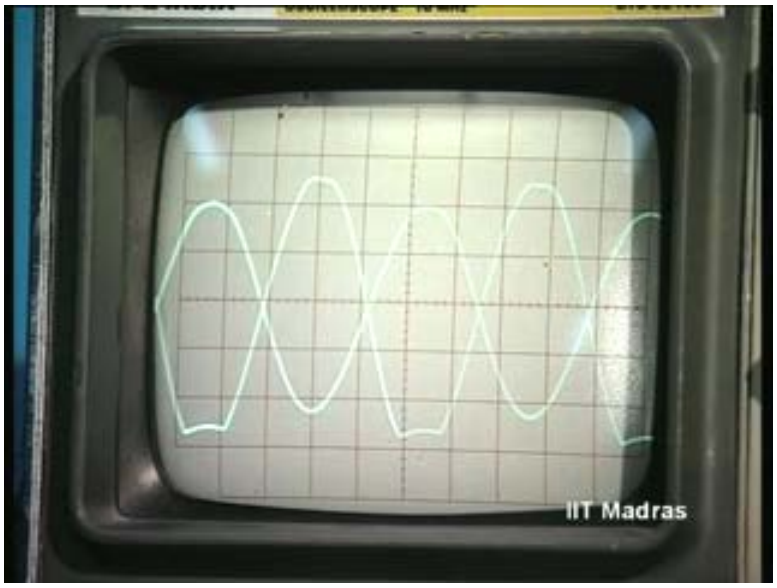

Now, if you increase the signal further, let us ((... Refer Slide Time: 35:34)). You will see the top is chopping off. It is very clearly indicating that it is going up to supply voltage; in the bottom you have the transistor deep in saturation. So, this illustrates very clearly the signal limitation. Now reduce so that it just enters the... now just enters the non-

linearity. It should just enter; keep on increasing the signal further, further; just just stop there now. The peak to peak signal is the limit that we have not really earlier obtained because the input signal is also going to reduce the output swing.

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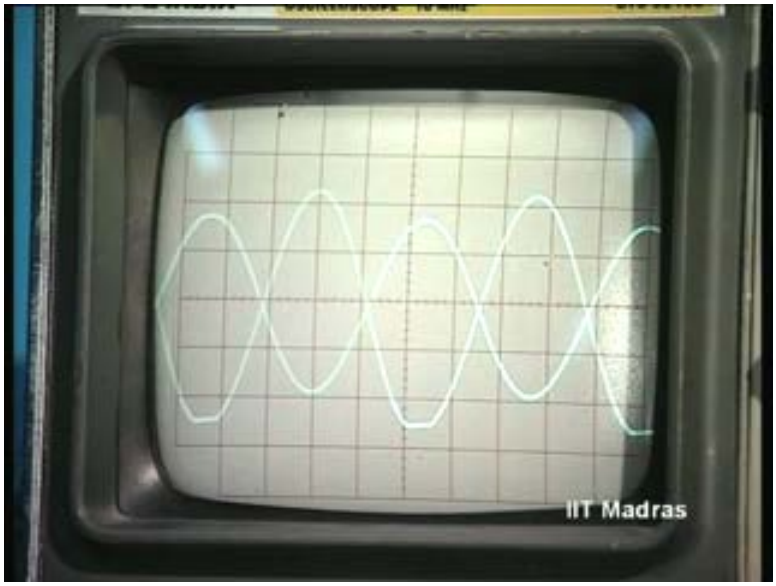

Input is increasing when the output is decreasing. That way, this is the signal swing. This kind of signal evaluation, we will be doing again later, when we discuss negative feedback circuit.

So, in analog electronics, part one, which we have covered through a series of about 38 lectures, we have covered starting with diode as a two terminal element; one port, one port, two terminal element and its applications in diode function generators, in voltage doublers, rectifiers, power supplies and Zener regulators; semiconductor diode application as a temperature sensor and its large signal and small signal properties.

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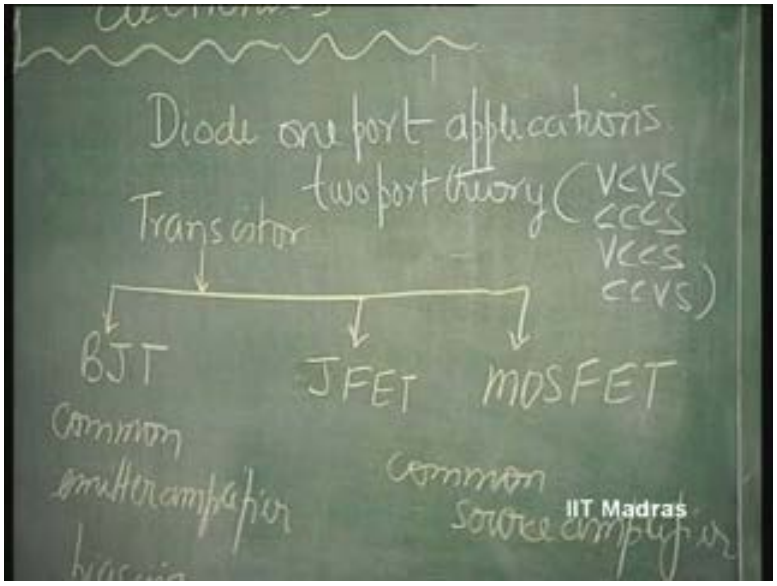

Then we had discussed about two port theory as a prelude to controlled sources wherein we had discussed four types of control sources: voltage control voltages source, current control current source, voltage control current source, current control voltage source, as nothing but amplifiers.

Idealized amplifiers are these control sources with parameters, two port parameters, which are h, y, z and g. We understood how to use these parameters in defining these ideal sources, what are non-idealities and how to evaluate the input resistance, output resistance and transfer parameter in these amplifiers; this two port network theory.

Then we went over to actual active device, three terminal device, transistor. First, we took up bipolar junction transistor and defined transistor action as that which takes place; and collector base junction is reverse biased; emitter base junction is forward biased; I c is equal to Alpha times I e; Alpha being made pretty close to 1. That is the important equation in bipolar junction transistor. So, g m of the bipolar junction transistor, we said, is equal to V T divided by I E Q, where I E Q is the operating current of the transistor. V T is about 25 millivolts; K T over Q at room temperature.

Then we went over to the common emitter amplifier biasing using single supply, dual supply; a reliable way of biasing; fixing up the emitter current that it is...that, a reliable way of biasing is fixing up the emitter current, then evaluation of gain of common emitter amplifier, input resistance and output resistance, the parameters of amplifiers.

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And then, what is the effect of large signal? What is meant by small signal? When does distortion occur, because of the non-linearity of the device? So, how to evaluate distortion. We discussed this. Then, we went over to field effect transistors, junction field effect transistor and MOSFET. How this is going to be discussed in terms of enhancement type of operation and depletion type of operation, and how JFET is a depletion type of field effect transistor and what is pinch off voltage, what is threshold voltage; all these factors we have discussed.

And the square law of current with respect to input voltage of the MOSFET has been highlighted and what is triode region and current saturation region has been discussed. Then, common source amplifier similar to common emitter amplifier can be derived and how using...by using single supply and dual supply you can bias, in an identical fashion, the MOSFETs.

Now, the source current being fixed and how to evaluate the input gain, input resistance and output resistance from the small signal equivalent circuit of the field effect transistor which is almost exactly same as that of the bipolar junction transistor. It is, V B E is the input voltage, g m times V B E is the current source, current in the case of a bipolar junction transistor, if it is V G S as the input voltage, g m times V G S is the current of the MOSFET or JFET and each of these current sources can be shunted respectively by R C E and R D S, respectively in the case of a bipolar BJT and FET. And therefore, the equivalent circuits are similar except that as far as bipolar junction transistor is concerned, at the input, it is not an open circuit. It has an input impedance which is R B E, which is r e into Beta plus one, approximately.

So, all these things we have discussed. And then, went over to getting rid of coupling capacitors and bypass capacitors and coming up with a normal configuration which is universally being used in place of all these discrete circuits and that is the differential amplifier, differential amplifier.

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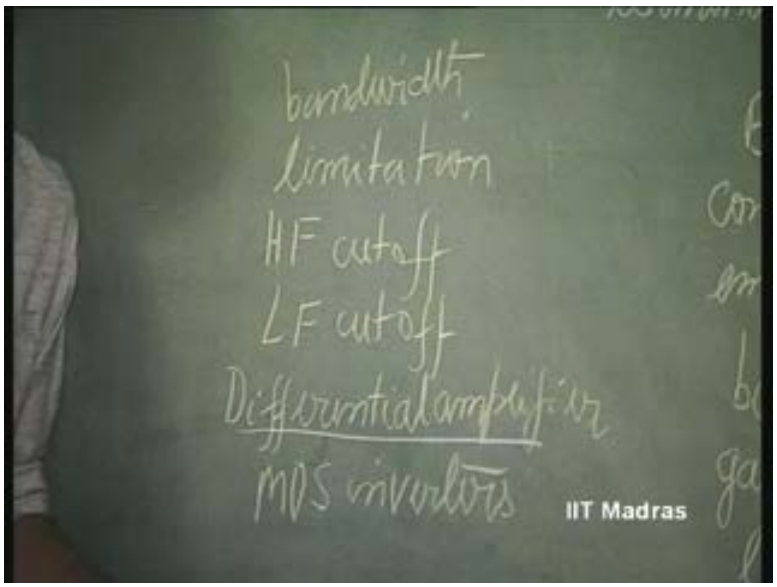

So, we said how this facilitates getting rid of bypass capacitors; and how using dual supplies we can also get rid of input coupling capacitor; and how, by direct coupling, we

can get rid of coupling capacitor from state to state. What are the disadvantages associated with direct coupling? What sort of signal limitation will occur when the NPN transistors alone are used? How NPN-PNP combination helps us in avoiding what are called as level shifters?

And then, we went over to design of an operational amplifier which is nothing but a cascaded version of differential amplifiers; two stages, so that in all these op amps, we always try to increase the forward transfer parameter. Therefore, we get four types of op amps corresponding to the four types of the sources or amplifiers which we have discussed, which are called operational voltage amplifier, operational current amplifier, operational transconductance amplifier, operation transresistance amplifier, wherein always concentration is over improving the forward transfer parameter by cascading. So, we had concentrated on design of operational voltage amplifier and we saw how we can give an equivalent circuit for the op amp, operational voltage amplifier.

Then, we went over to MOS inverters which do not have to necessarily use any resistor at all and the MOSFETs themselves are being used as resistors. We had also seen when discussing about FETs, how FET can be used in the triode region as a linear resistor. So, this form the complete discussion of amplifiers as well as diode, part 1.

In part 2, it is going to be further discussing about other aspects of amplifiers: negative feedback, positive feedback, frequency limitations, wide band amplifiers; and then filters, oscillators; and then modulators, demodulators, automatic gain control, A V C, phase locked loop, etcetera.