Electronics for Analog Signal Processing - I
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Lecture - 37
NMOS INVERTERS AND CMOS INVERTERS

Earlier, we have been considering inverters or inverting amplifier with resistive load. Then in the last class, we saw how those resistors could be replaced, in the case of BJTs, by current sources. Now today, we concentrate to a certain extent on such MOS circuits which do not use resistors as loads at all. That is why they have become famous in VLSI design. The MOS is technology...is the simplest technology compared to the BJT technology. Number of steps for the process of fabrication, they are minimum. That increases reliability of such circuits enormously.

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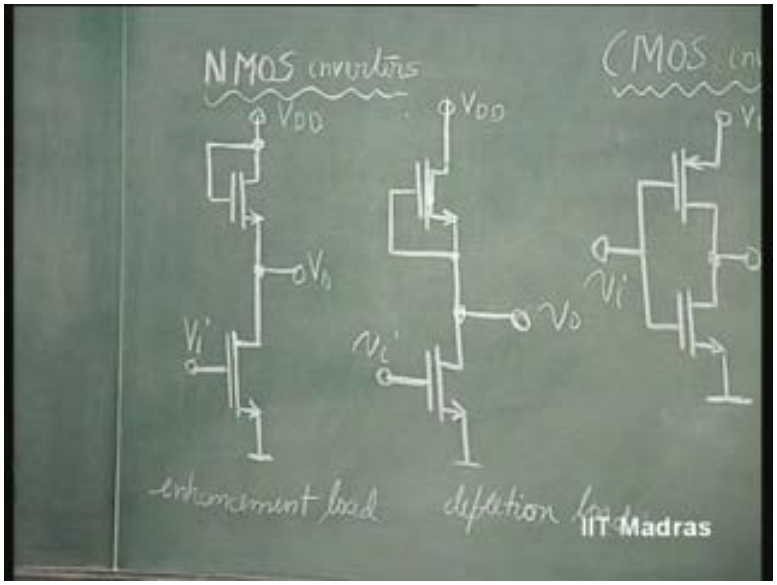

Now, in such MOS circuits, the density of packaging can be increased considerably if we just do not have any resistors at all. The resistors are replaced by MOSFETs connected suitably.

Now, such inverters form the basis of logic circuits, inverters. So, we have the logic family emanating from that. An inverter which uses only n MOSFET is called NMOS logic family. Same thing can be done with the help of only PMOS; then it is called PMOS logic family. And you can also obtain inverters using complementary MOSFETs; that is both n and p MOS. This is called C MOS logic family.

So, these are the three important logic families which exist in your VLSI design for using MOS alone. Now obviously, we should understand the functioning of this. Even in analog circuitry, analog integrated circuits, the same inverters can be used as amplifiers. I have told you inverter is synonymous to amplifier. High gain amplifier can be used as an inverter. So, this can also be used in the active region as an amplifier. So, these blocks are also used in NMOS op amps or PMOS op amps or CMOS op amps. So, these are the basic building blocks which are used in also analog ICs. So, let us understand these also.

Now, consider first this circuit. This is nothing but the common source amplifier with a load resistance here. Source is common to input and output; so the same common source amplifier which we have discussed earlier with resistive load now is being discussed with resistor replaced by a MOSFET. How is this MOSFET connected? We do not want any resistors at all coming into picture. So, and also, we do not want to use further voltage sources other than V D D; in which case, this gate is a terminal. It should be connected to something. The only thing that...if you connect it to source, it will not conduct at all; because it requires a gate resource voltage higher than the threshold voltage; whereas if you connect the gate to the drain, that means V D G is made equal to zero. That means V D S, this is V D S, is always equal to V G S. So, this is an important situation here. V D S is always equal to V G S. We will call this T 2; this as T 1.

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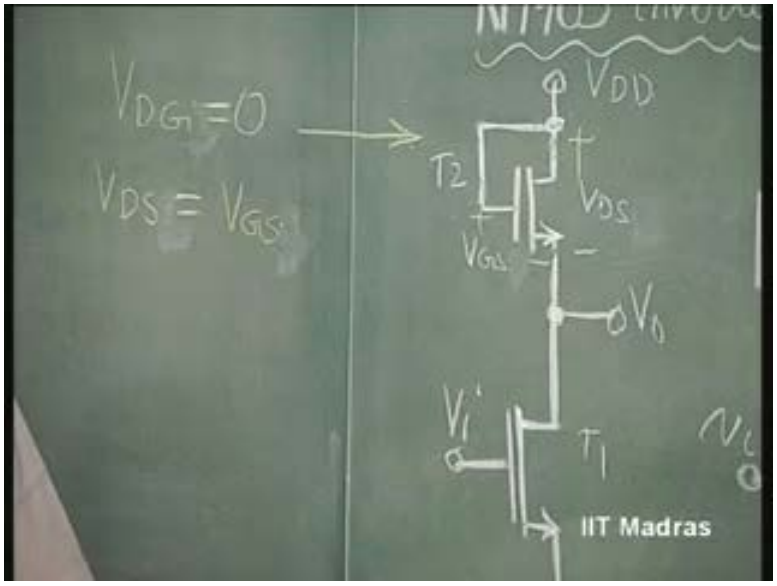

Now, this is V D S 2, this is V G S 2. And V D G 2 equal to zero. Therefore, V D S 2 has been made equal to V G S 2 in this case. So, what is the state of affairs as far as the T 2 is concerned? T 2 therefore is always in current saturation region. Why? Current saturation region, a transistor is going to be, as long as V D S is greater than or equal to V G S minus V T.

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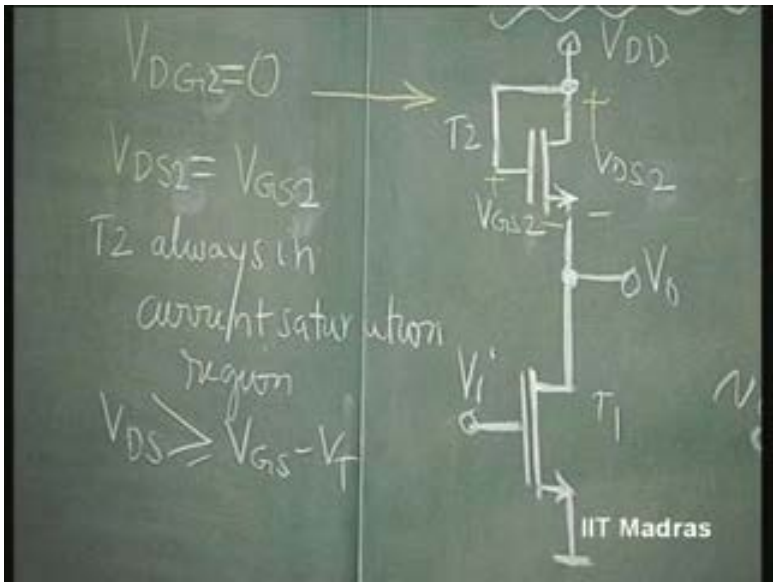

Here, V D S is always equal to V G S; and therefore, we have this transistor always remaining in current saturation region. So, this is what is called as enhancement type of load. For the...this MOSFET, this is an enhancement type of load. In such a situation, let us try to plot V naught as a function of V i. This is what we have done in almost all the inverters earlier also. Now in this situation, what happens? When V i is less than V T, let us say, this V T, this transistor is off. So, when V i is less than V T, T 1 is off.

So, V naught is going to be equal to... Now, that is important. V naught is going to be equal to V D D minus V G S 2. V G S 2 should be hovering around even when current is zero at V T. That is, when V G S 2 is equal to V T, current is zero; so, that is a valid operating point. Therefore, V G S 2 drop of V T is always going to be there; whether it is zero current or higher current; higher current, it will be higher, correspondingly.

So, this voltage V naught, which is V D D minus V G S 2 is going to be... This is V naught, is equal to V D D minus V G S 2, always. When the current is zero, V G S 2 is equal to V T; and therefore, it is starting at V D D minus V T.

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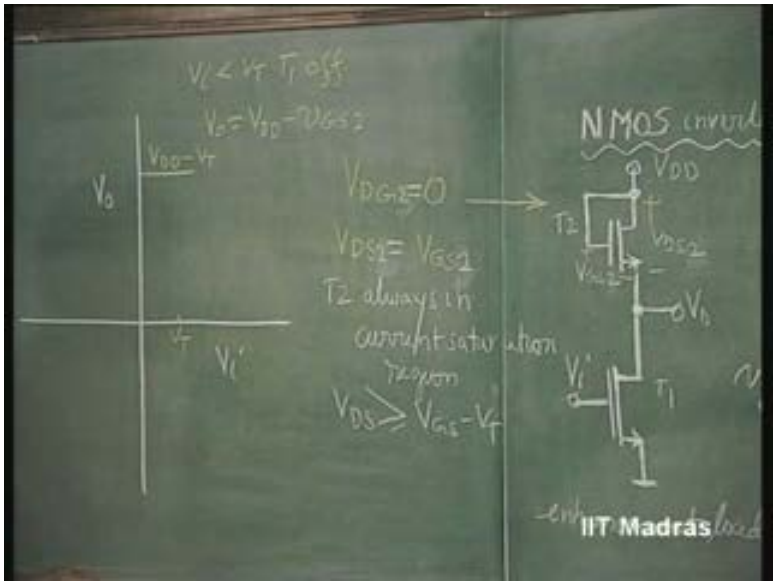

This is an important aspect of enhancement type of load. The high level in any inverter should be normally equal to V D D itself; but it is not so in the case of this kind of inverter. This is a disadvantage. Because we want simplicity in its structure, we have to live with this kind of disadvantage.

So, it is V D D minus V T. Up to V T this is going to be the output potential. Thereafter, let us see what happens. Thereafter, this T 2 is always going to remain in current saturation. That we know. As far as this transistor is concerned, in what region is it likely to be? This potential is very nearly equal to V D D.

So, V D S is obviously much greater than this V G S minus V T, hopefully. Therefore, this T 1, to begin with, is in the current saturation region. So, both these transistors, when we enter conduction, are in the current saturation region; which means the current in this, how much is it? Current in this is going to be, I D S 1 is going to be, K. The K of the...this thing, this MOSFET, is assumed to be same as K of this MOSFET, because these are identical. So, K into V G S 1 minus V T whole square.

What is V G S 1? This is V G S 1 which is V i itself. So, this is K into V i minus V T. This current is same as I D S 2. So, this is same as I D S 2 which is going to be K times how much? V G S 2 minus V T whole square because that also in the current saturation region.

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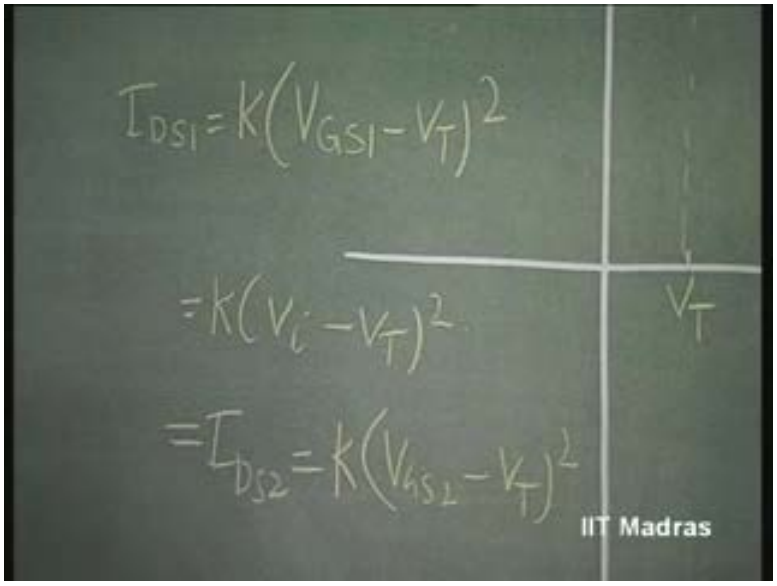

So, now assuming that this K is governed by its W by L ratio. That is the only thing that can be different. V Ts are going to be the same because they are the same type of MOSFET. V Ts are going to be the same. Ks can be made equal if W by L ratios are made equal. Now we have to see whether we have to make w by l ratio equal in order to design a worthwhile inverter; or, W by L should be same. Now, therefore we will call this as K 1 and we will call this as K 2. K 1 and K 2 will be directly dependent upon W 1 by L 1 and w 2 by l 2.

So, these are the equations to be satisfied. And V G S 2 is therefore equal to how much? V G S 2 here is nothing but V D D minus V naught.

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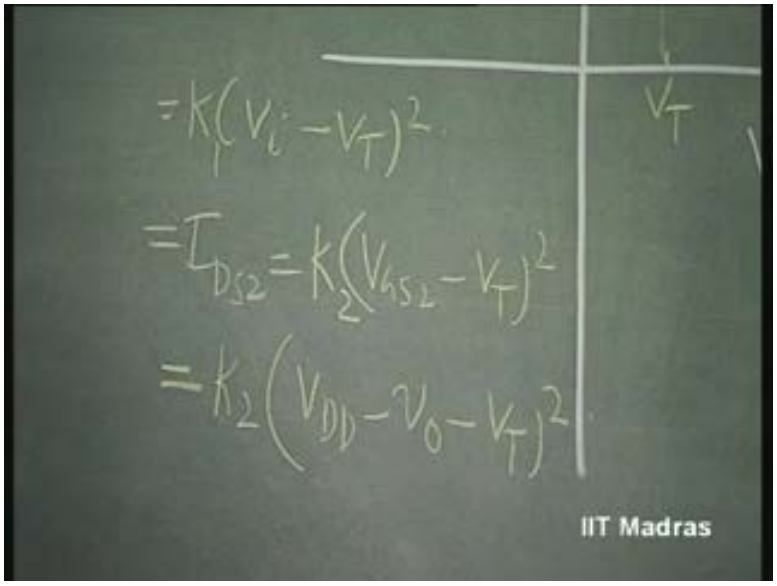

So, from this important relationship, we get the transfer characteristic of the inverter. How is it going to be? It is going to be perfectly linear. It is going to be linear. Why? This square. This is square, this is square. So, we get... you can equate these two. You get V D D minus V naught minus V T equals root of K 1 by K 2; root of K 1 by K 2 into V i minus V T. Is this clear?

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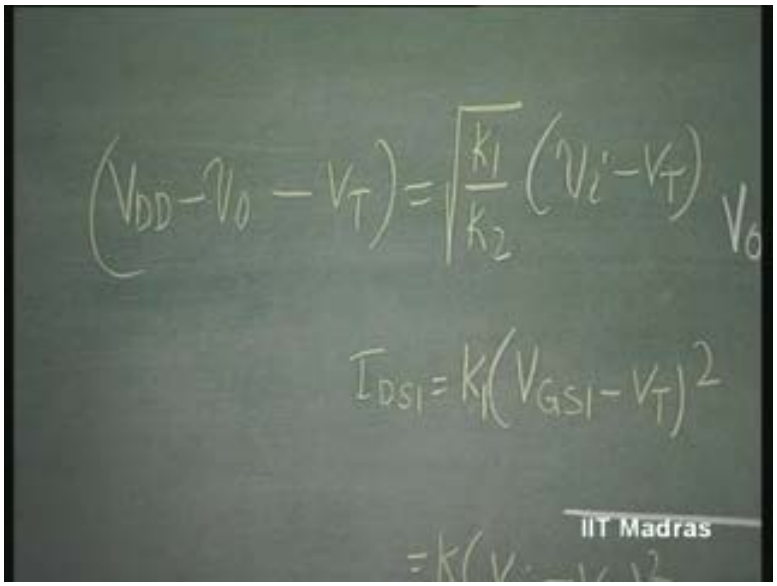

Or, V naught therefore is equal to...you just take V naught on that side; V D D minus V T. V D D minus V T. V naught is taken that side, minus root of K 1 by K 2 v i minus V T.

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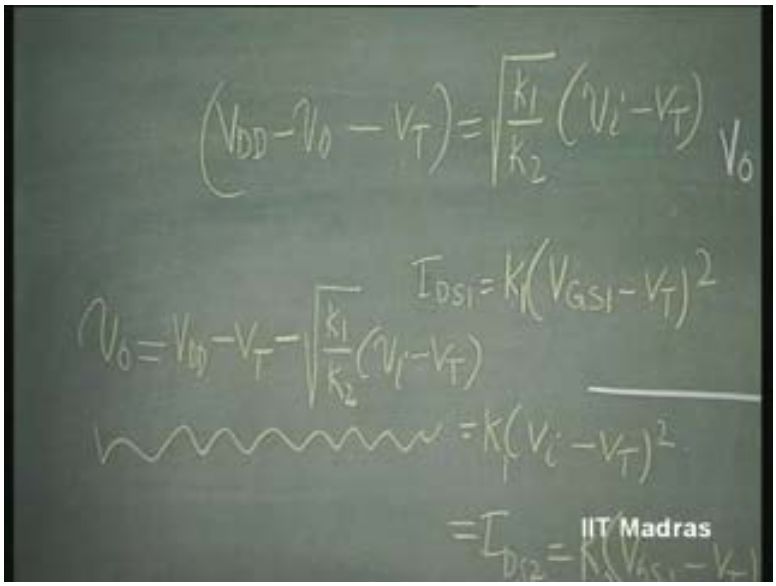

So, if you plot this, this is the slope; negative indicating that it is inverting and the magnitude of the slope depends upon what? - root of K 1 by K 2.

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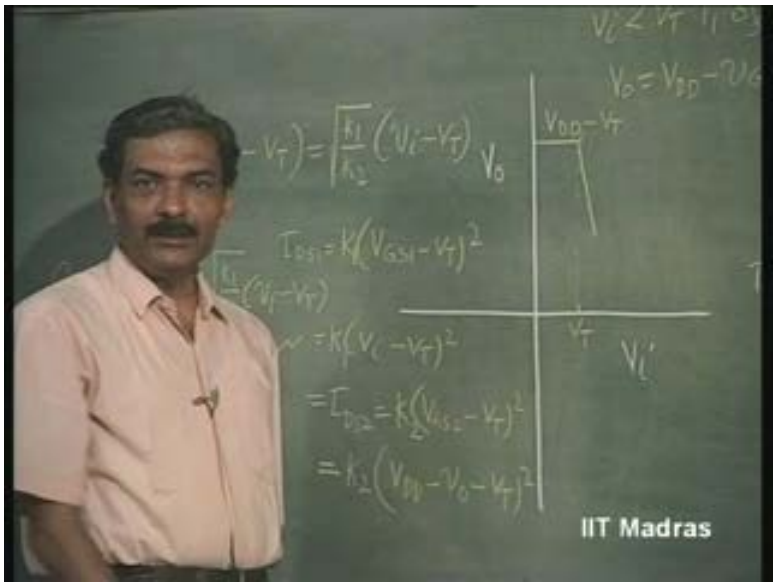

For a good inverter, we have mentioned that this slope is nothing but what is it? - the gain of the amplifier in the active region. The slope is nothing but the gain of the amplifier in the active region. This should be both in the digital inverter as well as amplifier, very high. That means K 1 should be much greater than K 2. Or, W by L ratio of transistor 1 should be much greater than W by L ratio of transistor 2. Is this clear or not?

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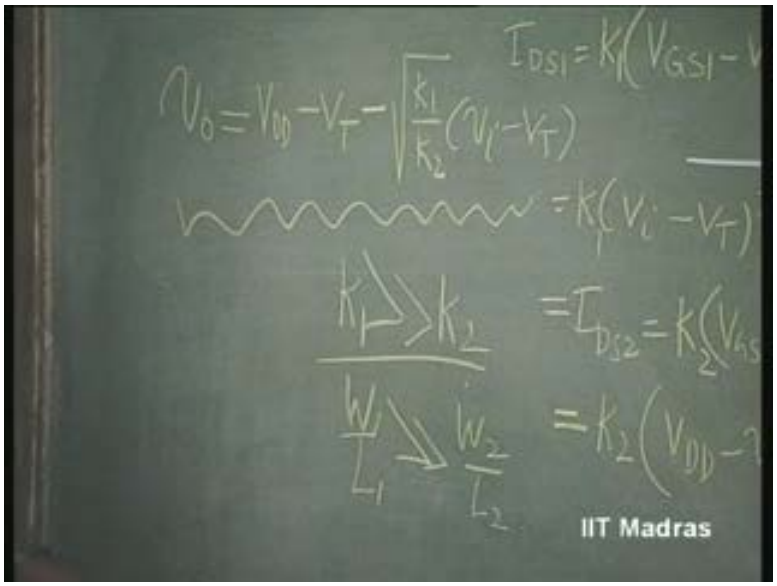

So, this is the design aspect. So, if we make them identical, then it will be having unity gain which is not good, either for amplification or for inversion, inverter application, in the case of the digital circuit. So, this is always what is done.

Now, let us see how it progresses further. That...this voltage will keep on decreasing as you progress. This voltage, output voltage will keep on decreasing. V G S 2 will keep on increasing for higher and higher currents. So, this voltage will keep on decreasing. A time will reach when this voltage, which is the V D S of this transistor, becomes equal to V G S. That is, V i minus V T. That is when this transistor enters the triode region. What is that region? Let us again put...V D S, that is V naught; when that becomes equal to V G S 1, which is V i minus V T, the transistor T 1 enters what? - triode region.

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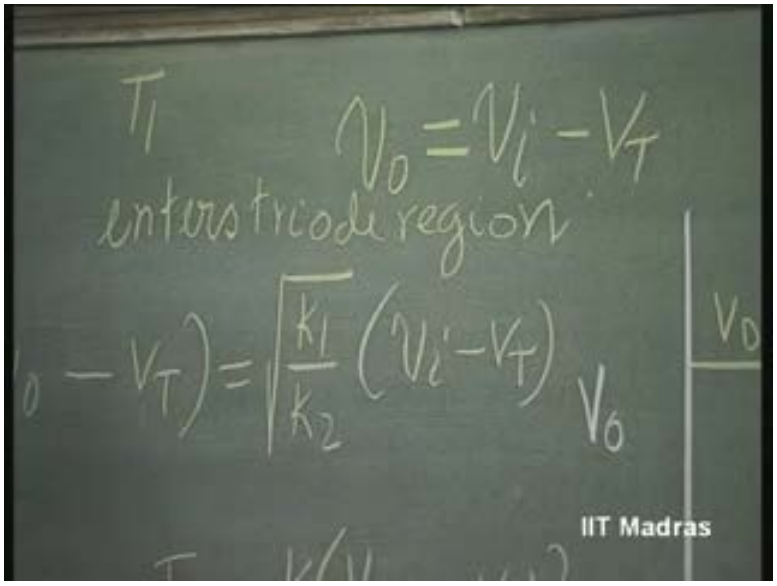

So, this is nothing but a line; let us say this is a line, which is starting at V naught equal to zero, V i equal to V T; so, with a slope of 1. This is V naught equal to V i minus V T. This is another line whose equation is already known. This equation is the equation of this line. This equation is the equation of this line; and intercept is the point where it is entering the triode region. That you can evaluate because you have two equations and two unknowns. So, you can find out V naught and V i at which this happens.

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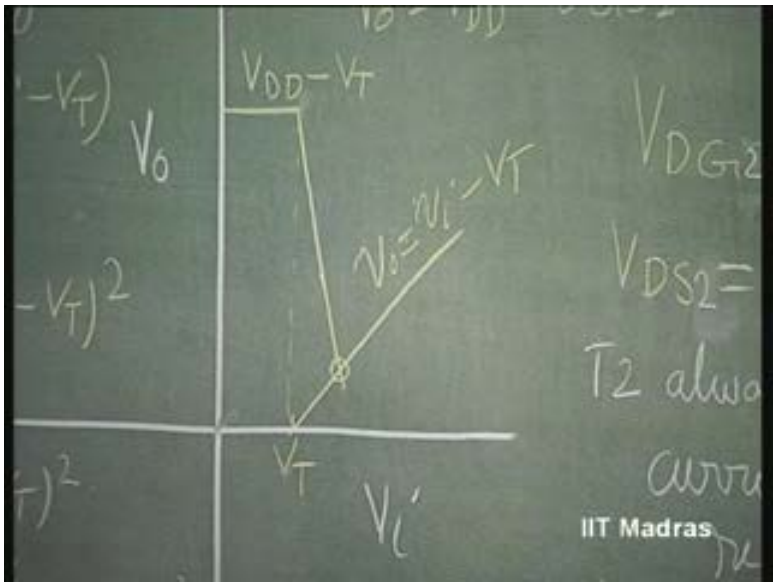

So, that I am going to leave it as an exercise for you. Solve these two equations and obtain V naught and V i at this point, the transition. Thereafter, this equation is going to change because it has entered the triode region. I D S 1 is no longer K 1 into V G S 1 minus V T whole square. It is equal to what? 2 K 1 into V G S 1 minus V T into V D S, which is V naught, minus V naught square by 2, V D S square by 2.

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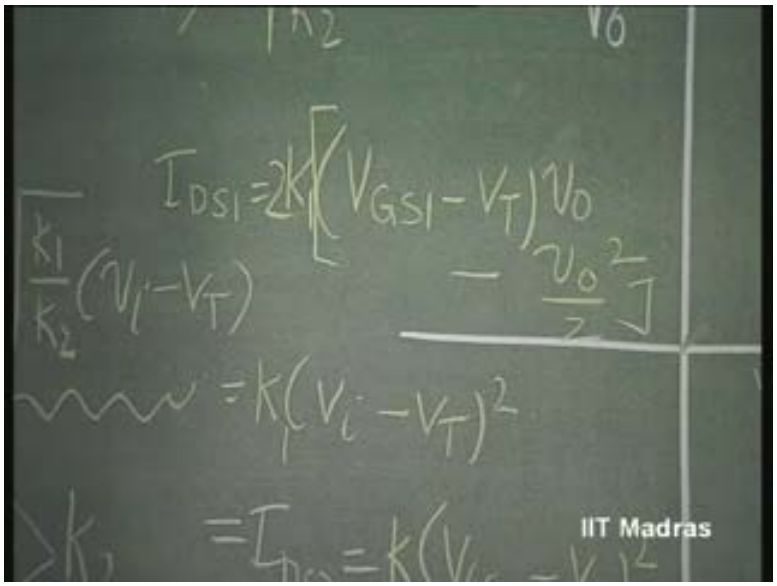

So, this is the equation that is going to be valid and V G S 1 is equal to v i. So now, you will see I D S 2 is going to remain the same. Only I D S 1 is going to change. Again, I D S 1 is equal to I D S 2. Now, this is no longer linear. This is nonlinear because you have square, linear and square here.

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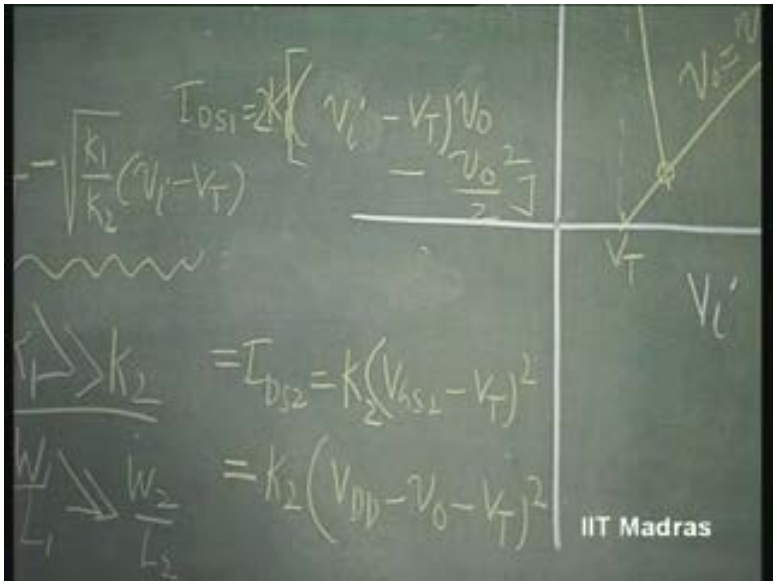

So, this is a non-linear relationship. If you solve for V naught using these two equations, equate these two, then solve for V naught. It is a quadratic equation in V naught. Solve for V naught and obtain that. That again is going to be left as an exercise for you. These two equations, you must take, equate them and solve for V naught. So, both T 1 and T 2 are in current saturation region here. Here, T 1 is off and T 2 always in current saturation. And here, T 1 is in the triode region and T 2 in current saturation.

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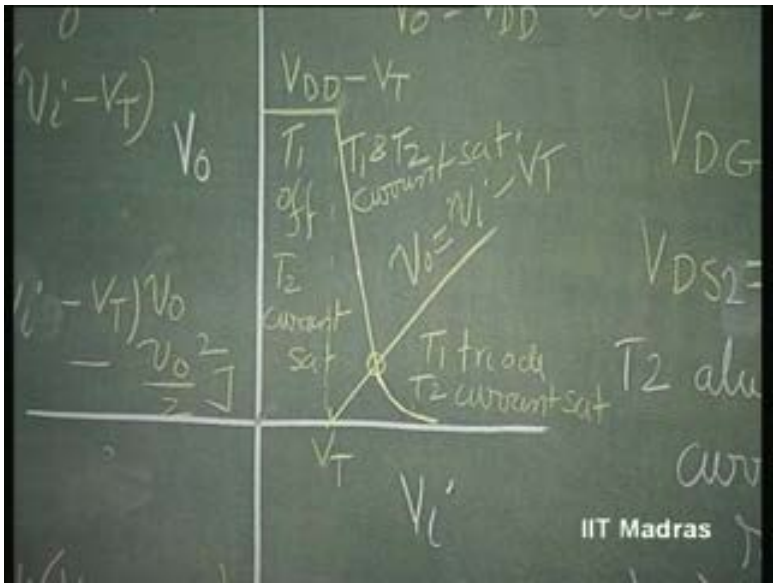

So, you can use this as an amplifier and that is beautiful because you are using a non-linear load and transfer characteristics become perfectly linear. And the gain is root of what? - K 1 by K 2. So, if you use it as an amplifier, for example, in an NMOS operational amplifier, the gain is straight away known as root of K 1 by K 2.

This is not small signal gain. This is large signal gain. It is linear. So, because there is a non-linear characteristic here and there is a non-linear characteristic here, these two non-linearities cancel one another and you get a perfectly linear relationship here. So, therefore, it is perfectly linear here, up to this point. Anyway, this region, we are ignoring because the amplifier is going to saturation. So, this T 1 is going to triode region.

So, this is the operating point. In between, these two can be the operating point, you...so that you get the maximum signal swing. So, you can select appropriately. Once you know this point as well as this point, you can select appropriately the bias point here as the centre point between these two; half of this plus this voltage; that will give you the maximum swing.

So, even if this is made out of PMOS, almost similar analysis is valid. The characteristics will be exactly identical; only that all the things will happen for negative voltage. That is all. That is the only difference. But the entire analysis, its structure and everything remains the same.

Another alternative is to go for what is called as depletion load. This requires a diffused channel here. This we know. In order to make a depletion MOSFET, we have to diffuse the channel and therefore channel exists; so, it is conducting. Even when V G S is equal to zero, it is conducting. Now, this is a nice thing. V G S can be made equal to zero. That was not possible here. So, we can make V G S equal to zero. If V G S is zero, it will have a current of I D S S through it, if the voltage across this exceeds the pinch off.

But below pinch off, it is going to act like a...almost like a resistor. So, this is the advantage and therefore the voltage dropp, when it is zero, the current is zero. When the

current is zero, the voltage drop is zero. That means, the voltage here can start now from V D D itself. So, between this and this, you have this disadvantage here. So, it will straight away start with V D D.

So, its transfer characteristics, now if you plot, it is going to start at V D D. Then, at that point of time, this transistor is going to be in the triode region and this transistor is going to be in the current saturation region. Things are slightly different from this. This is going to be in the triode region and this is going to be in the what? - current saturation region. So, we can once again start off this whole thing for the second circuit where depletion type of load is there.

Until V i is equal to V T is reached, this transistor T 1 is going to be off.

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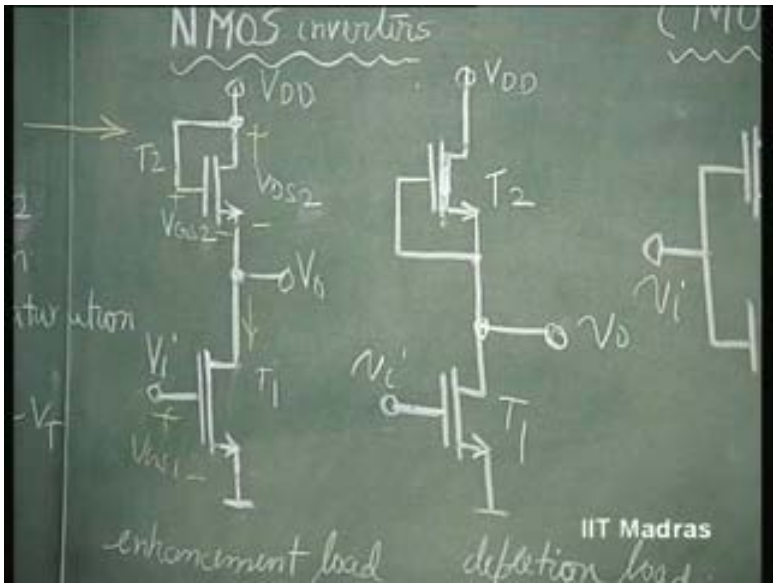

But, the voltage is going to start now from V D D. Why? The T 2 is in the triode region for V G S equal to zero. So, T 2 is in the triode region. T 1 is in the current saturation region. Up to V T, this will be the case. Thereafter, what happens? T 2 will continue to be in the triode region. T 1 has now come out of off state.

It is in the current saturation region. Actually, this is T 2 in the triode region is going to be here. Here...sorry. T 2 in triode region in both these places. T 1 here is off and T 1 has entered current saturation. That means I D S 1 is going to be K times V i minus V T whole square. That is valid for T 1 like it happened here. But for T 2, it is going to be...is...this is going to be in the what? - triode region.

So, this current is, I mean, you cannot write it as 2 K, strictly speaking, because this characteristic is now going to be I D S equal to I D S S in the current saturation region, 1 minus V G S by V T whole square. This is the equation for the current saturation region of depletion type of MOSFET. Is this clear?

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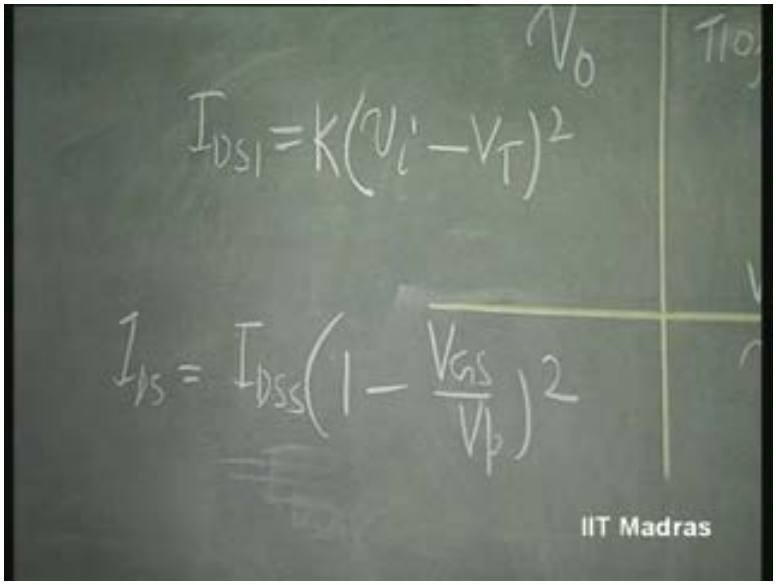

For the other region, that is, for the triode region, I D S is going to be twice I D S S. It is going to be similar. Mathematically, it is similar; into 1 minus V G S by V P into...now V D S and V P are opposite signs. So, we put for the magnitude of current this, because we have known the current direction. So, magnitude of current only we are interested in. Half of V D S by V P square.

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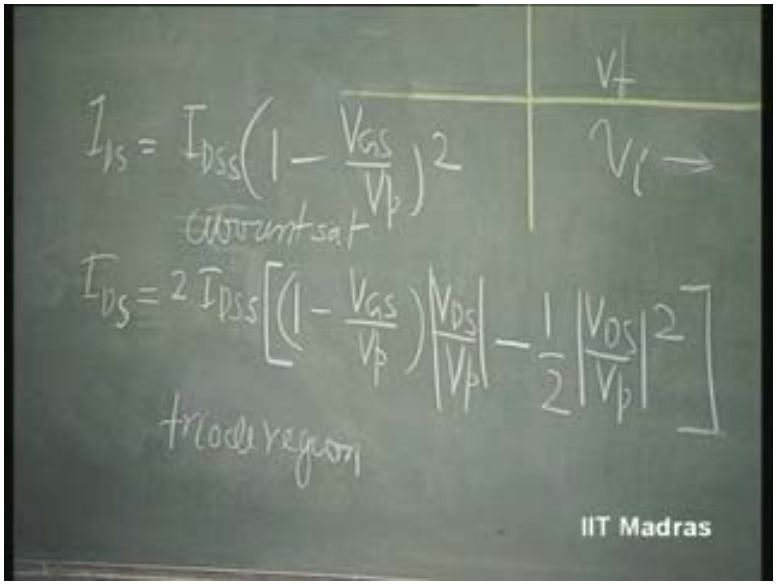

Now, this current is going to be equal to this current, I D S 2. V G S in this case is zero at all times. So, this is zero. This into V D S minus V P. That is all. 1 into V D S minus V P.

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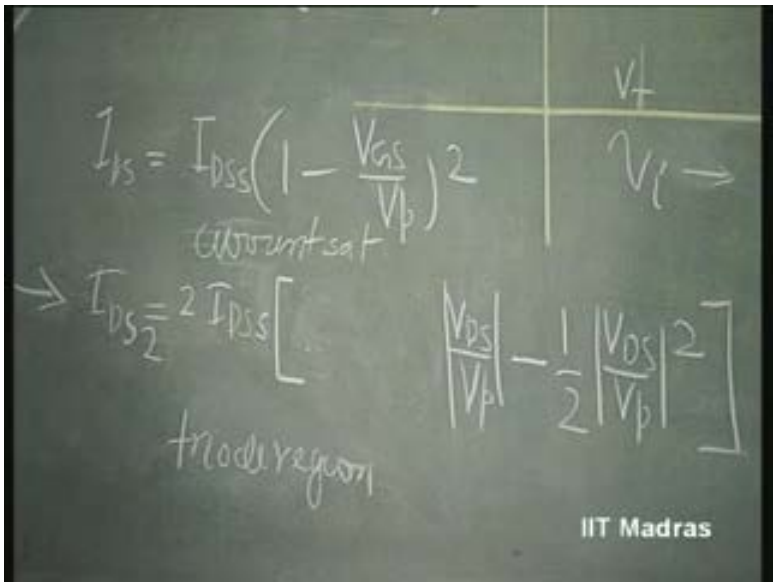

And V D S, for this V D S is going to be V D D minus V naught. This also is going to be V D D...square. So, this is the equation that one has to satisfy.

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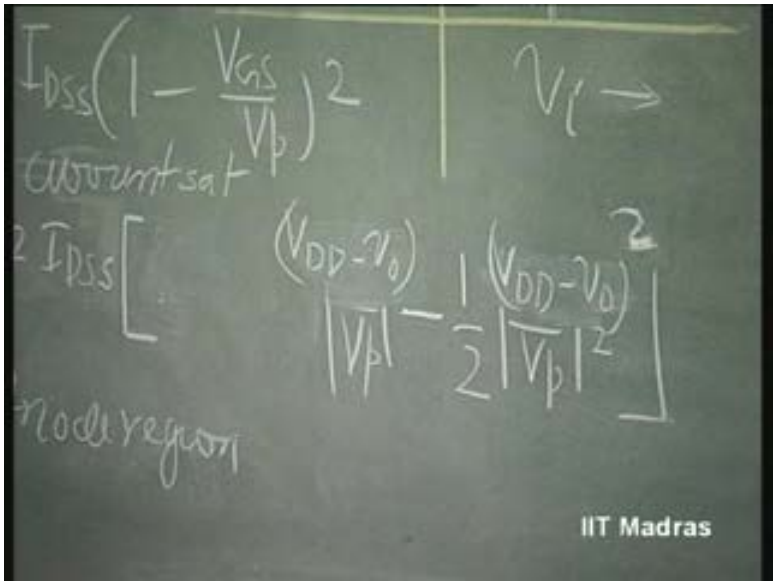

Once again, you will see that this is highly non-linear. You have square here, square here, but no square here. So, this is non-linear.

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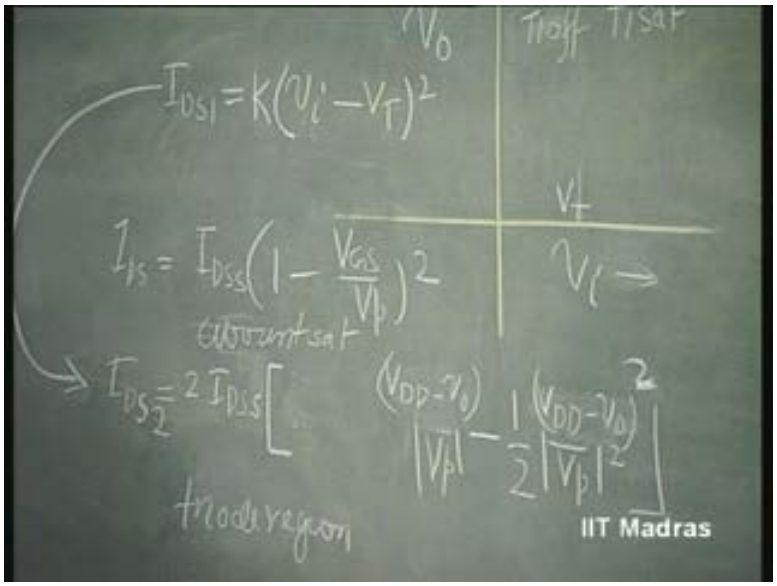

So, this is going to follow some kind of relationship like this; and then... This voltage is keeping on decreasing. Now, T 2 can enter the current saturation region; T 1remaining still in current saturation region. T 2 can enter current saturation region; T 1 still remaining in current saturation region. So, that is the point where, obviously, the current in this is going to remain constant at I D S S thereafter. So, this is going to remain now constant at I D S S. This current is going to remain constant at I D S S and this current is going to be equal to... I D S 1 equal to K times V i minus V T square is going to be satisfied.

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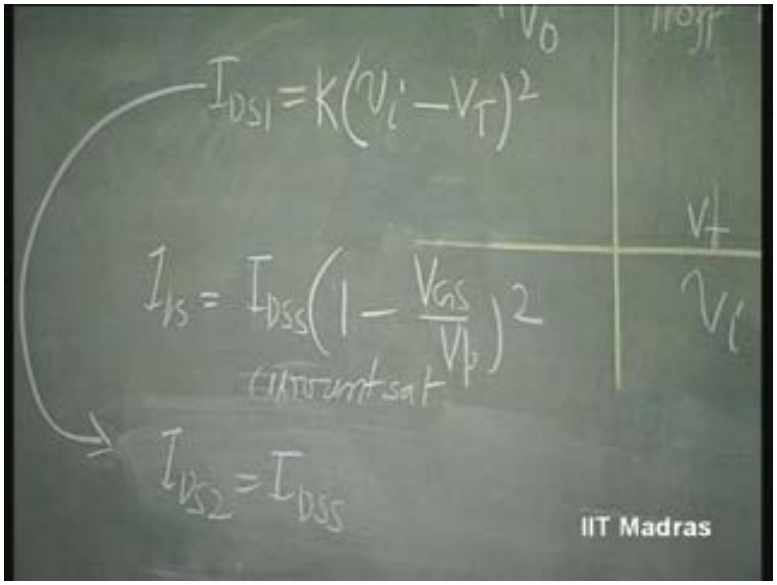

So the... What is going to be the gain? It is going to be a current source. As long as this is remaining constant at I D S S, this is going to act like a current source. The gain is going to be infinity, strictly speaking. What is the slope therefore? This is going to be almost vertical here.

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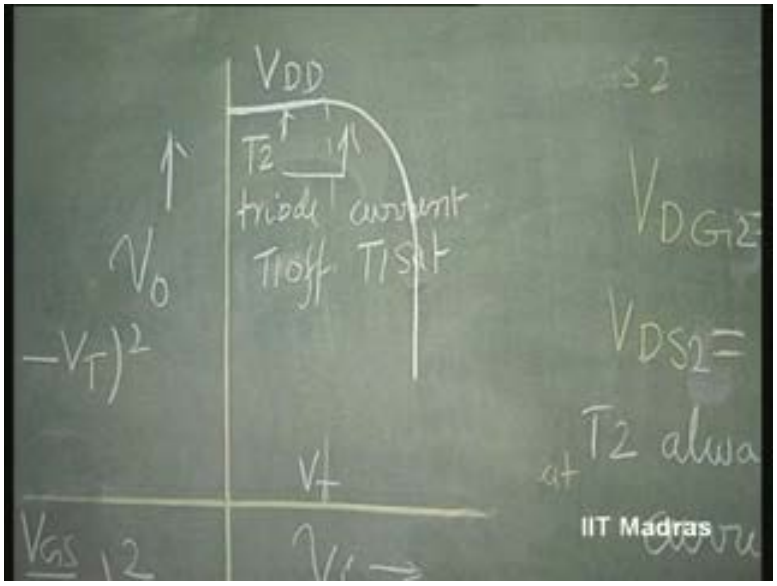

This is going to be the case, as long as this particular thing is going to remain in the current saturation region. A point will reach when this transistor will enter the triode region. This is going to enter the triode region. So, this is going to go on until the transistor enters the triode region.

Once again, we can draw the same line; that line remains the same. That is corresponding to V naught equal to V i minus V T; and thereafter, the output voltage is going to remain... This is I D SS; depends upon...this is going to act like some resistor here. So, it depends upon the potential that this develops here. So, output voltage is going to depend upon this; and again it is going to be non-linear.

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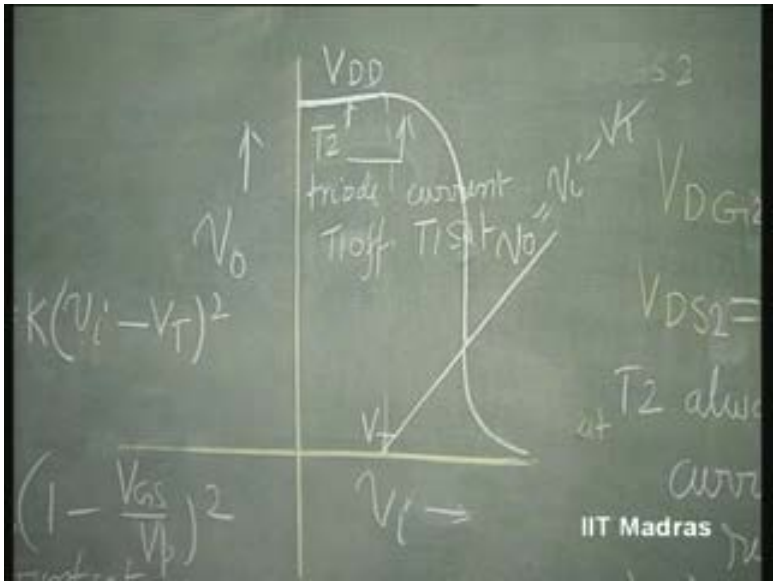

So, this is the advantage of this scheme. When the both, this and this, are in the triode region, we have this acting as a high gain amplifier. So the slope is going to be infinity and the transition is going to take place like this. Unlike this situation where the slope depends upon the K 1 by K 2 ratio, here, we have the slope becoming equal to infinity.

We had seen that this region, the transition region, where both T 1 and T 2 of this inverter remain in the current saturation region is a very important region because that is the region, active region in which gain is very high, infinity. Now in actual practice, obviously, gain is not infinity because this, when it enters current saturation region as well as this entering current saturation region, there will be this R D S of each of these FETs; R D S 1 and R D S 2 coming into picture. So R D S 1 parallel R D S 2 into g m of the FET is the actual gain.

Under this case, when we had assumed that these are ideal current sources and sinks, the gain looks to be infinity. So, this is that region. Further, the T 2 triode has entered into current saturation region here, where both T 1 and T 2 are in current saturation. See this transition, how do we obtain? That is the region where V G S is zero. When V G S is zero

for the transistor T 2, the transistor enters the triode region, when V D S becomes equal to V P. V D S in this case is V D D minus V naught becomes equal to magnitude of V P.

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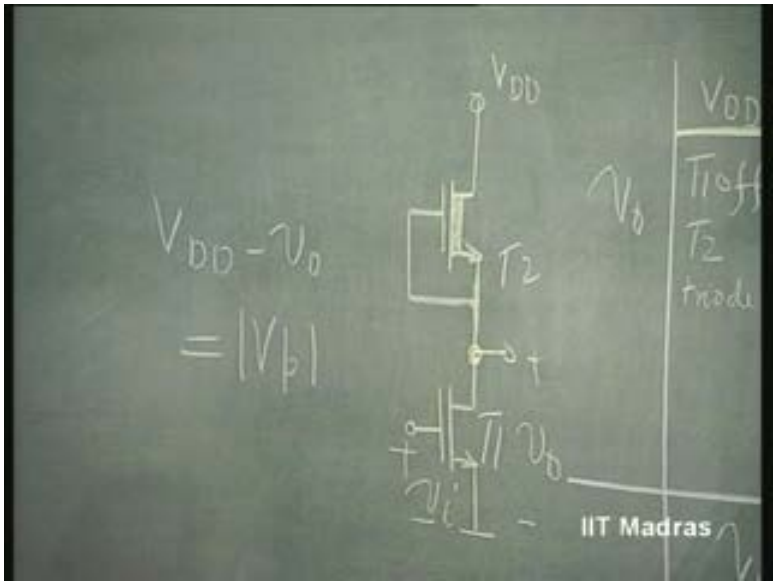

So, this is the point; that is, you can now find out from this the value of V naught at which the transistor T 2 is entering the triode region. That is, when this V D S becomes same as V P, V D S being equal to V D D minus V naught; becomes equal to magnitude of V P. Is it clear?

Now, that is something that you have to remember. That is, this point. This point we have already seen is the point corresponding to V naught equal to v i minus V T where T 1 goes from current saturation to triode region. Thereafter, of course we have this. This completes the characteristic of the inverter.

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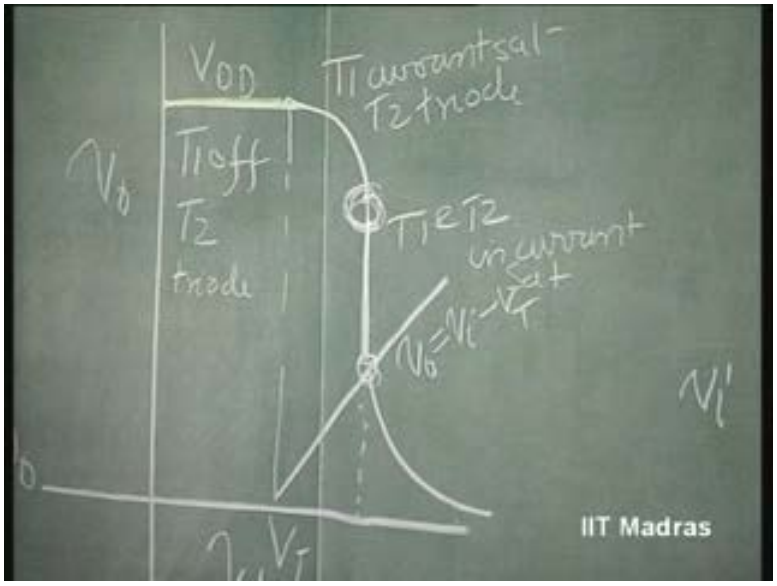

I would like you to evaluate the transfer characteristic for this portion where the entire amplifier is in saturation; equating the...for T 1, current in the triode region to the T 2, current in the saturation. That is of course I D S S.

Now we go to an important basic building block; that is the CMOS inverter as shown here. So, unlike the other inverters which used the same type of enhancement MOSFET, either n or p, here we are using NMOS and PMOS in combination; the complementary MOSFET.

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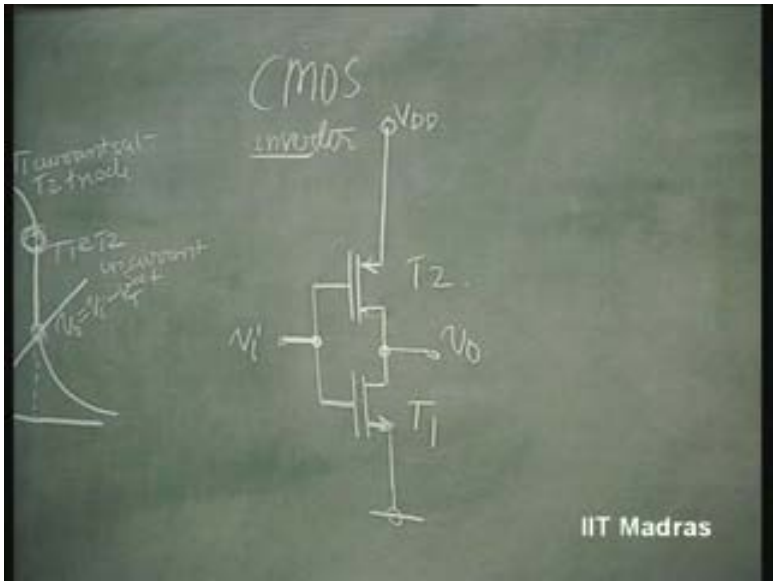

This is the most important basic building block for VLSI design. Also, it is used as an inverter in analog circuitry. Let us see what it is. Here, just as we did the analysis in the case of these NMOS circuits, we can also do the analysis in an identical fashion and come up with the transfer characteristic. So, let us once again obtain the transfer characteristic for this. V naught. Now you have become almost familiar with the routine that we are going to go through. When V i is less than V T, T 1 is off; when V i is less than V T.

Therefore, T 1 is off. T 2...because V i is less than V T, no current is flowing through this. As far as T 2 is concerned, this voltage is going to be extremely small; drop across this. V naught is going to be very nearly equal to V D D. T 2 is going to be in the what? - triode region. Please see...V i is connected to, let us say, ground, zero. This is conducting; this is conducting. There is considerable amount of voltage applied to this. This is conducting.

It is only that this is not conducting, but this is in the triode region. So, T 1 is off. T 2 is in the triode region. If V i goes very nearly up to V D D, this can be made to go off. So, when V i is zero, T 2 is conducting. But T 1 is forcing the current to be zero because the

currents in these two must be same. Now, as long as V i is less than V T, T 1 remain, will remain off; and this is going to be at V D D.

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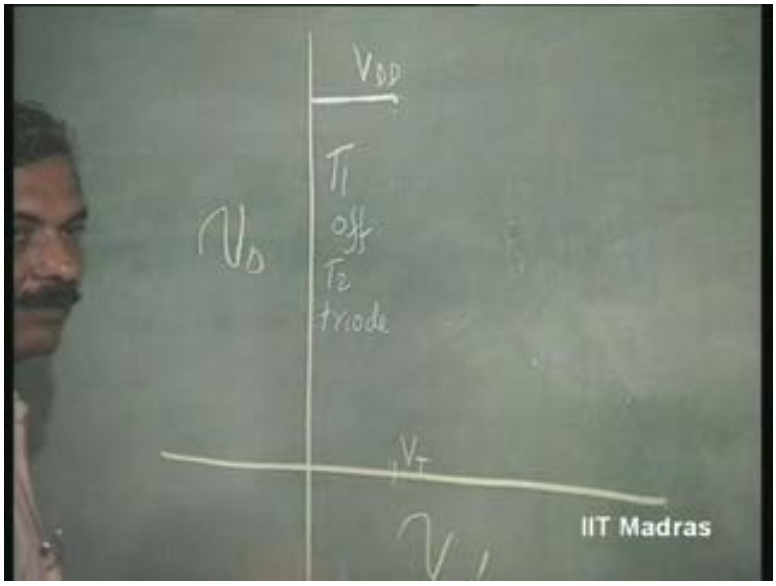

So once again, we are having the high level going almost up to V D D. No problem. Thereafter, T 1 starts conducting. T 1 is going to be in the current saturation region because V naught is very nearly equal to V D D. So, T 1 is in the current saturation region but T 2 still remains in the what? - triode region. So, characteristic is going to be non-linear.

Because T 2 has remained in the triode region and T 1 is in the current saturation region, we can write down the equation, I D S 1 is equal to K 1 into V G S 1 which is V i minus V T 1, we will call it; square. This is in the current saturation region.

This is equal to... Now we have to be careful. We will only out the magnitude of current. Consider it as positive I D S 2. This is equal to...now, this is in the what? - triode region. So, 2 K 2 into... now let us say, we have to keep this positive all the time. So, first you get V G S 2. Now, V G S 2 is V i minus V D D. But we will put V S T 2 which is positive. V

D D minus V i minus magnitude of V T, because this is negative. So V T 2. This is negative. So now, this remains positive. Is this clear?

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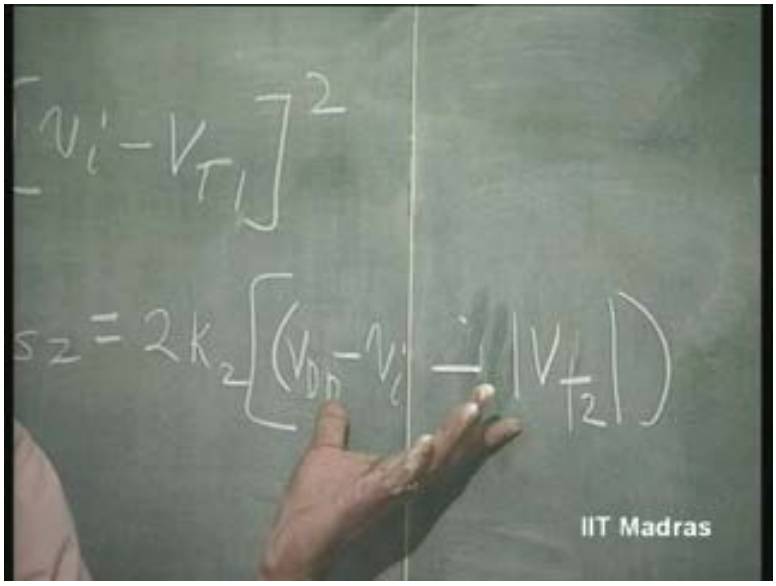

Or else, you should have put it as V G S which is V i minus V D D minus V T 2. That is all; sign being taken care of properly. Here in order to prevent any confusion, I am putting all quantities as positive; V D D minus V i is the positive voltage, minus V T 2 into what? - V D S. Again, it is V naught into V D D whereas we will put it as V D D minus V naught, minus V D D minus V naught whole square by 2. Is this clear?

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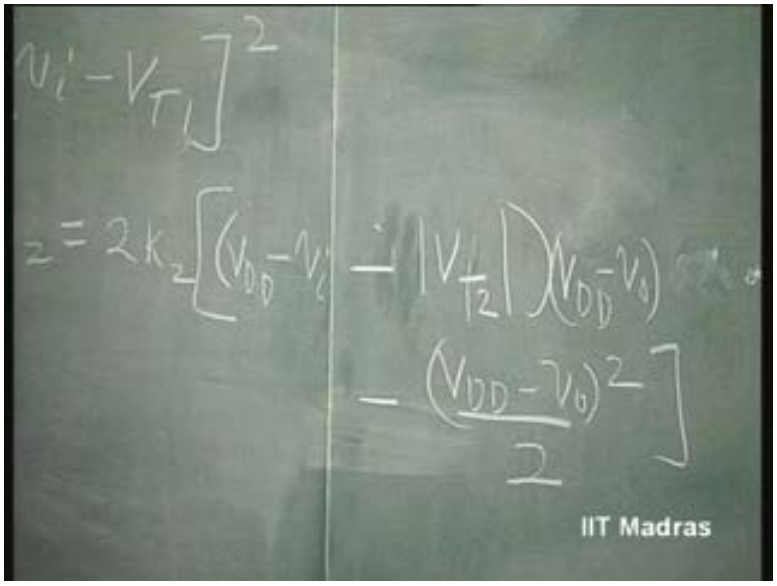

So, there is not going to be any confusion here. Otherwise, you stick to the original equation with signs being properly taken care of. So, this equation will give you some kind of non-linearity here. Up to a point, this will go on. The triode region, T 2 remains, until a point is reached at which it will come into current saturation; that we have to find out.

What is that point at which T 2 comes out of current saturation...triode region into current saturation. Let us see. That is the point where V D S which is, we will put it as V D D minus V naught. This voltage becomes equal to... V D D minus V naught. Actually, V G S; we will put it as V S G. V D D minus V i minus magnitude of V T 2. No problem. So, this is the point at which this is entering current saturation region.

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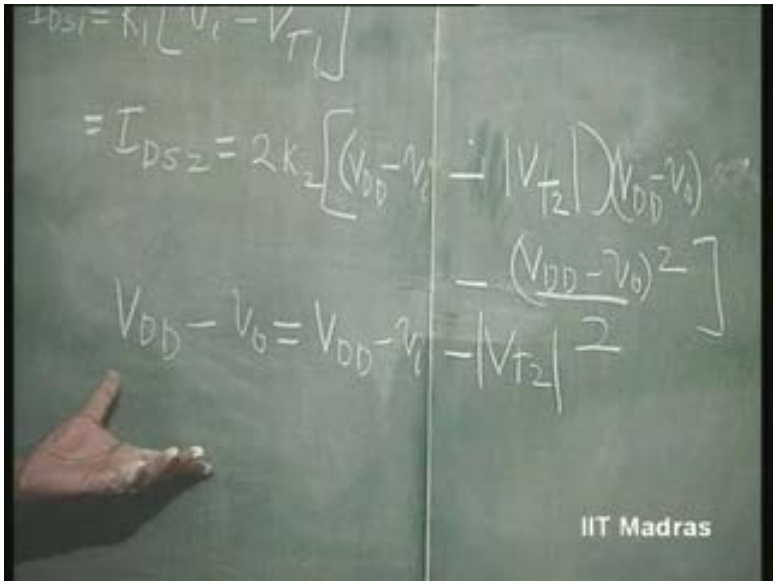

What is this? We can cancel V D D, this... So, this is nothing but V naught equal to V i plus magnitude of V T 2.

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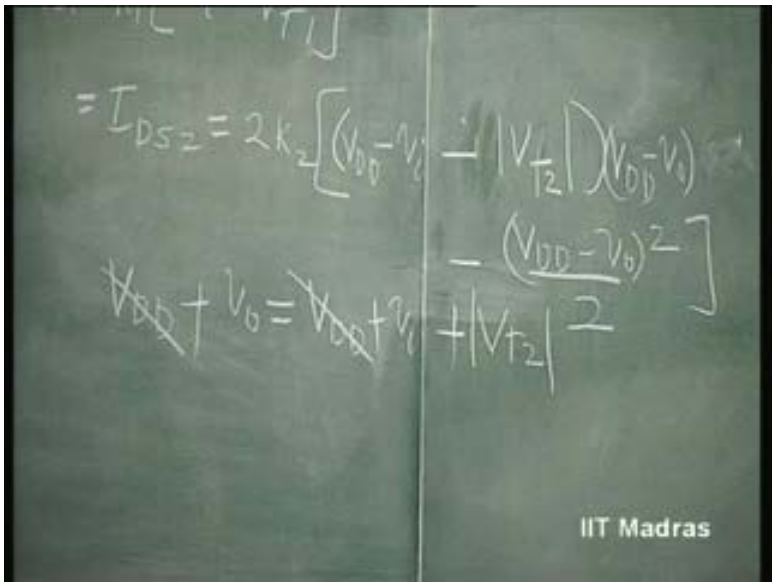

Another line which is going to...if this is V T 1, the intercept here is going to be at V T 2, when V i is equal to zero; and it will go on like this. This line is going on like this. This line is V naught equals V i plus V T. This line which was earlier itself known, V naught

equals v i minus V T 1. So, within this region, both the transistors are in current saturation region.

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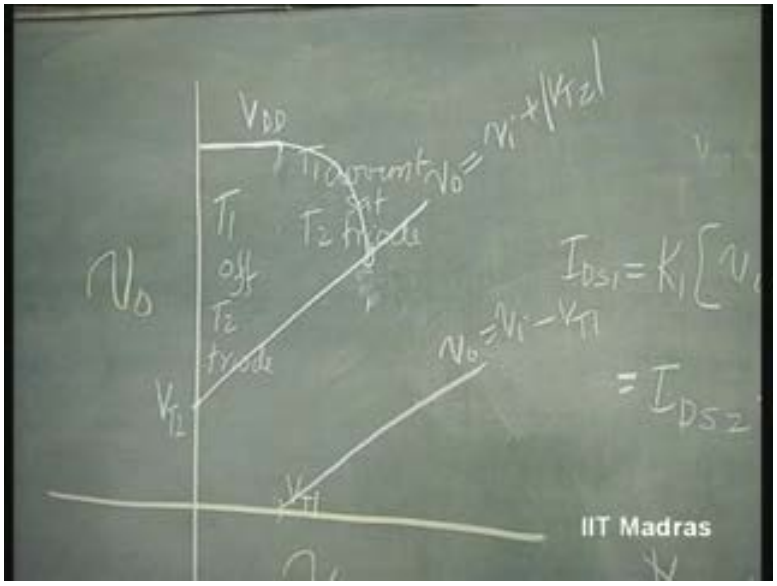

That means this equation is no longer valid. I D S 1 equal to I D S 2. This is equal to T 1 and T 2 in current saturation region; and therefore it is going to be infinite gain; slope is going to be infinity.

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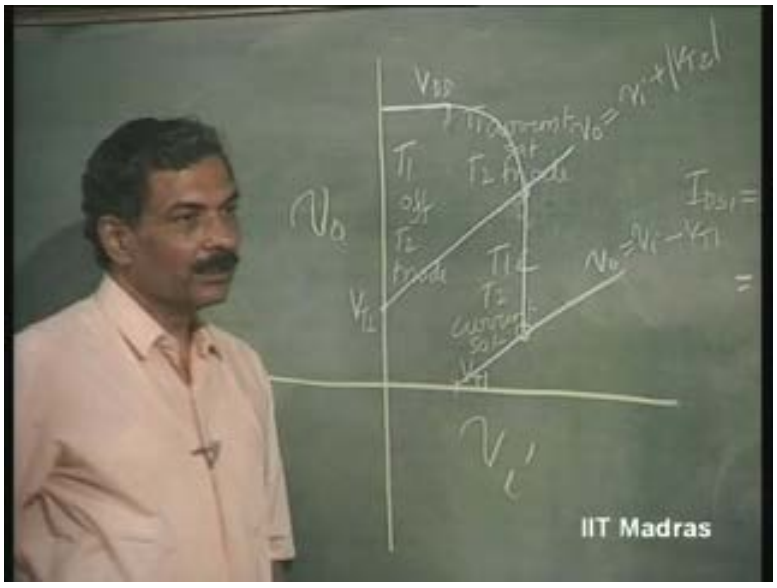

This will go in until the...now, lower transistor T 1 goes into triode region. So, what is that I D S 2? It will be K 2 into V i of... There is this, which is strictly speaking... How much is it? This V i, this is actually,...which is nothing but V G S 2, which I am, had been putting as V D D minus V i minus magnitude of V T 2 whole square.

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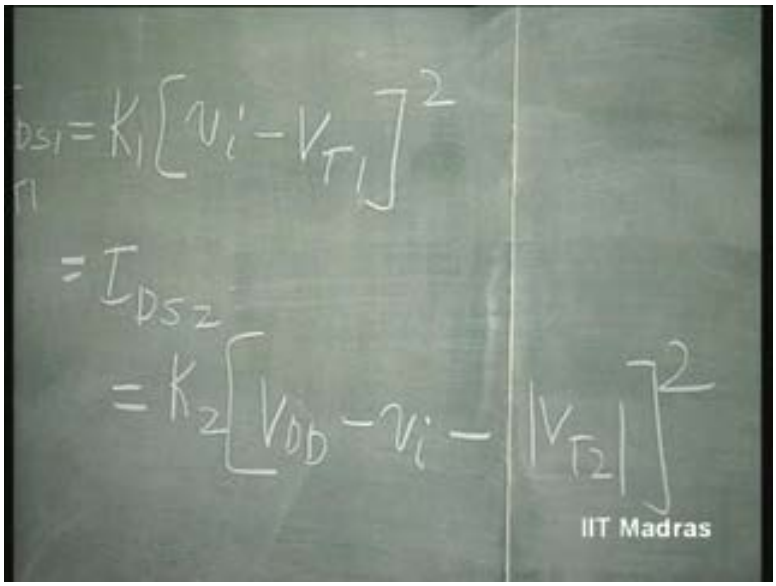

So, you can see that this is perfectly linear. This is going to be perfectly, in this sense, linear; and the slope is equal to infinity; and this is the region where the amplifier is in active region.

Now, you can also, from this equation, find out the value of V i at which it will remain with slope equal to infinity. So, you can find out from this equation the value of V i.

If K 1 is equal to K 2 and V T 1 is equal to V T 2, you can show that this will occur at exactly equal to V D D by 2. If K 1 equal to K 2, V T 1 equal to V T 2, this transition will occur exactly at V D D by 2. That is the ideal inverter characteristic, where the transition from high to low occurs exactly at V D D by 2. Thereafter what happens? This transistor enters the triode region. This story is exactly similar to this region.

Since it is symmetric, it is exactly similar to what happens in this region. So, I would leave it to you to complete this. Ultimately, this as it reaches what value? When this reaches V D D minus V T, the upper transistor goes to off state. So, V D D minus V T 2... The upper one goes to off state and output is going to be zero. No current; and up to V T. So, this is a charac... complete characteristic of this CMOS inverter and it is the closest to an ideal inverter.

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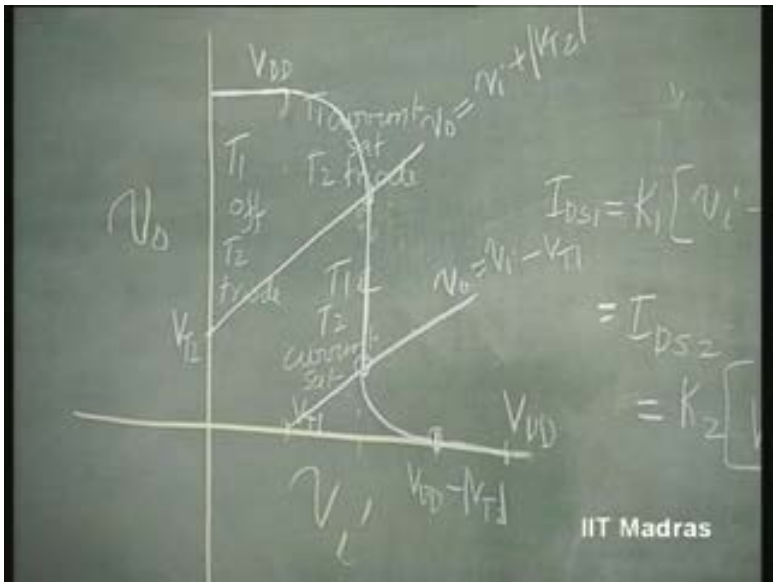

There is no other inverter which is approximating to the ideal inverter. Gain is infinity and the transition, if they are perfectly symmetric, if K 1 is equal to K 2 and V T 1 in magnitude is equal to V T 2, then it is going to transit at V D D by 2. Correspondingly, you can find out for this value of V i, what the V naughts are. We will get the...for...from this, you will get one value of V naught and from this you will get another value of V naught.

So, I would like you to complete this and obtain all the critical points in this.