Electronics for Analog Signal Processing - I
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Lecture - 36
Current Source and Current Sink

So, in the last class we saw there is a need for current sources and sinks in biasing and acting as active load, to get rid of resistors, which I said is going to limit the performance of our amplifiers, particularly in giving us good common mode swing, good CMRR and low current operation.

So, let us now see how this can be done using a diode. A transistor connected as a diode; that base collector shorting makes the transistor act as a diode for external use; but internally it is acting as a transistor.

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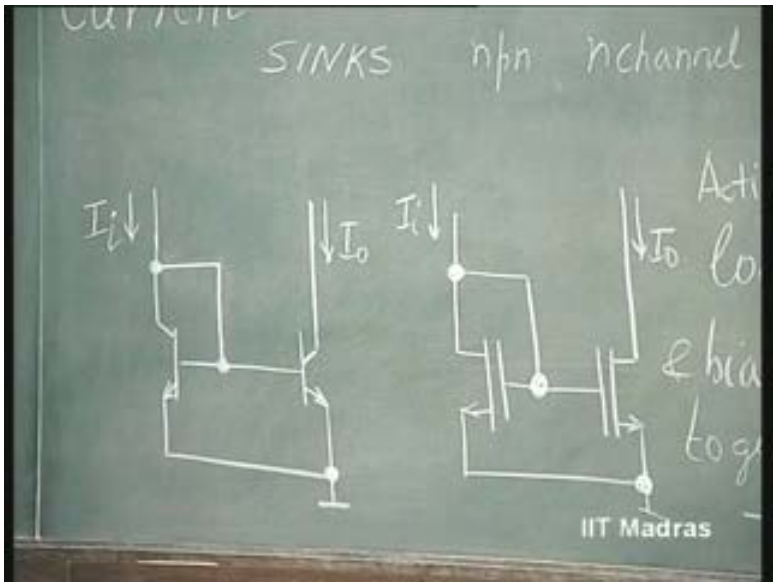

So, that develops a voltage. So, if I pump I i, this current I c is going to be very nearly I i because this is I c by Beta and this also is I c by Beta; and the current drawn from this apart from I c is twice I c by Beta.

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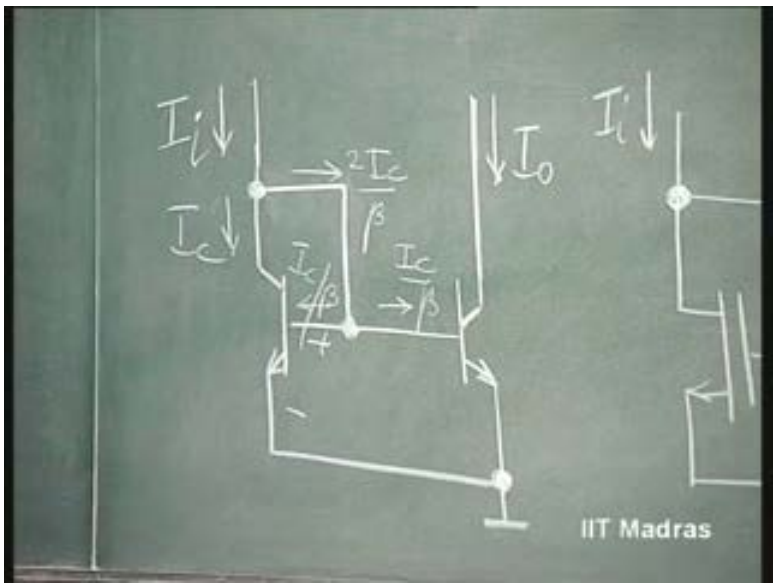

In this case, therefore, I i is going to be equal to I c into 1 plus 2 over Beta. So, Beta being very large, this is very nearly equal to I c, for Beta much greater than 1.

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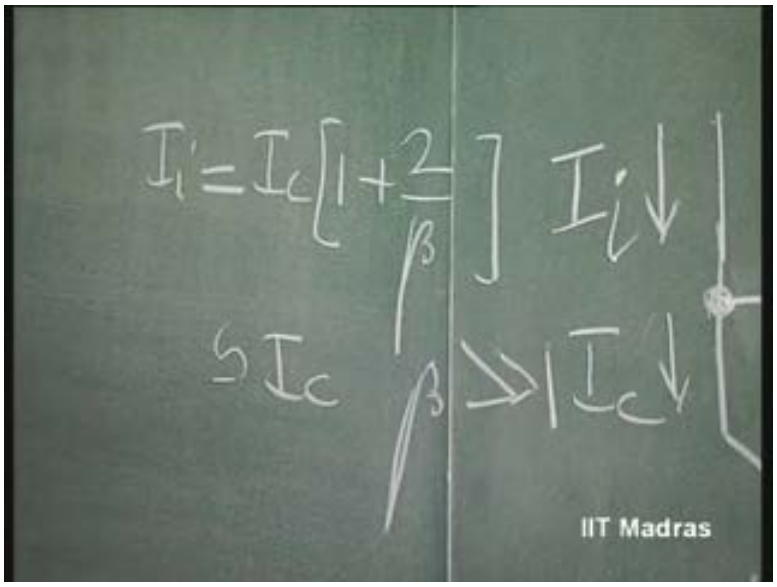

This is the case with these N P N transistors of integrated circuits, whose Beta is normally in the range of 200 to 300. So, we can in fact therefore get a current source here whose output impedance is r c e, which is of the order of mega ohms. It is nothing but a common emitter configuration. So, r c is the output impedance.

Now, this can be done merely by using one single resistor to convert the voltage to current I i. The same thing can be done using enhancement type of MOSFET. Important. It is... it should be enhancement type of MOSFET because just like this, if I short the drain to gate, V D G is zero... If V D G is zero, V D S...in this case VD G is zero. So, V D S is always equal to V G S. V D S is always equal to V G S in this configuration which means only when I use enhancement type of MOSFET, this transistor is going to be in the current saturation region.

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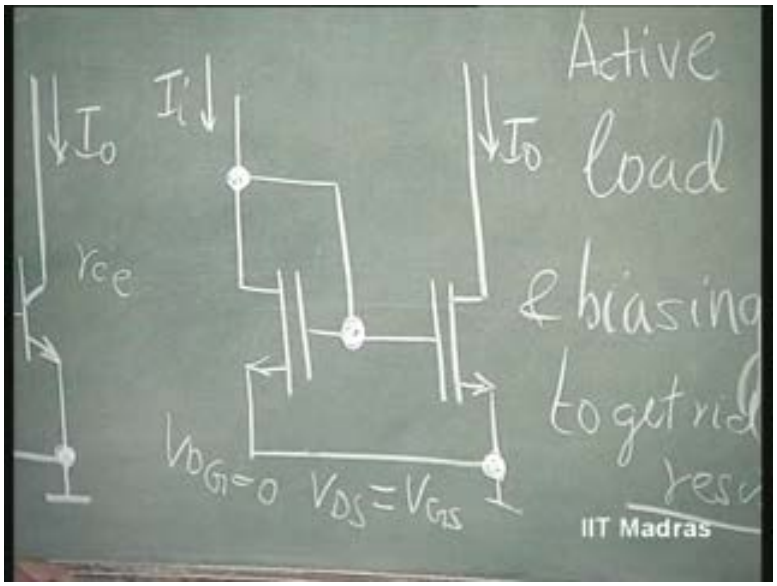

What is current saturation region? V D S should be greater than V G S minus V T is the current saturation region; whereas, we have in this configuration, V D S being always equal to V G S. This means this is permanently in current saturation region, which is good.

But, that is not the case when we use, instead of enhancement type of MOSFET, JFET or depletion type of MOSFET. That will be tamp...always in the triode region and therefore we are not going to use this kind of current mirror; it is not possible in depletion type of MOSFET and junction MOSFET. This is applicable only in the case of enhancement type of MOSFET.

So, current mirror is not existing in JFETs and depletion type of MOSFETs. The current mirror now obtained in this case is...obviously, there is going to be no gate current. So, I D S is exactly equal to I i in this case because there is no gate current; and that is reflected as I naught.

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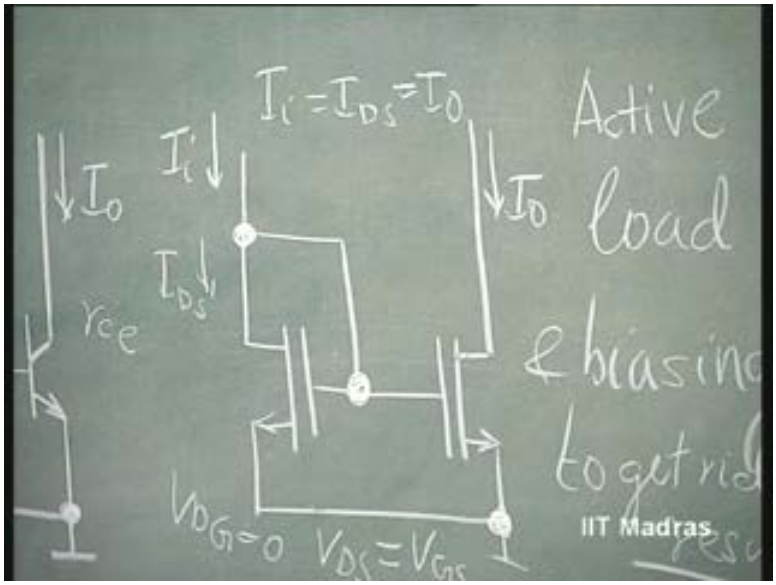

Here, I c is equal to I naught. I c is equal to I naught at all times; but I c itself is approximately equal to I i; whereas here, it is not the case. I i is equal to I D S equal to I naught. But for sustaining any current here, V G S may be always greater than point 6 because here it should be greater than the threshold voltage V T, which may be of the order of a volt or so; whereas in this case, it is only point 6 irrespective of the value of current. Point 6 to point 7. So, that is the difference. Here, it may be fairly high voltage which might have to be subtracted from the V D D which is going to appear across the

resistance that is going to fix up the current I i. So, that is the difference; but otherwise, I can therefore derive any number of what? – any number of current mirrors, current sources, using this voltage as the reference. It is not going to affect the relationship; whereas such is not the case here.

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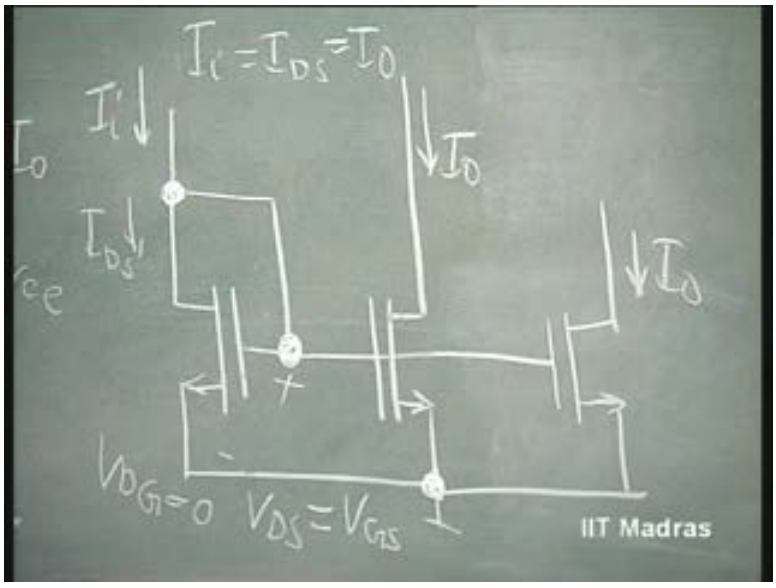

This number keeps on increasing. So, the error keeps on increasing in the case of bipolar structure. In this case therefore, I can generate a large number of current sources at no expense, no additional expense, simply by using this as the reference. So, this is a great advantage in the case of MOSFETs. There is no need for any resistor to be used at all for biasing. Fine. Now, can we come up with a configuration now that we know how to bias these transistors?

This transistor obviously is biased at I naught very easily now; whereas using a single supply, I have to use minimum of three resistors to bias a transistor in a stable fashion. Here, by using just one resistor, I am able to bias this transistor in a stable fashion at a current of V C C minus V gamma divided by R. This is the...this is I i. This is very nearly equal to I c.

So this current, I c or I naught is very nearly equal to...this is equal to I naught.

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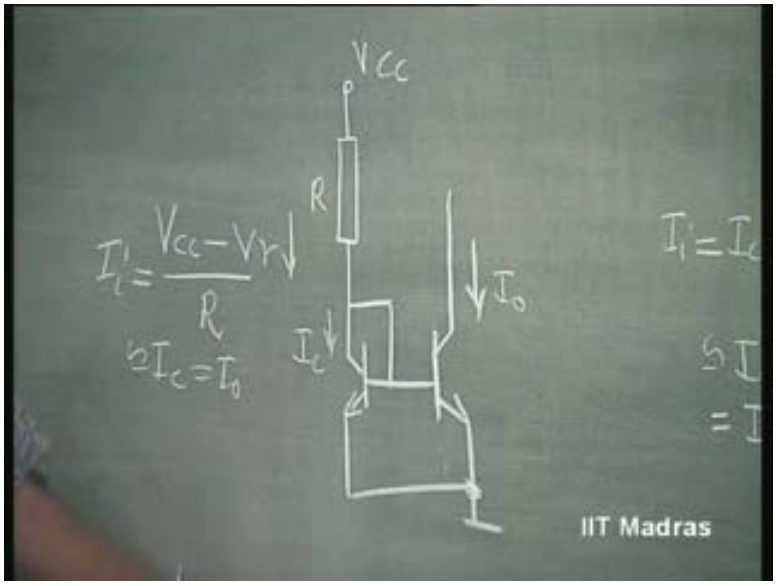

So, we can see this ease of biasing this kind of a structure. It is common emitter; emitter is grounded. There is no need for bypass capacitor at all here. In a three resistor configuration that we used earlier, we had to put a bypass capacitor across r e. We wanted to fix the emitter current; so we used r e, r 1 and r 2; as against this, here we use a single resistor to bias this transistor as a common emitter amplifier without any problem. How about the load? I can connect a load like this, R c. So now, this can have the input fed directly here.

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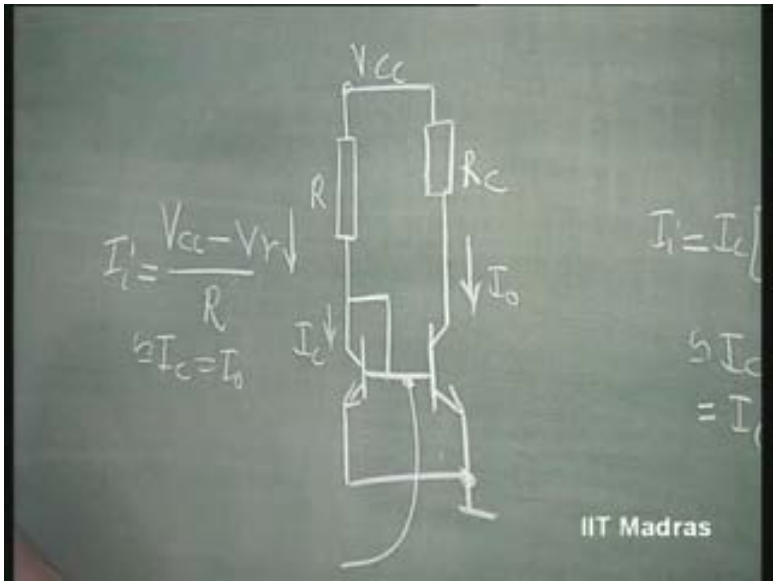

Input can be fed here and output can be taken here. This is a common emitter amplifier biased at I naught. I naught, I can fix at any value I want, independent of the transistor. So you can see the ease with which a common emitter amplifier can be used, biased, using current mirror concept.

But, there is a problem here. If I feed signal here, this impedance seen here is r e into Beta plus 1. This r e into Beta plus 1. This common emitter amplifier input impedance. But this impedance here is nothing but r e itself because it is nothing but a diode. Base is connected to collector. So basically here, the current, if you just remove all this, the current drawn is going to be the current outputted here. So, this current is the same as this current, if you remove this; which means this is acting as a diode, forward bias diode, whose impedance is r e. So here, on this side, it is r e; on this side, it is r e into Beta plus 1. So here, you have an impedance of r e; here you have an impedance of r e into Beta plus 1. This is your amplifier; this is some biasing circuit.

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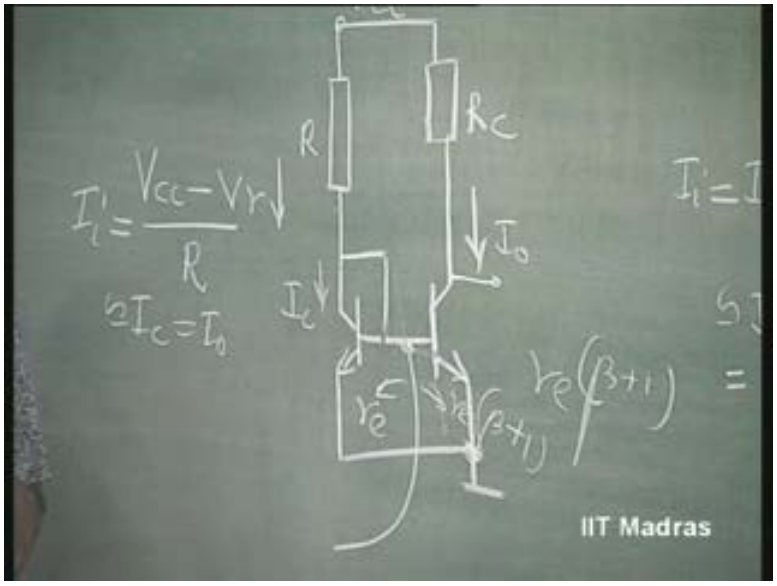

What does it mean? The biasing circuit is taking more signal current than the amplifier. So, this is the disadvantage. This is going to load your signal generator; and if the signal generator has a source impedance, that is going to bring down the signal level here. So, this is the disadvantage.

What to do about this? This can be fairly easily tackled. So, what...we have high impedance here; we want a high impedance from here. So, what I do is put a series resistance. I am feeding this. I am going to feed this signal here. Put a series resistance R B so that R B is as much as r e into Beta plus 1 or higher. So, R B is made higher than r e into Beta plus 1 so that this loading is reduced. If I do put a resistance like this, I must put a same resistance in series with the other base. This is because this works by property of symmetry. If I put a resistance here, I must put same value of resistance here. So, this current mirror property is retained. So, I put that and connect the emitter to ground and now connect this this way and now short this to this.

So again you see, from this point, there is a base resistance and base to emitter junction. From this point also, there is a base resistance and base to emitter resistance; base to emitter junction. So, the current mirror action is exactly retained. I naught is same as I c. This is still valid.

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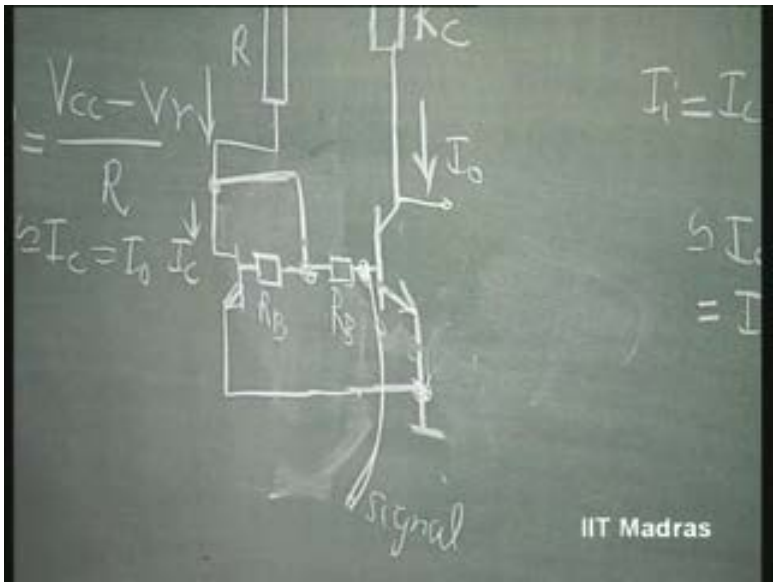

But now that the signal is being fed here, this is asymmetrically fed; so, this is going to act as the resistance R B and may be a low impedance from here to ground. So essentially, we have R D preventing loading of the signal generator. So, this is an arrangement to use this whole configuration as a common emitter amplifier. We can do this coupling here, capacitive, because signal input... So, at this point anyway, terminal has to be brought out in order to give the signal input. So, as a preamplifier, anyway terminal is going to be brought out; we can as well put a capacitor to decouple the D C from the signal.

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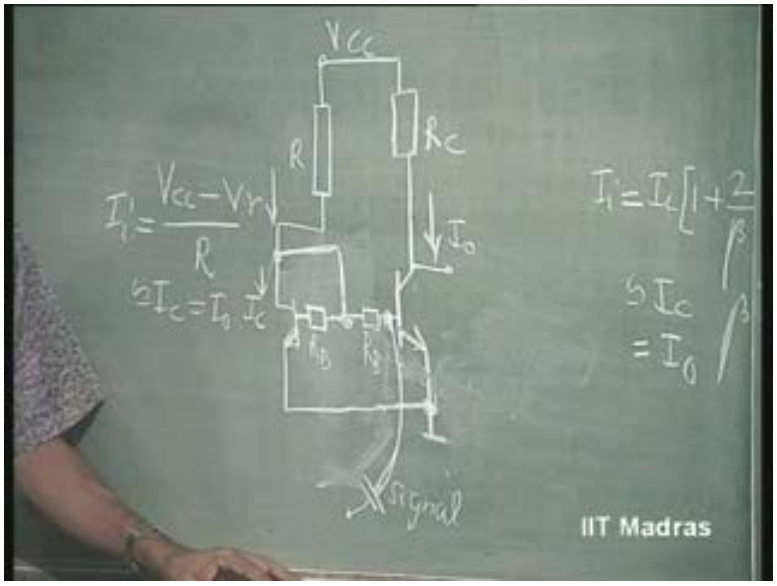

So, you can do capacitive coupling here and then use this amplifier as a common emitter amplifier. So, this is an alternative arrangement in integrated circuit to obtain what is called as your common emitter amplifier.

Now, as far as this is concerned, I want to increase the gain of this. The gain of this is... How much is it? g m into R c; g m being equal to 1 over r e; r e being equal to V T divided by I. Now, I want to increase this gain so that this is the highest. But I do not want to use high value resistance. So, what can I do? I can obviously replace this by means of a current source.

So, current source means, what kind of current source? I can use a p n p current source going in to an n p n current sink. Now, how do I make this work at the same current? What I do is I use a current mirror here. So, you can see that I am using a current mirror here. Theoretically speaking, if Beta of this is the same as Beta of this, then I can say that the current in this, if it is let us say I, I i, I i being now equal to how much? V C C minus 2 V gamma. This is one V gamma and this is another V gamma, divided by R. This, since it is carrying only the base current, we are ignoring the D C drop in R B. So, we are

assuming that this potential is V gamma. So, this is the current here and this current gets reflected here as I naught. I naught is equal to I i.

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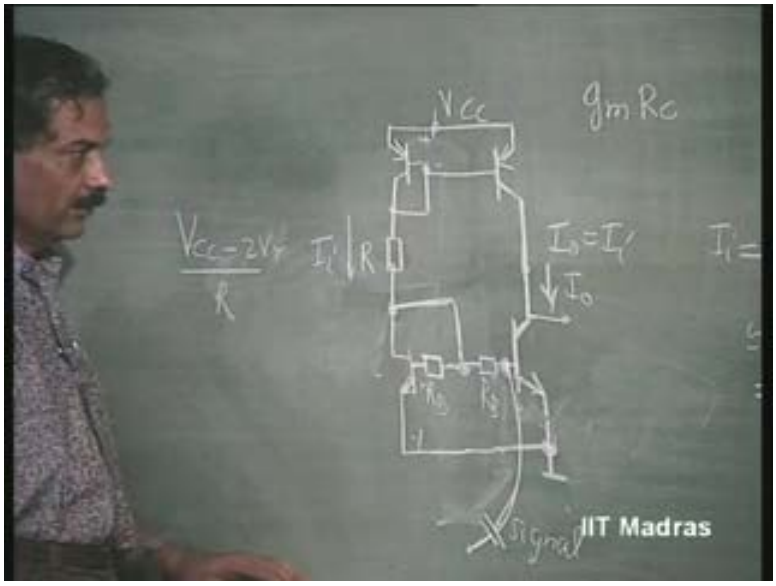

So, now you see, the load also is replaced by a current source. So, a current source can act as a load. I have got rid of the resistance. What is the D C drop? The D C drop is only V gamma here. The collector potential can vary as much as V C C minus V gamma. Until that time, this is going to act as a source. That means this collector potential can become pretty low. Even then, this is going to act as a high load resistance.

This collector potential, on what does it depend? Obviously, when I say this is exact reflection, if this is I naught, this also is I naught. Strictly speaking, these are identical. This should be exactly at half the supply potential. By some bad luck, if this reflection is not exactly I i and this reflection is also not exactly I i, there is a mismatch between the reflective pair.

So, this is demanding a current of, let us say, I i dash. This is delivering a current of I i double dash. So, that means, let us say, this is demanding I i dash which is different from I i; and this is delivering a current of I i double dash because of mismatch. Then, what

happens? I i dash minus I i dash, I i double dash minus I i dash should go into open circuit. It is not really an open circuit; in practice, there will be some capacitor. So, it will charge this capacitor and the voltage will keep on increasing until this current source ceases to be a current source.

That means the volt potential here will become higher than V C C minus V gamma, at which point, this goes to saturation and this ceases to be a current source; at which point of time, this can happily demand I i dash and that can be sunk into a saturated transistor. So, this ceases to function.

So, if there is a perfect match, then it is good. If there is mismatch, there will be an offset voltage which goes on drifting until one of the two go to saturation. Either this will go to saturation or this will go to saturation. When will this go to saturation? Suppose I i dash is less than...I i double dash is less than I i dash, then the current will be in the opposite direction and this will get negatively charged. And it will keep on increasing until this goes to saturation.

Therefore it will be perfectly biased only when I i double dash is equal to I i dash. That can only happen if this I i is exactly reflected as I naught on both these sides. In practice, it can never happen. So, this combination very rarely works as an amplifier with zero offset or V C C by 2 as offset.

If I use symmetric supply, it should give you zero offset. If I use single supply, you should give...get biased at V C C by 2; but it will invariably go to saturation. But that does not matter. High gain amplifiers always behave like that. Output offset will be so large if it is very high gain that even with a small imbalance at the input, output will go to saturation. We will see that this is the case with all the operational amplifiers. Then, how do you use it?

When the signal applied is applied, it is going to be much more than the offset voltage and it will bring this into active region and make it work in the active region. That is what

is you are hoping for, because the signal to be applied to counter the offset is going to be extremely small. So, when you large...apply a large signal at the input, obviously, you are going to make the amplifier come out of saturation, work in the active region and may be the signal itself will drive it to the other end of saturation. So, it is...it can be made to work. So you do not get unusually worried if...when you are biasing this, this transistor goes to saturation or this transistor goes to saturation.

In simulation, this is something that always happens. Suppose you do spice simulation of this circuit and there is mismatch. Automatically, the quiescent point here is going to be such that it will make one of these transistors go to saturation. For it not to go to saturation, you must necessarily trim this current exactly and make it exactly equal to this current; and at that point of time, it can remain in a stable fashion. So, this is how you can sort of use this concept of current source and sinks in practical configurations.

Now apart from this, in a differential amplifier for example, we said this resistance can be replaced by a current sink. So, we will do that. Now, this r e is going to be replaced by a current sink made out of n p n current mirror.

This is the other application of these current sources and sinks. So, you can see here now that this is connected to the same V C C here; this is a current mirror and the current in this now is... How much is it? V C C plus V E E minus V gamma. V C C plus V E E minus V gamma; that divided by R. V C C plus V E E minus V gamma divided by R is the current I i.

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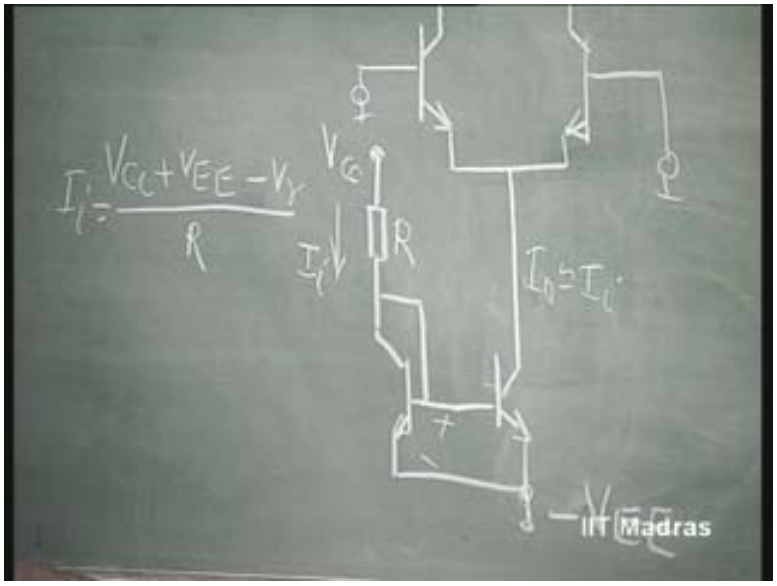

That I naught now is very nearly equal to I i, we have established. So, we can therefore fix it at any current we want by suitably selecting the value of R for a given V C C and V E E. Is this clear? So, let us say this is plus 10 volts; this is minus 10 volts. Then, this becomes 20 volts minus point 6. That means 19 point 4; and if I put, let us say 19 point 4 K, I get a current of 1 milliampere. So, as simple as that.

But, what is the common mode gain of this stage now? Earlier, the common mode gain of single ended stage was R C divided by twice R E. R E was the resistance that was existing here. Now, it is no longer twice r e, but it is going to be twice r c e. Since r c e is going to be of the order of mega ohms, we can see that A C is going towards zero.

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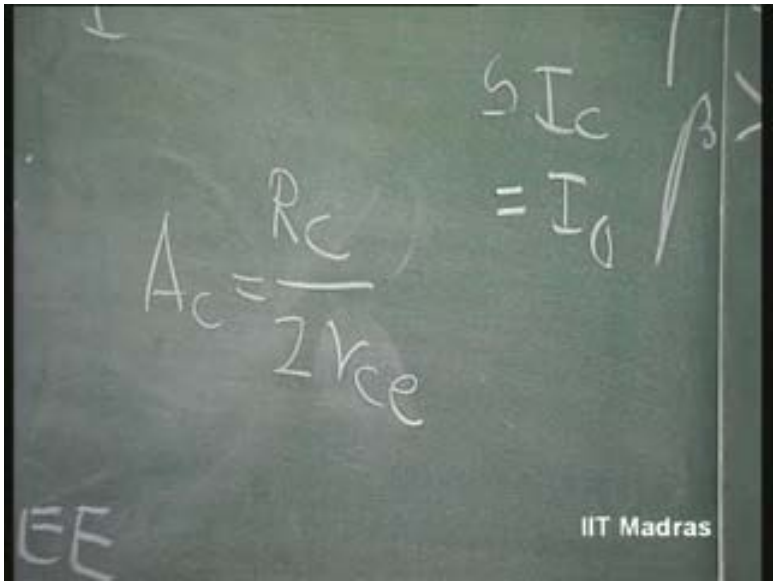

Earlier, R C was of the order of Kilo ohms and r e also was of the order of Kilo ohms. This was going to something like point 5 at most; it was decreasing to point 1 or something like that; whereas here, irrespective of the current that you are operating, this is going to...can be made very low. So, its CMRR gets boosted up enormously.

So, this is definitely very useful in improving the input stage CMRR. So, at the input stage, you will never use what? - a physical resistance. In a differential amplifier, it is always advantageous to use this current mirror and this uses only a single resistance to bias the transistor. So now, we have resistances here. Can we get rid of these resistances, is the question.

We just now said, felt, that in a common emitter amplifier, we had replaced it by a current source. Now let us see what happens. If I replace this by current source, I have the same problem. What is the problem? That, already biasing current is fixed by sink as I naught. If this was connected to ground, these have to be automatically equal to I naught by 2 and I naught by 2, if they are perfectly matched transistors.

That means current sink tells that current has to be fixed at I naught by 2. Now, current source cannot tell that it has to be fixed at some other value. It has to be fixed at I naught by 2. How do I do it? So, if you use two sources, that is not the solution. What you therefore use is a current mirror which will always say that current here is going to be same as current here; but what that value is going to be is determined by the input current and input current is I naught by 2. And that I naught by 2 can be easily reflected by this current mirror.

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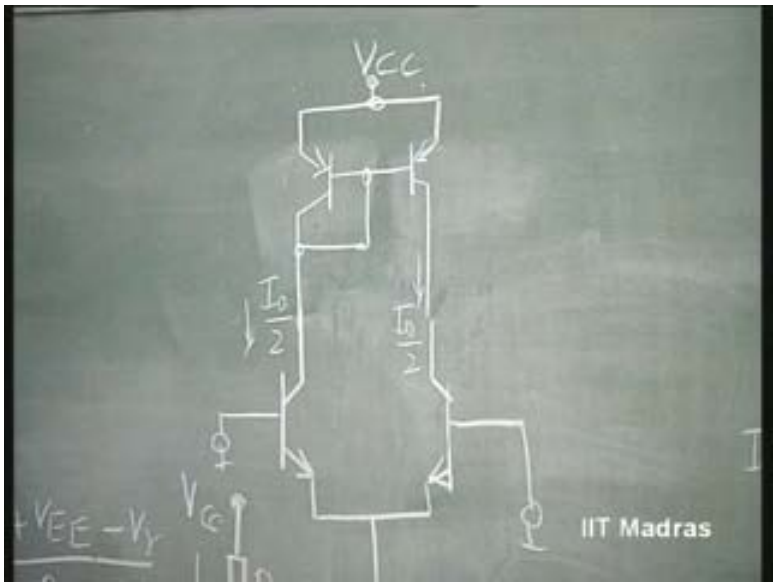

So, this source here is going to be not two sources, independent sources, but a current mirror which will develop nothing but a dependent source. So, if this is I naught by 2, this is going to be I naught by 2. So, using the current mirror as the load in place of two R Cs has facilitated nice way of biasing it.

This is particularly true...if the Beta is high, this is true; otherwise, what is reflected here may not be exactly same as this. And then again, you have the problem of offset coming into picture, which has to be compensated for. Is this clear? If I use, instead of this, a MOS current mirror, then there is no such problem; these two currents will always be seen, if I use a current mirror. In the case of a bipolar structure it is more so, because in

an integrated circuit, Beta of the p n p is not so high as the Beta of the n p n transistor. It is an order of magnitude less. So, this kind of reflection is not exact, when we use p n p current mirrors as compared to n p n current mirror. That itself is going to cause what is called an offset voltage, when you use even this current mirror. You might have to use what are called better current mirrors than this. That one we will discuss slightly later.

But under this assumption, now if you use a current mirror as the load, we have got rid of this resistance and what have we achieved? Let us see. When we apply a voltage v i, when we apply a voltage v i, what did we say? If this is I naught by 2 and this is I naught by 2, this will increase to what? v i divided by 2 r e. There is this 2 r e coming here.

This will decrease by v i by 2 r e. 1 over r e is nothing but g m. So, g m by 2 into v i and g m by 2 into minus v i; or actually, g m into v i by 2 and g m into minus v i by 2. That is how we have to integrate. So, the current here is going to increase by some amount; and this is going to decrease by some amount; and this is a current mirror. So, what will be the current here? I naught by 2 plus v i by 2 r e.

So, this is going to pump out to the next stage a current of how much? This is I naught by 2 plus v i by 2 r e. This is I naught by 2 minus v i by 2 r e. So, the current that is pumped out is going to be v i by r e. v i by 2 r e plus v i by 2 r e which is v i by r e. Is it clear

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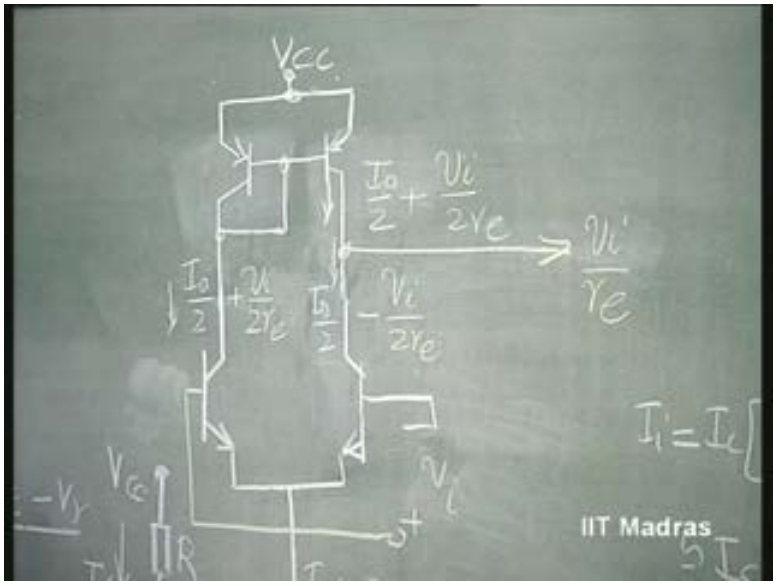

Therefore, if I...this is what is served. If you put the current source as the load, the gain is infinity. What does it mean? Entire signal current is going to be pumped in next stage. Hopefully, it has some input impedance which is finite; otherwise, gain is going to be infinity.

So, the moment you replace the load by current source, the gain is going to be g m into r c. r c is infinity and gain is infinity; but it is not practically infinity, because all these things have output impedances and that can be collectively put along with the input impedance of the next stage as the load.

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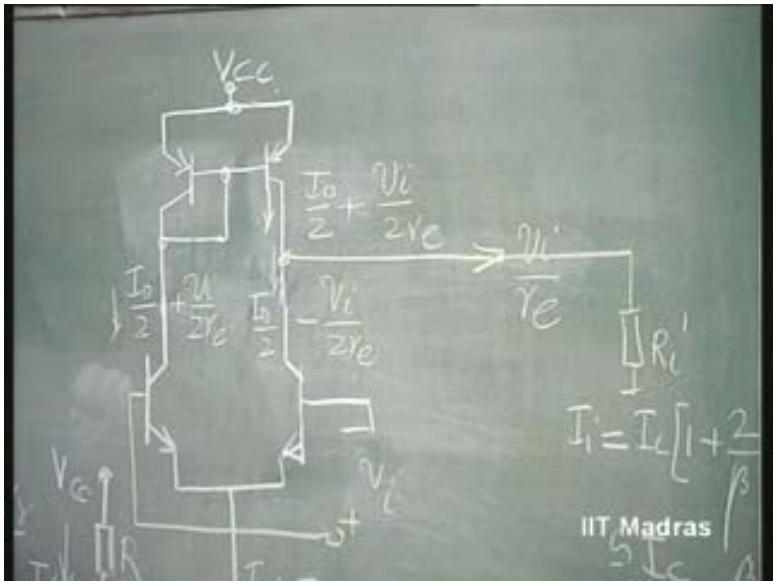

So, what is going to be therefore the gain r i divided by r e? Or, we can still consider this as let us say, R c effective, assuming that this is the output impedance of this, RC E of this and R C E of this and input impedance of the next stage, all put together as R c effective, which is going to be of the order of hundreds of Kilo ohms.

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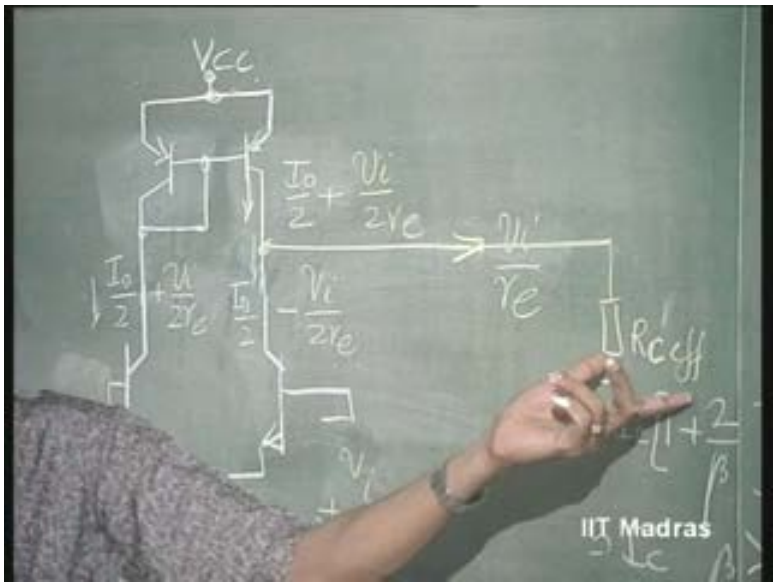

If these are all of the order of mega ohms, this will be of the order of hundreds of kilo ohms and therefore, the gain is going to be very high. And the entire thing is going to take up very little space because all these resistors are replaced by transistors. So, the input stage of the present day operational amplifier is always having this kind of active load and is always having this kind of current mirror biased.

Now, the advantage is that the gain is the highest possible and not only that we have tackled another problem now. What is the gain that you get? g m into R C effective. But that is a single ended gain. Earlier, g m into R C effective was the gain only when differential output was taken. So, this arrangement of current mirror is converting the differential gain into single ended gain. So, that means output has to be only taken with respect to this collector to ground and with that itself you are getting the gain as g m into R C effective.

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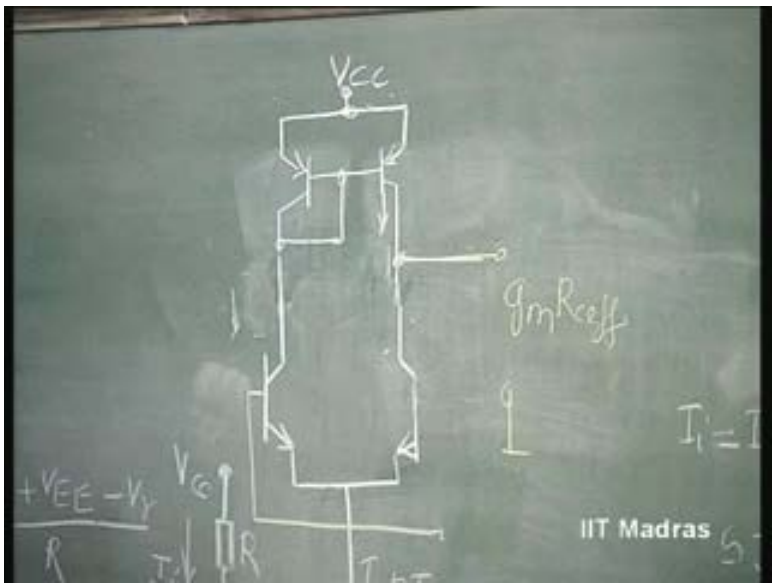

So, not only that you are getting higher gain because of active load usage, it is also giving you the original common emitter gain without necessarily taking differential output. For the single ended output, the gain is this.

Now, consider...as far as the input is concerned, that the input is a common mode input. When there is a common mode input, this common mode voltage can keep varying all the way up to what? - V C C minus V gamma because this potential can go all the way up to V C C minus V gamma. Until that point, we do not have any problem. So, you can see, this potential is already fixed at V C C minus V gamma. So, this is very nicely biased; and this potential can go all the way up to V C C minus V gamma before there is any serious problem of this transistor going to saturation.

So, that means common mode voltage on this side can go as much as very nearly V C C on this side. It is this voltage...if it is V c, this is V c minus V gamma and this is at minus V E E plus V gamma. So, this potential can become equal to zero. That means this can go down as much as minus V E E plus 2 V gamma; one V gamma down here, one V gamma down here. That means it can go down up to minus V E E.

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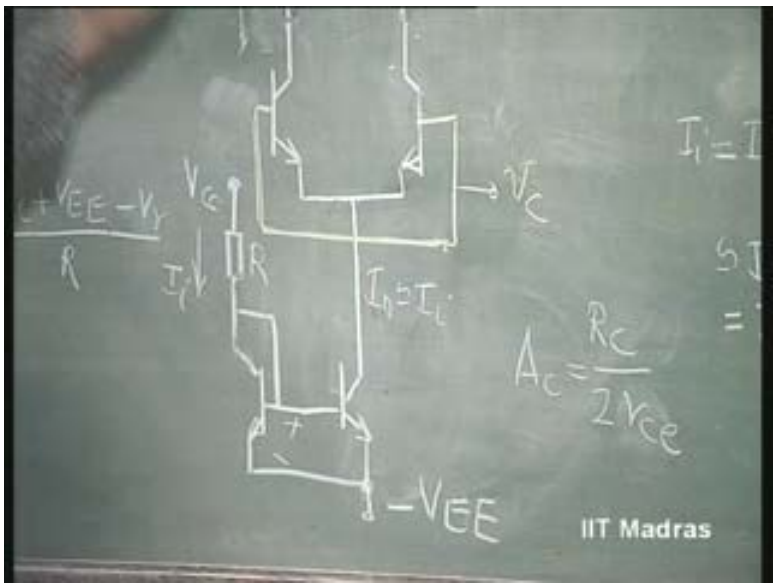

So, this is going to give you the fullest swing possible for the common mode voltage, without the transistors going to saturation. So, common mode swing problem is solved; high CMRR is obtained and low current can be used without using high valued resistor.

That I will discuss presently. Without necessarily using high valued resistors, we can bias this at very low value of current. So, these are the advantages of using these active loads.

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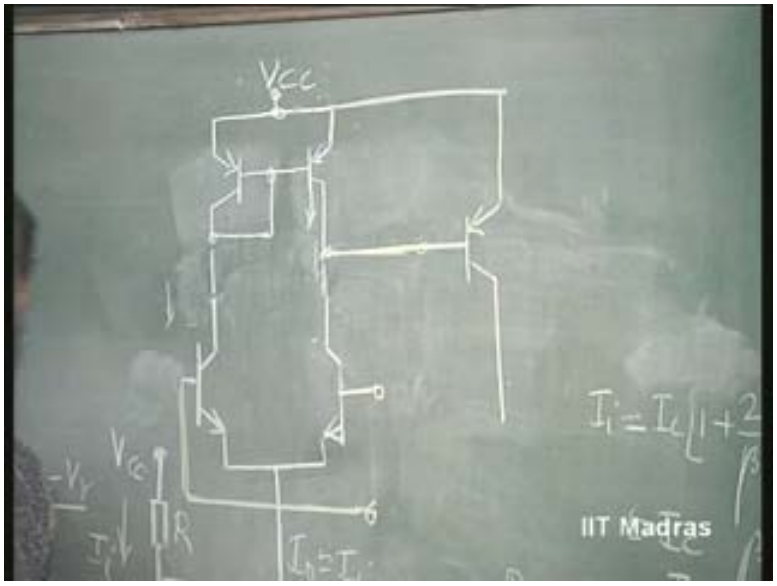

Now, you can really connect the next stage simply as, ... For example, this can be...if you have good p n p, you can therefore connect a common emitter configuration like this; direct couple. This potential is going to be restricted to V gamma. That is no problem because this is very neatly having its collector clamped at V gamma. This has its collector clamp clamped at V C C minus V gamma. This also is having at V C C minus V gamma. This is perfectly symmetric.

Now, the next stage is a common emitter. So, this current of yours which is V i by r e can be straight away pumped into this; and then as far as this stage is concerned, you can use an active load here which is a current sink. This is a current source; this is current sink. If this current is fixed as whatever it is, I i now, this current will be I i; and accordingly, so much base current will be drawn by this.

So, this kind of arrangement which we had used earlier, common emitter with current source load, this we used just earlier. Please remember. But, we had to use fairly

sophisticated arrangement to prevent loading at that. Such a thing is not needed when you are coupling to this differential amplifier another stage amplifier. This can give the highest gain possible. This can take care of other responsibilities like input impedance, etcetera, but it also gives you gain. So, these two combinations now will give you very high gain of the order of 10 to power 5 to 10 to power 6. That means about 100 to 120 decibels as the gain. So, this has been chosen as the basic configuration.

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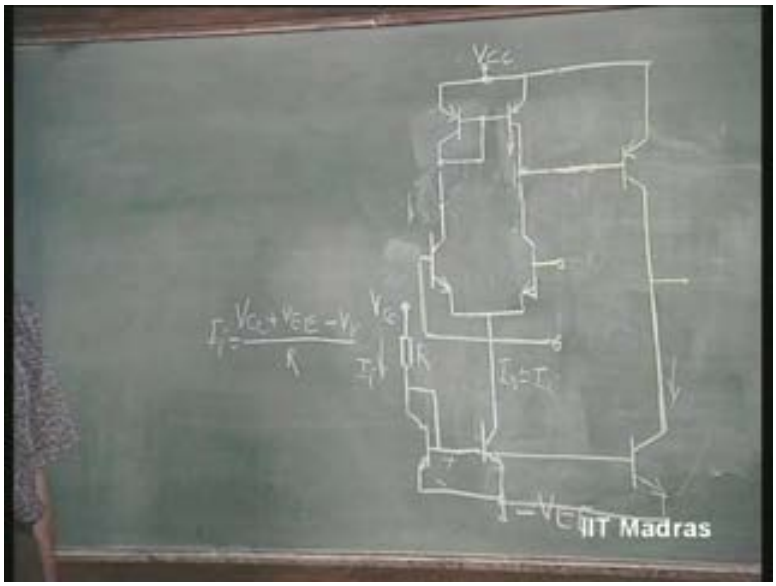

There is something else. The output stage also has to be connected. That, we will discuss later. After we discuss feedback, etcetera, we will discuss about what is the output stage; but for the time being, you can say that as far as op amp is concerned, the highest possible forward transfer ratio for the gain has been obtained by simply coupling an input stage with an intermediate stage. It is an intermediate because an output stage has to be connected. These three stages: input stage, out...intermediate stage and output stage form the configuration of all, what are called as third generation op amps.

We will see why it has been forced on a three stages. Why it can't be less than three, etcetera later, but for the time being it is necessary that I should cascade as many stages as possible in order to boost up the forward transfer ratio to a very high value. I now stop

at two such stages to give the gain, required gain; and this is a basic op amp configuration. There might be lot of variations in this but this is the architecture for a basic voltage, operational voltage amplifier. The input impedance being fixed by this input stage, intermediate stage, gives you sufficiently high gain.

Now, like input stage, we also want an output stage because both input and output deal with external world; and then we do not know what kind of external world is faced by these op amps. So, they have other responsibilities. We have to have output stage with protection provided, so that outside world does not damage anything.

We have output stage required for delivering the required amount of power with low output resistance if it is a voltage source. So, these are the responsibilities of the output stage. So, just as we had input stage taking the responsibility of common mode rejection ratio, input impedance and common mode swing, output stage will have the responsibility of protection, low output impedance and high output swing. So, that kind of stage, we will discuss later.

But now, as far as the swing is concerned the swing is pretty high; almost up to V C C and V E E possible, minus V E E possible. No problem. As far as output impedance is concerned, it is pretty high because it is going to be R C E of this shunted by R C E of this. So, output impedance is pretty high in this case.

So, that is the only disadvantage of these two stage structures. The gain is very high; so, and it does not use any resistor except for what? – biasing; one resistor. And, if you want, you can put it externally, so that what is inside contains only this. So, this whole thing can be put in an I C except for this resistor; and such is the configuration when we have MOSFETs and other things coming into picture; because in a bipolar technology, resistance is already available. But in MOSFET technology, we do not like to use any resistor and if resistance is needed to convert voltage to current, it is put externally.

Now, you can consider Example 17 where I have given you the structure of a MOS, CMOS op amp, operational amplifier. This configuration has this architecture similar to that of the bipolar op amp that we have discussed.

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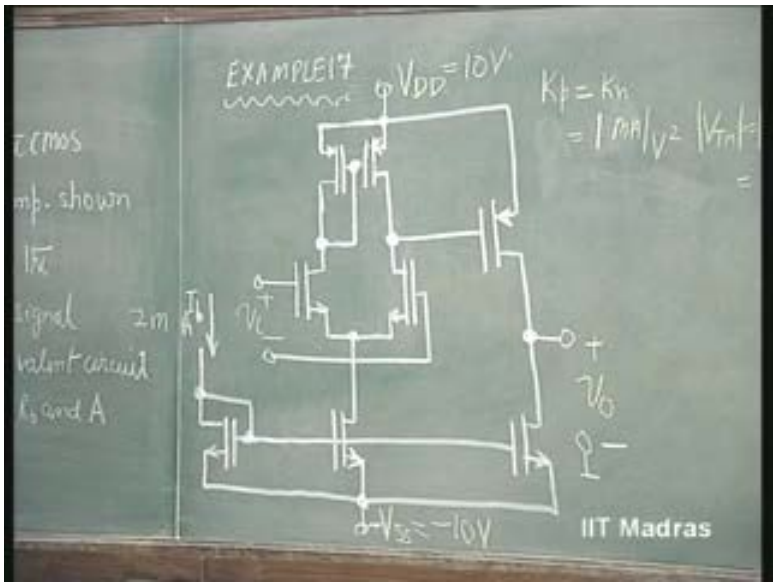

It is also a differential amplifier. You can see the differential amplifier here with the active load; differential amplifier with the active load and the current mirror for biasing; which is then cascaded to a common source amplifier with current source load which has been derived from the same current mirror. So, architecture wise, it is same as what we had discussed earlier. So, for this, we are now required to find out the equivalent circuit.

For the CMOS op amp shown, obtain the small signal equivalent circuit; that is R i, R naught and A.

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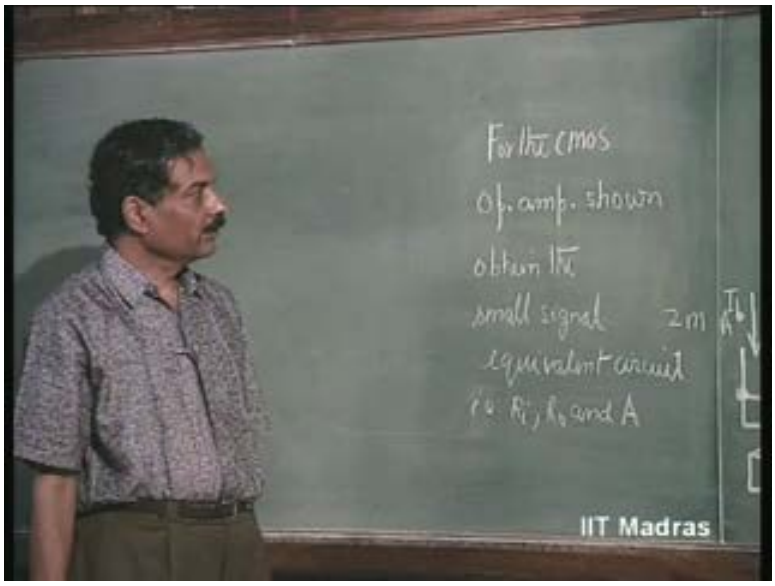

So, that is the example. You can perhaps take down the circuit completely. Now, K p has been made equal to K n in this case. I mean, by suitably selecting w by l ratio of this, you can select whatever K p and K n you want for the design. V T N is assumed to be same as V T P in magnitude. V T N is positive and V T P is negative. V T N is plus 1 volt; V T P is minus 1 volt. Now, this has been arranged to be biased at 2 milliamperes here.

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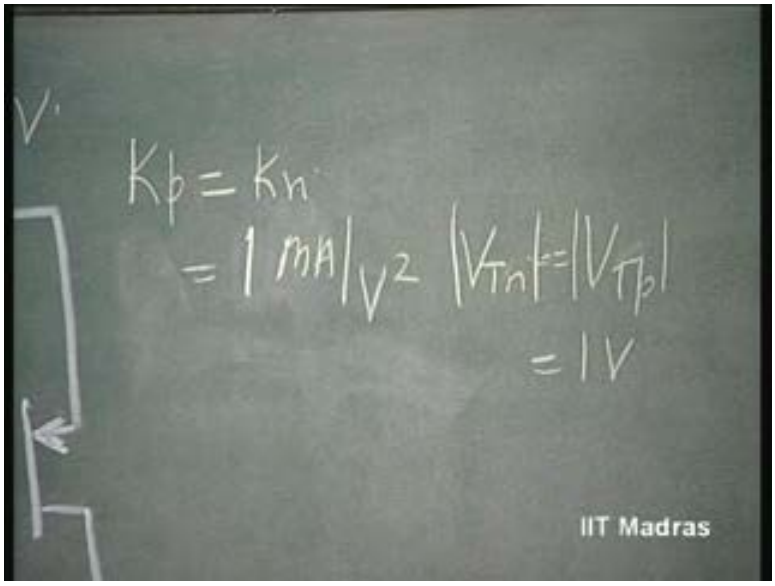

So, the current mirror will be such that this is 2 milliamperes. That is simple. So, this is the answer here. As far as current mirror action is concerned, this is 2 milliamperes, the current source biased; corresponding to which we can find out what this V G S is going to be. How do you find out that? That is obtained from the equation saying that K, K p or K n are the same. So actually, you have to use K n for this. So, 1 K into V G S Q minus 1 whole square is equal to 2 milliamperes.

K is given as 1 milliampere per volt square. V G S Q minus 1 whole square. So, V G S Q minus 1, therefore, is equal to root of 2, which is 1 point 414, which is root of 2.

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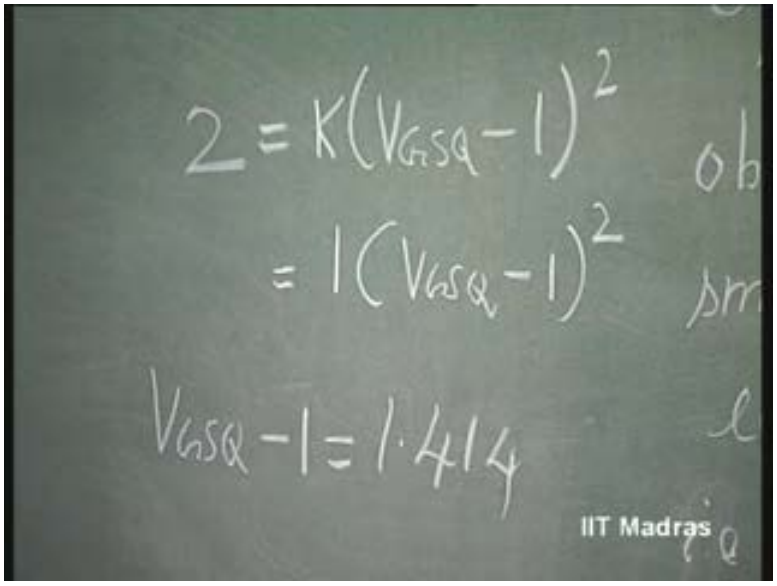

So, this is going to be nothing but root this and root this. So, V G S Q therefore is equal to 2 point 414. So, you can see here, if it is a bipolar current mirror it would have remained very nearly at point 6. Here, it has gone as high as 2 point 414.

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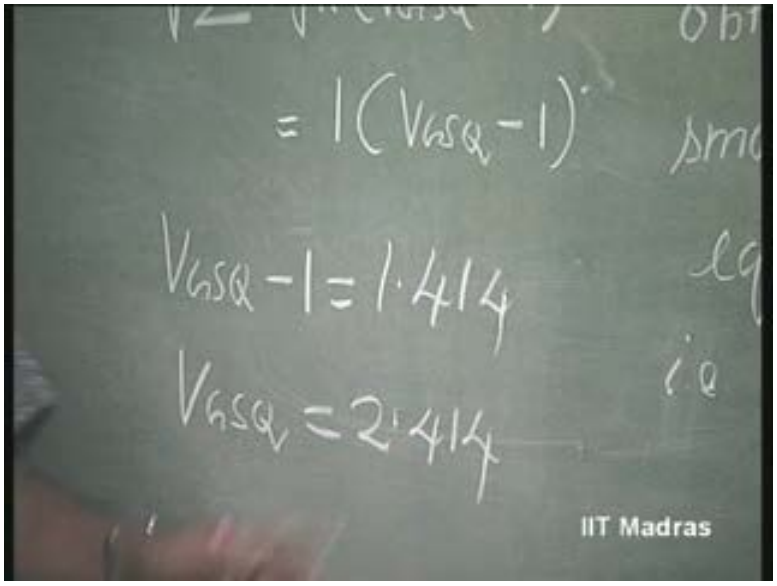

So, this is the thing; and r d s of this, of course it is dependent upon the voltage, etcetera. But now, I am going to give you... r d s of all these things we will take as equal to, let us

say, 100 K, just to make things simple. r d s of n channel as well as p channel, whatever be the bias, these are all bias dependent, please remember. But I am going to assume for these, that r d s of all the transistors will be equal to 100 K.

So, there is this 100 K resistance coming here. If you want to evaluate the common mode rejection ratio, this 100 K resistance is important. Now, g m of the stage has to be evaluated. You know that the operating current here is 1 milliampere each and therefore we can find out g m. g m is 2 K into V G S Q minus 1; but V G S Q to be used is the V G S Q of this. V G S Q of this is going to be...if you work it out, 2 volts for 1 milliampere.

You can put here...you see, 2 volts. 2 minus 1, 1; 1into 1. So, current is going to be 1 milliampere. So, this is going to be 2 volts. So, this is going to be...g m is 2 into K which is 1 into 1. So, g m is 2 millisiemens. So, the gain of this is g m into r d s of this; and r d s of this and input impedance of this.

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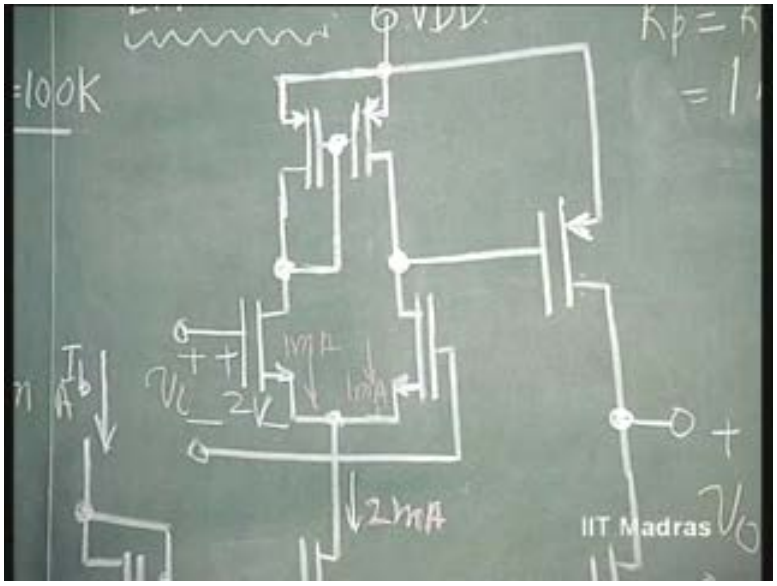

Input impedance of this is infinity. So, r d s of this and r d s of this; parallel. 100 K parallel 100 K is 50 K. So, r d s of this as well as r d s of this, if they are unequal, you

have to take the parallel combination of these unequal output impedances. So, this is going to be 50 K. So, gain of the first stage is 2 into 50 – 100; 100 K parallel 100 K.

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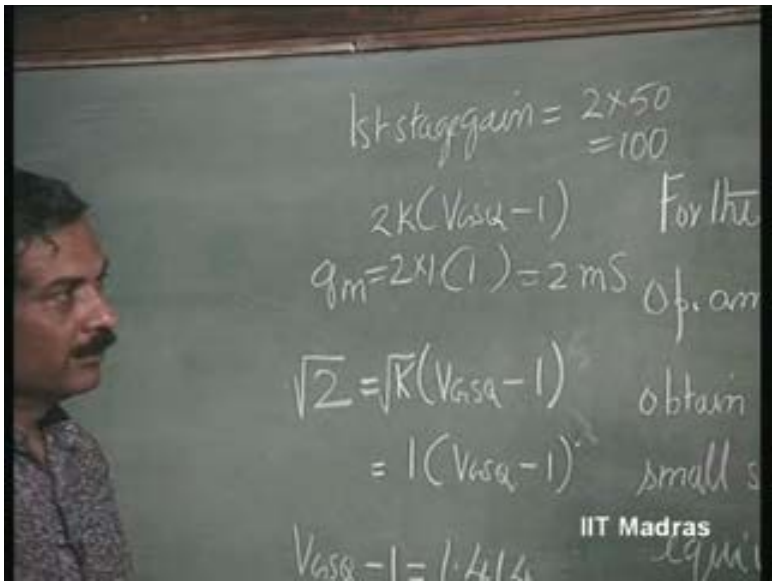

Next, this is applied to this and g m of this, this operating current is... Again, this is a current mirror. So, 2 milliamperes. Operating current of all this, 2 milliamperes. So, g m of this is going to be again 2 K into V G S Q minus 1. V G S Q minus 1 is 1 point 414. So, K is 1; this into 2 into 1 point 414 which is 2 point 828 millisiemens.

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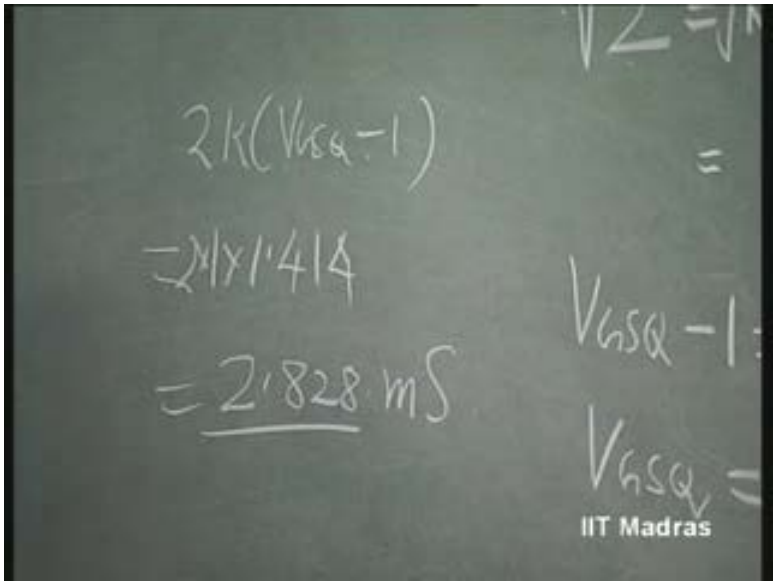

Again, r d s of this comes in parallel with r d s of this. So, the effective r d s is going to be 50 Kilo ohms. So, the gain of the second stage is equal to 2 point 828 into 50, whatever it is. How much is this? This is going to be 2 by 100. So, 141 point 4. So, overall gain is this into that. So, A is equal to 141400. No... 14140.

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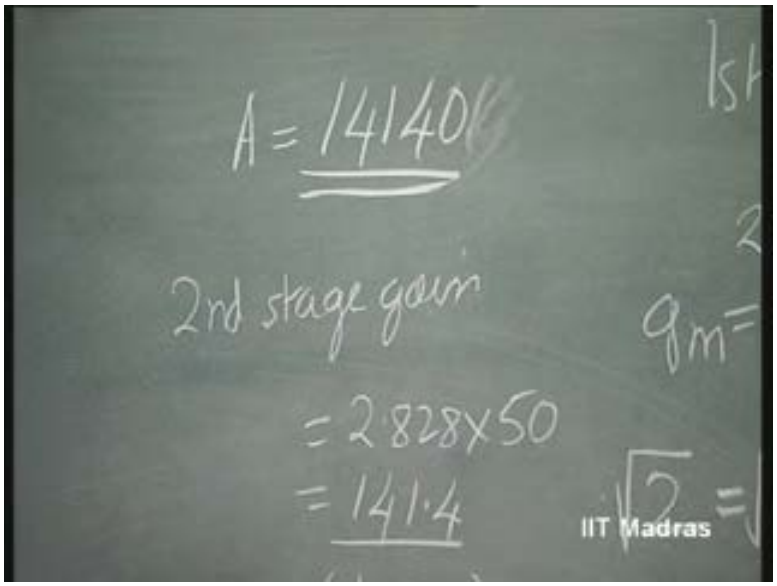

So, that is the gain of the entire thing. R i is infinity because it is MOSFET. R naught is... How much is it?- 5o K, which we have already assumed. So, that is all. Problem is so easily solved.

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