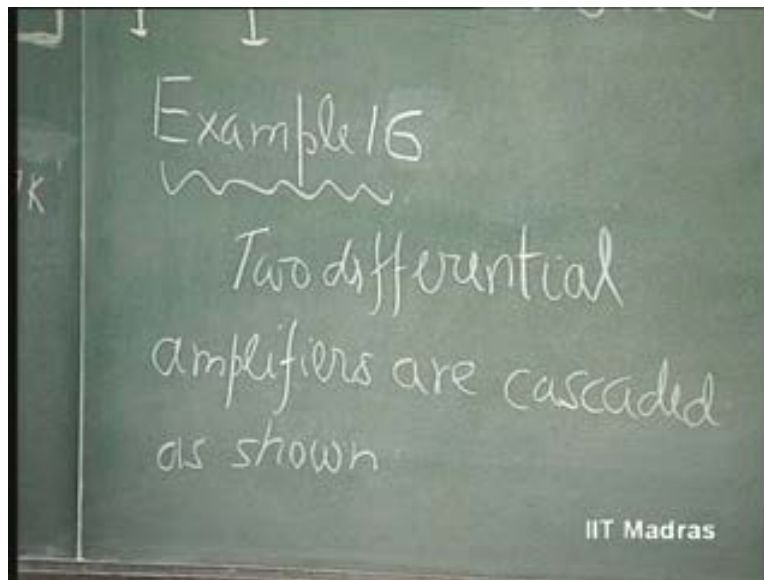


**Electronics for Analog Signal Processing - I**  
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**Department of Electrical Engineering**  
**Indian Institute of Technology – Madras**

**Lecture - 35**  
**Cascading Differential Amplifiers**

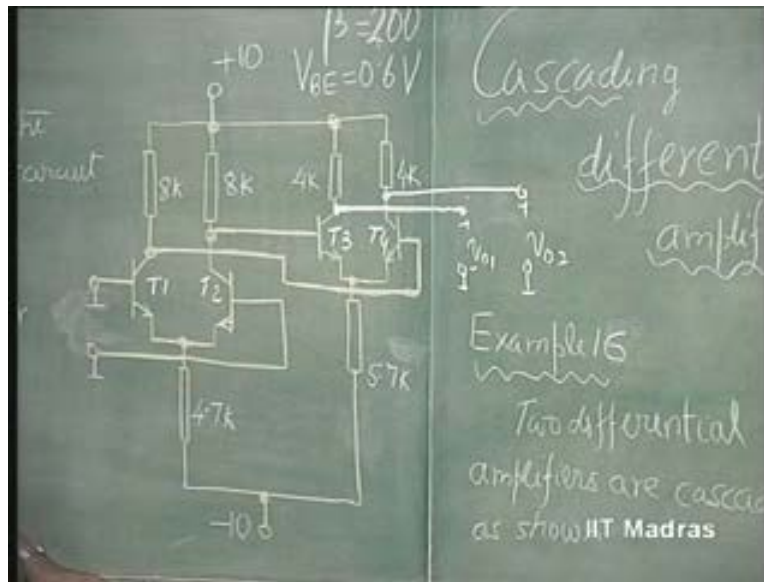
Today, we will discuss cascading differential amplifiers. We have done this earlier for the other types of amplifiers also and seen how cascading is going to improve the forward transfer parameter. Now consider this example. Two differential amplifiers are cascaded as shown. We will therefore understand the basic idea about cascading through these, this example.

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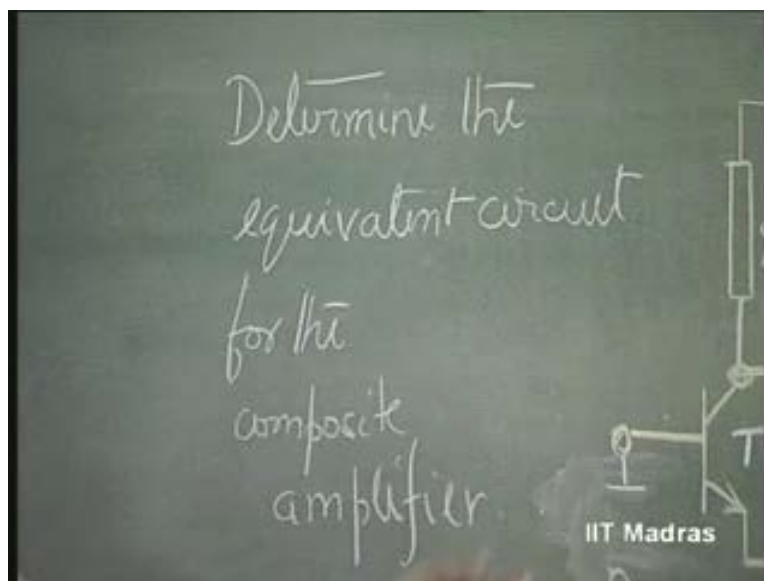
So, a differential amplifier made up of the pair T 1, T 2 is cascaded to another differential amplifier made up of pair T 3 and T 4. Cascading means, output of this is, in this case, directly coupled to another differential amplifier input. So, this is what happens if you want to get rid of the coupling capacitor and thereby fabricate these amplifiers in a monolithic integrated circuit.

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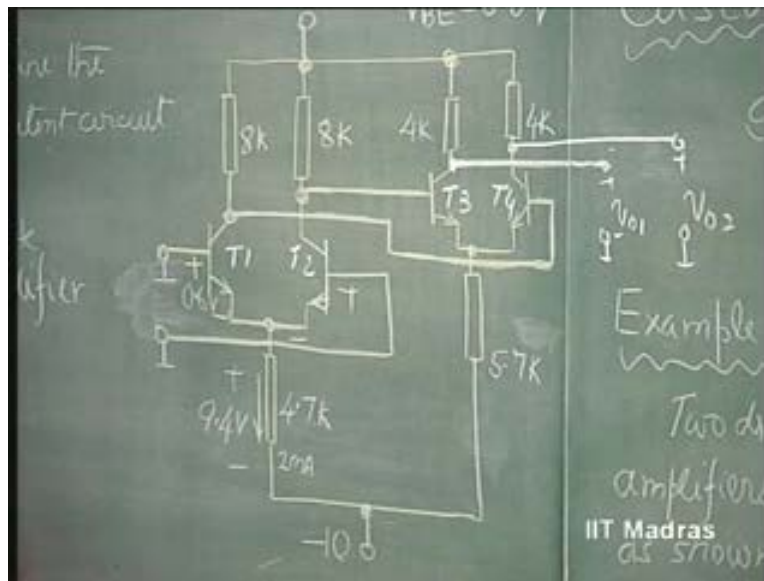
It does not need bypass capacitors. It does not need coupling capacitors. So, this is ideally suited for present day integrated circuit fabrication of amplifiers. So, let us see what the limitations are and what the parameters associated with this differential amplifier are. Determine the equivalent circuit for the composite amplifier.

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So, I want for the composite amplifier, an equivalent circuit. So, let us see... First, the input; these two are connected to ground. If that is the case, the voltage here is assumed to be point 6 volts. So, this emitter is at minus point 6 volts. This is at minus 10. So, the voltage across 4 point 7 K is 9 point... How much is it? - 4 volts. So, the current in this is 2 milliamperes. This is fixed at 2 milliamperes.

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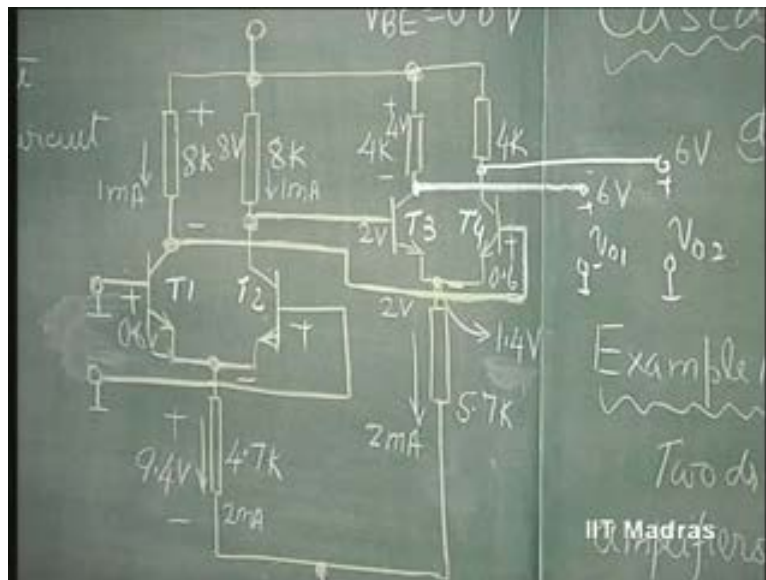
So, now you know how to fix the operating current of, for example, an input stage. When this is grounded, this voltage is going to be minus point 6; this is going to be minus supply voltage; and the rest of it is dropped across the resistance. So, you can fix the current, as in this case, 2 milliamperes; which means, the current in these two will be 1 milliampere each, neglecting the base current.

So, the current in each case will be 1 milliampere. This is...this collector current is same as this collector current. That is the assumption. Base currents become negligible, we say. Then the drop across this is going to be 8 K into 1 milliampere which is 8 volts. So, 10 volts minus 8 volts; so this voltage is at 2 volts; 10 minus 8 – 2 volts.

So, this is at 2 volts. Again, we have a drop of point 6 here. So, the voltage here is 1 point 4 volts. So once again, 1 point 4 volts; this is minus 10. So, the total voltage is 11 point 4 volts and I am fixing the resistance as 5 point 7 which is going to give us, again, current through this as 2 milliamperes. So, I have purposely fixed these currents uniformly as 2 milliamperes.

So, you can see here, the drop across this will be now...this being 1 milliampere each once again, the voltage will be 4 volts. So, if this is 4 volts drop, 10 minus 4, these voltages will be at 6 volts, quiescent. So, you can consider that if it is single ended output, the quiescent voltage of this amplifier is 6 volts; or you can consider the offset as really 6 volts. It is not really offset because we have purposely fixed it at 6 volts.

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We could have made it equal to zero volts, if we wanted. So, the difference output is going to be zero volts. So, if you take the differential output for a differential input equal to zero volts, then the output voltage is going to be zero volts. So basically, for a single ended output, you have the offset voltage as 6 volts or quiescent voltage as 6 volts and for differential output it is zero volts.

Now, what about the gain, etcetera? So first, let us consider from the input side, the input impedance. The currents being 1 milliampere each, the res will be approximately 25 ohms each. So  $r_{e1}$  equal to  $r_{e2}$  equals 25 by 1 milliampere. So, 25 ohms. Instead of 26, I am writing 25 for ease of mathematical computations.

So, 25 ohms into 25 plus 25; that is 50 ohms; 2 r e you get, into 200. So, the input impedance of this - this is differential input impedance we are talking of now. So, if I do not mention anything, it is always assumed that it is differential input impedance. So, this is equal to 2 r e into Beta plus 1. This is 50 into 201. So, this is about 10 K.

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Handwritten mathematical derivation on a chalkboard:

$$r_{e1} = r_{e2} = \frac{25\text{mV}}{1\text{mA}} = 25\Omega$$

$$P_i = 2r_e(\beta + 1)$$

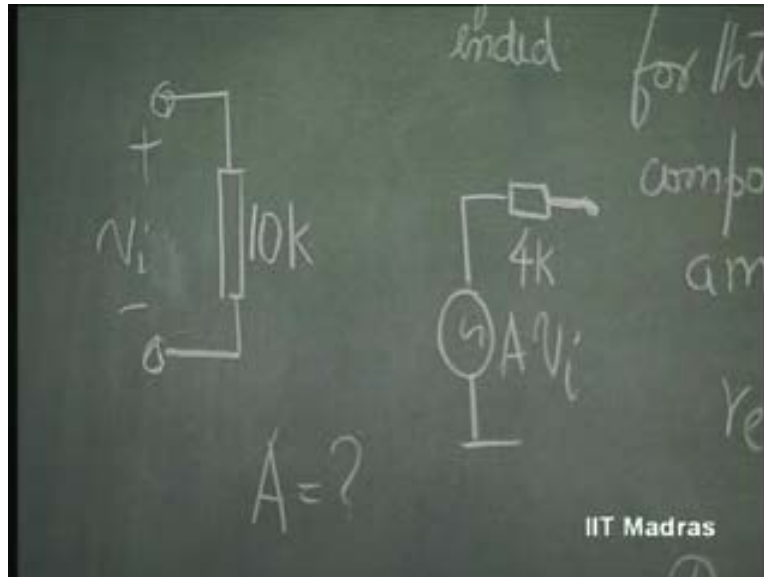
$$= 50 \times 201$$

$$= 10\text{K}$$

The chalkboard also shows a small circuit diagram with a current source 'I' and a voltage of 9.4V.

So, you have seen here that the input impedance is fixed at 10 K. So we can say the differential input impedance of this is 10 K. This is the input. We can forget about the rest. Now, as far as the output is concerned, output is going to be from this point to ground or across this.

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If it is from this point to ground, output impedance is going to be 4 K. If it is between these two points, output impedance is going to be 8 K. So, let us consider the single ended output. For that, output impedance is going to be 4 K. This is a single ended output. So, if I apply a differential signal, therefore again, this suffix d is going to be dropped in future; because for differential amplifier, we are most interested only in differential gains.

So, this  $v_i$  is going to be appearing as  $A$  times  $v_i$ . We have to find out what  $A$  is, differential mode gain, the composite differential mode gain. Input is differential; output is single ended. That is what is considered now. So, this is the only parameter that has to be found out. All the other parameters associated with the equivalent circuit are known. So, let us see.

As far as this amplifier is concerned, this is a differential amplifier and its differential gain comes into picture at this point. So, what is the impedance at this point? 8 K plus 8 K; or 8 K is going to be shunted by what? I told you that any differential amplifier can be split into single common emitter amplifiers by connecting this to ground. So, that means

this 8 K is going to be shunted by its input impedance here. Input impedance here is 25 into 201 which is approximately equal to 5 K.

So, 5 K plus 5 K will be shunting 8 K plus 8 K. Is this clear? Or, 10 K is going to shunt 16 K here. This is the differential impedance. Or, 8 K is going to shunt 5 K; 10 K is going to shunt 16 K; or, 8 K is going to shunt 5 K. So, 8 K shunted by 5 K. This is the impedance which can be replaced using the effective impedance at this point; 8 K shunted by 5 K. How much is it? 2 point, 3 point zero 77. So, we will put it as 3 point zero 8.

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The image shows a chalkboard with handwritten calculations. On the left, there is a calculation for the parallel combination of two resistors:  $\frac{8 \times 5}{13} \text{ k}$ , which is simplified to  $= 3.08 \text{ k}$ . The word "Single ended" is written below the calculation. On the right side of the board, the words "Determining equivalent" are written in a cursive script. At the bottom right, the logo for "IIT Madras" is visible.

So, that is the effective resistance at the collector.  $g_m$  is already 1 over  $r_e$ , which is 40 millisiemens for this transistor. 40. 40  $g_m$  into effective R C; 40 into 3 point zero 8 K. So, the first stage gain, first stage gain is going to be  $g_m$  into R C effective, which is 40 millisiemens into 3 point zero 8 – 123. This is the first stage gain. Is this clear?

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$A = ?$   
 $1^{\text{st}} \text{ stage gain} = g_m \times R_{\text{eff}} = 40 \times 3.08 = 123$   
IIT Madras

Now, second stage gain is  $g_m R_C$  by 2 because we are taking single ended output. So,  $g_m$  is the same because operating currents remain the same for all the transistors. So,  $g_m$  is the same 40 millisiemens. So, second stage gain is equal to  $g_m R_C$  divided by 2. So,  $g_m$  is 40 millisiemens and  $R_C$  is 4 K. So, this is 80. So, overall gain therefore,  $A$  is equal to simply 80 into 123.

So,  $A$  is really speaking equal to 120 into 83 which is, pardon, 123 into 80. So, how much is it? 9840; 123 into 80; so, 9840. So, this is nothing but...now, which is the output we are considering? This is important. Let us consider this here. If input is marked, this as positive and this as negative, let us say  $v_i$ . So I am saying this is positive and this is negative; what is connected to T 1 as positive and what is connected to T 2 as negative. Then, there is phase shift of 180 degree from here to here. There is no shift, phase shift, from here to here. So, zero phase shift from here to here. From here to here, there is a phase shift of 180 degrees; and therefore, if I take this as the output, strictly speaking, I get inverted; minus  $A$  I will get.

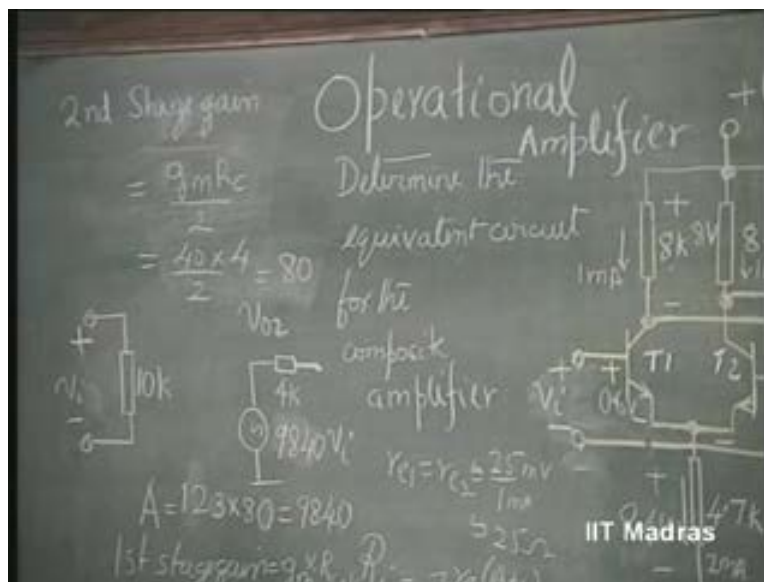
If I take this as the output, the phase shift of this and this will be zero. So, whatever I have assumed as plus minus become valid. So, if this is plus minus, this is plus, this is



plus. So, I take  $V_{out}$  as the output. Then the marked... What is marked here? What does it mean? This is what is called as the non-inverting terminal. This is called inverting terminal. What does it mean? From here to here there is no phase shift; from here to here there is a phase shift of 180 degrees. So, this is how you can mark the terminal of this so called cascaded amplifier.

Now I can forget about this entire circuit and use only this. Such a cascaded structure with very high forward transfer gain is called an operational amplifier. Such a cascaded structure with very high forward transfer parameter is called by a special name for this amplifier, called operational amplifier.

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Basically it is a source, control source. Basically it is a control source with high forward transfer parameter; in this case, voltage gain. It could be current gain; it could be transfer resistance; it could be transfer impedance. Therefore, we have four types of operational amplifiers possible depending upon whether the forward transfer parameter of interest is voltage gain, current gain, transfer conductance or transfer resistance. Respectively, these things will be called as operational voltage amplifier, operational current amplifier, operational transconductance amplifier or operational transresistance amplifier, just as we

had in the beginning of this course defined basic control sources as voltage amplifier, current amplifier, transresistance amplifier and transconductance amplifier. So, the main fact in designing such operational amplifiers is making sure that the amplifiers are cascaded and the transfer parameter is as high as possible; and then most of the analysis could be as well carried out by using this equivalent circuit instead of this complex circuit.

Now, as far as this is concerned, let us once again see. The gain being of the order of 10,000 or so for volts of swing. What will be the swing available here? Can you think of... See, this is at 6 volts. This is at 2 volts. So, the reverse bias voltage is 4 volts. On one direction, we have a swing of 4 volts available before the transistors go to saturation. This is 6 volts; this is 4, 2 volts. So, reverse bias voltage is 4 volts. It can become equal to zero.

On the other hand, these operational amplifiers or the transistors are operating at a current of 2 milliamperes. So, the swing, strictly possible, for this differential amplifier is...for how much is it? This  $I_{naught}$ , this  $I_{naught}$  can completely flow through this and therefore there may be a drop of 8 volts here. There can be a drop of 8 volts here when this is 10 volts so that this can go to 2 volts on one side and go to 10 volts on the other side. 2 to 10 volts. That means peak to peak swing of 8 volts is possible. That is easily found out by remembering our swing discussion in differential amplifier, which is simply  $I_{naught}$  into  $R = 4 \text{ ohm}$ , Kilo ohm into 2 milliampere. So, that is the peak to peak swing for the differential amplifier, 8 volts.

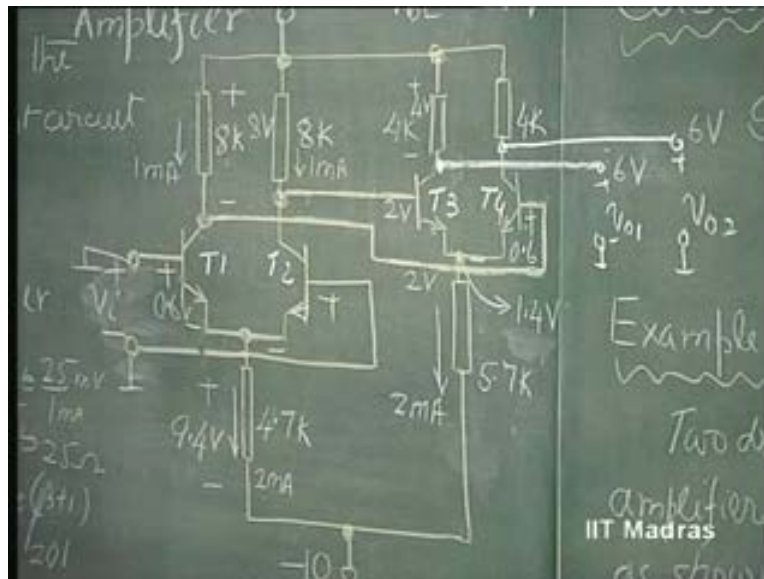
Now, is it possible to have 8 volts output swing? On one side it is possible because it can go up to off state; on the other side, when it goes to complete switching of 2 milliamperes to this, this transistor should not go to saturation. That is the condition. When you have 2 milliamperes and you have 8 volts, this potential goes to 2 volts; just it is entering the saturation. This has been therefore optimally designed. So, this is going to give me a symmetrical swing of how much? - single ended output; you can get a swing of 8 volts peak to peak, or 16 volts peak to peak for the differential mode operation. Is this clear?

This is going to give you a peak to peak swing of 8 volts for single ended operation; or 16 volts for differential operation without any problem, symmetric swing. So, this amplifier design really tells us something about the problems associated with the design of op amp. Let us now consider that this is at zero volts. Let us say, common mode voltage is zero volts,  $v_i$  is zero.

Then, this is at 2 volts. That means this can give you a swing of 2 volts. But that much swing is not needed because the gain of this entire structure is going to be of the order of 80 or so. So, even if you consider 8 volts swing, 8 volts divided by 80; that is the voltage swing that is required, at this point. You are providing considerable amount of reverse bias unnecessarily.

Again, this 2 milliamperes into 8 K is not at all needed here. So, the current has been excessively chosen here. The current could be made very small for the input stage. If I make the current very small, the input impedance will increase. If, instead of 2 milliamperes, I make it point 2 milliamperes, the input impedance, instead of being 10 K will become 100 K. Is this clear?

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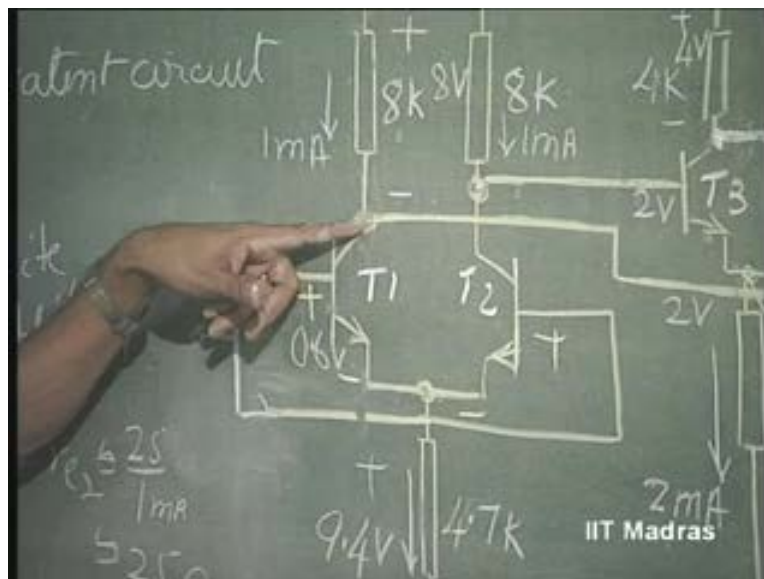


And, this will just work. Of course, gain is going to be reduced; this stage gain is going to be reduced. That is the price you are paying for, for making the input impedance high. So, whenever I try to boost up the input impedance by making the current low here, the gain also falls. But the first stage of any amplifier has major responsibility of not gain, but input impedance and common mode rejection ratio.

So, we do not bother about the gain reduction here. We purposely make the operating current very small and this voltage very small. So, this is the situation of design in what is called operational amplifiers. Now suppose, because of a common mode voltage here, let us consider the common mode voltage. How much common mode can it have here?

No differential voltage is there, but common mode voltage is coming into picture. So, this  $V_i$  common mode can go up to how much voltage? - in this case, up to 10 minus 8; that is 2 volts. There is no question of this current totally getting switched here. That will never happen because that much voltage, swing is never required in the input stage.

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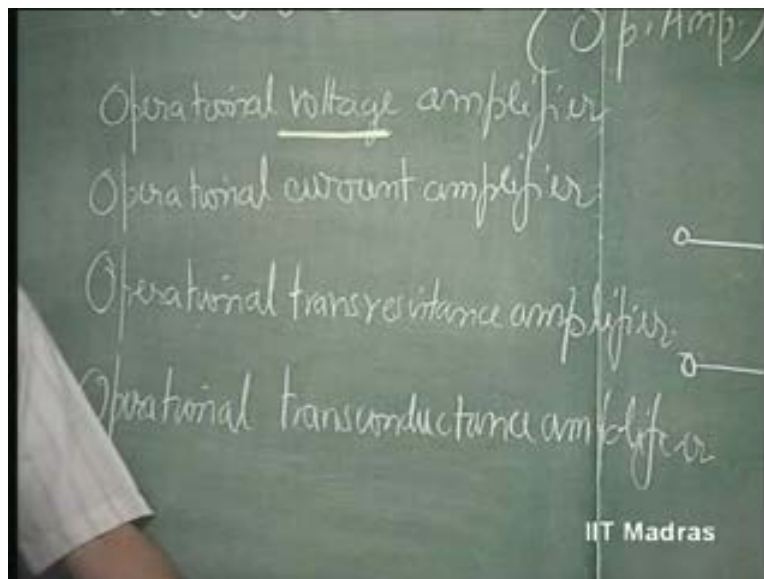


So, this common mode voltage can only go up to 2 volts on this side, where as it can go up to minus 10 volts on the other side. So, there is a problem with this. Suppose common

mode voltage goes higher. Both these op amp transistors will go to saturation. And if both of these go to saturation, there will be a serious problem, which we will discuss later. So, that is called latching.

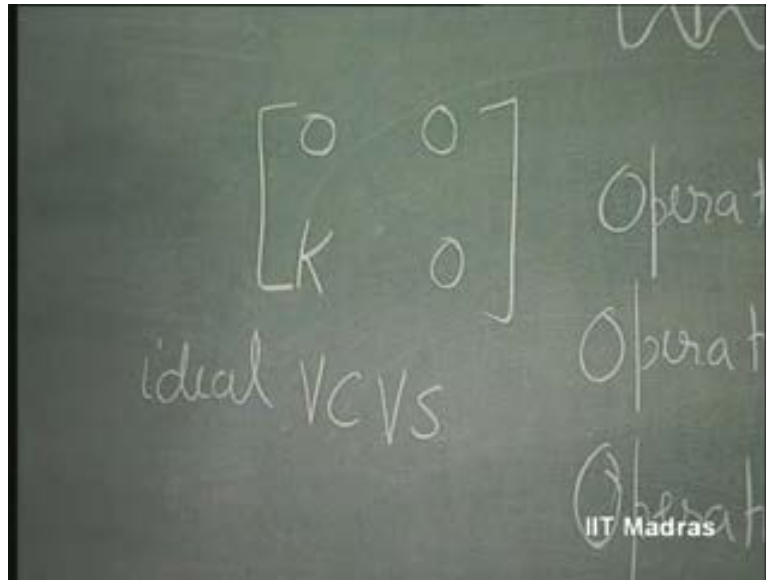
We just started the discussion on a special type of amplifier called operational amplifier, popularly called op amp. This has become a very useful building block these days of electronics and we should know the basis of design of such stages. There are therefore four types possible, obviously. Operational voltage amplifier, operational current amplifier, operational transresistance amplifier, operational transconductance amplifier.

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Historically, this is the one which has come into existence as a popular amplifier. So, we will confine our discussion for the next few classes on the operational voltage amplifier. What it means is, it is nothing but an ideal voltage controlled voltage source. Ideal voltage controlled voltage - we have seen as this parameter. So, what is the parameter with which we can define ideal voltage controlled voltage source?

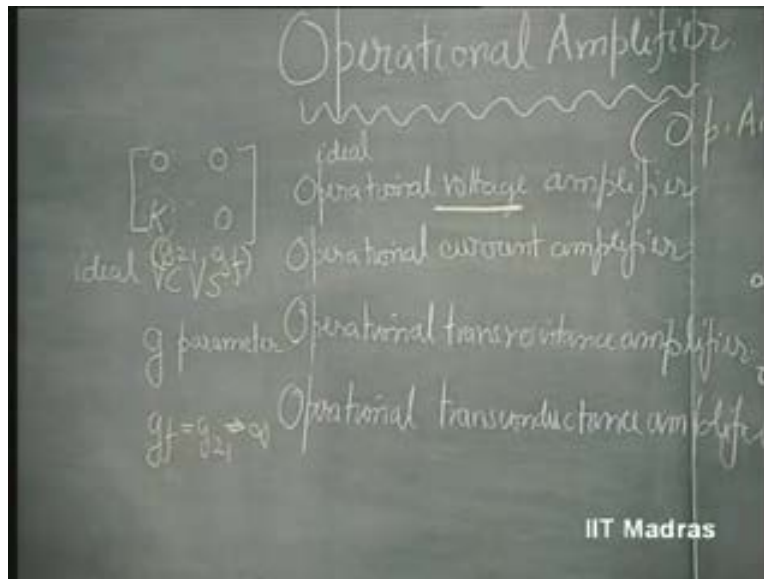
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V C V S - this parameter, if you remember, there is only one way of defining; an ideal voltage controlled voltage source can be only defined by using what is called  $g$  parameter. There is no other way you can define an ideal voltage controlled voltage source; and this  $g$  parameter which is called  $g_{21}$ ; or, this is also called  $g$  forward. This is nothing but open loop voltage gain it is called; voltage gain, voltage transfer ratio.

So, in the case of ideal voltage controlled voltage source, if  $g_f$  which is actually  $g_{21}$  tends to infinity, then it becomes an ideal operational voltage amplifier.

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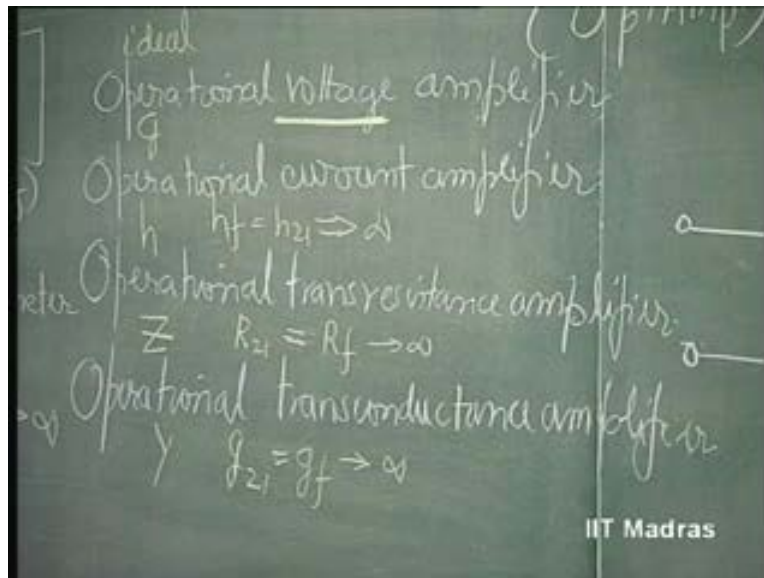


So, once again, if an ideal voltage controlled voltage source is taken in which all the three parameters - input impedance, output conductance, reverse transfer ratio - all these three things are zero; and only the forward transfer ratio which is the voltage gain, this is reverse transfer current ratio, this voltage gain, if it becomes infinity, then we reach what is called ideal operational voltage amplifier.

Same way, we can define ideal operational current amplifier. If we take, instead of g parameters, h parameter and make  $h_{f1}$  or  $h_{21}$ ,  $h_{f1}$  or  $h_{21}$  tend towards infinity, then it becomes an ideal current amplifier.

Now, operational transresistance amplifier by the name itself implies  $R_{21}$  or,  $R_f$  goes towards infinity. Here,  $g_{21}$  equal to  $g_f$  goes towards infinity. This is z parameter; this is y parameter; y parameter, z parameter, h parameter and g parameter. So, these are the basic definitions of operational amplifiers.

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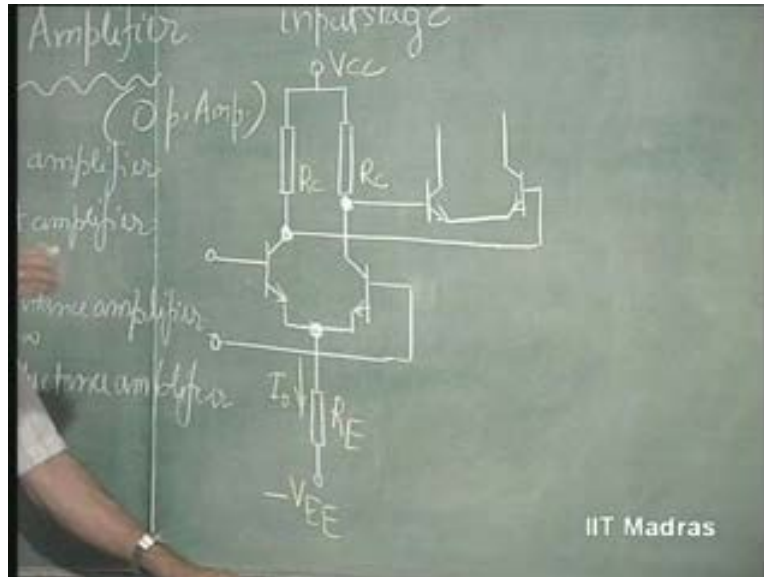
Let us concentrate on how we can design a good operational voltage amplifier. Obviously, the input impedance should be as high as possible; output impedance should be as low as possible. When you cascade any amplifier configuration, we have proven earlier that the forward transfer parameter of the individual amplifier, if it is high, the reverse transfer parameter is going to be low. And, when you cascade, this becomes higher; this becomes lower. This is the basic effect of cascading. So, as we cascade, this will keep on increasing. This will keep on going towards zero. So, that is the basic nature of cascading. So, that is why cascading is a must in order to realize an operational amplifier. These two you have to design such that these two parameters are going towards zero.

In this case, input resistance is made very high. So, let us concentrate on input stage of an operational voltage amplifier. The input impedance has to be high. As I pointed out



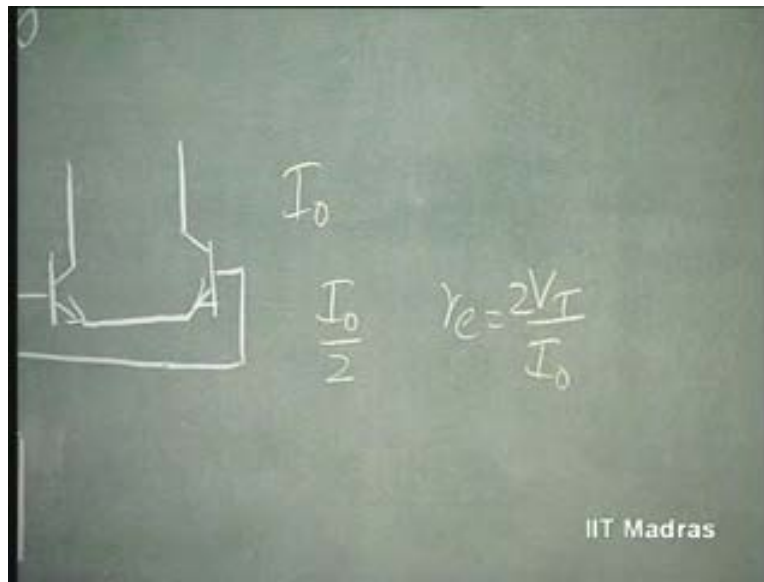
earlier, when solving the problem, we said the current is fixed by this resistance here and this has to be made as low as possible.

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So, what is the first thing is,  $I_0$  naught, which depend...determines the input impedance. How does it determine the input impedance? Because of  $I_0$  naught, the operating current is  $I_0$  naught by 2 for the transistors and the  $R_E$  of the transistors will be  $V_T$  divided by  $I_0$  naught by 2.

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So, the  $r_e$  of these transistors, these are inversely proportional to  $I_{\text{naught}}$ ; and therefore, input resistance which is twice  $r_e$  into  $\beta + 1$  is going to  $4 V_T$  by  $I_{\text{naught}}$  into  $\beta + 1$ . This is the input impedance of any op amp which uses a pair of transistors at the input stage.

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Handwritten equations on a chalkboard. At the top, there are some faint markings: a horizontal line, the number '2', and the symbol  $I_0$ . The main equations are:  
$$R_i = 2r_e(\beta + 1)$$
$$= 4 \frac{V_T}{I_0} (\beta + 1)$$
The second equation has a wavy underline under the fraction  $\frac{V_T}{I_0}$ . The IIT Madras logo is visible in the bottom right corner.

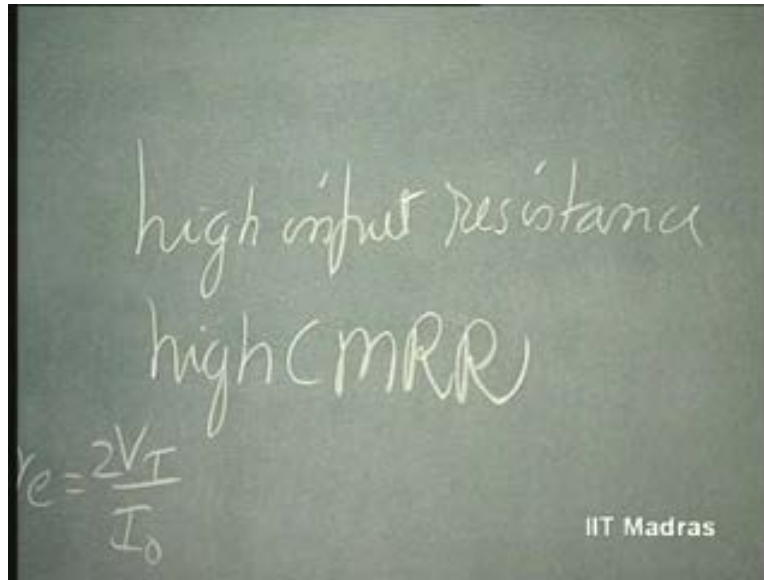
So, Beta is not in our hand. It...may be, the technology fixes the Beta at a fairly high value of the order of 200 or so.  $V_T$  is not in our hand. The only thing in that can be played upon is  $I_{naught}$ .

So remember, for an input stage...input stage is like a watchman of a building. It...let us say a building has people inside; the host trying to entertain the guest who are coming from outside. Watchman is the part of the whole show but he has limited function. He need not entertain the guest in the way guests are entertained after they come into building by the host. Same is the case. This differential amplifier need not amplify; but its main role is to offer high input impedance. This is...this can be treated as sort of resistance to great gate crashes in a function. Only the genuine guest should be allowed inside. That kind of selection is what is going to be done by this watchman kind of role adopted by the input stage. It is going to get rid of unwanted elements.

First, input impedance should be high. It should get rid of unwanted people. That means this unwanted people may be the common mode signals. This should have high common mode rejection ratio. It should allow only the differential signal to be amplified; and it should ignore the common mode signal. This is trash. It has no business entering this building. So, it will select the differential signal from the composite signal.

Now, that role is the major role. That means apart from high input impedance, high CMRR is the responsibility of the input stage. Please remember this. This is a major responsibility. The guest, the guests inside may be blissfully unaware of the responsibility of the watchman in trying to fight with unwanted elements getting into it. So, this is a major responsibility.

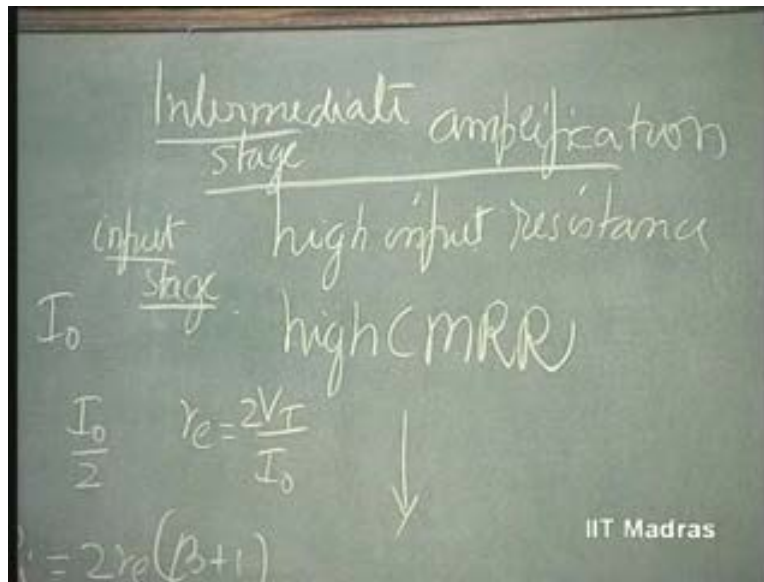
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So, what do these guests now do? They never bother about what is happening outside the building. They will concentrate on entertaining the guests. The host will concentrate on entertaining the guests. That is what is done by the next stage. So, in any op amp, the input stage has the major responsibility of taking care of input characteristics. Consequent to this, whatever gain is obtained is going to be taken as good, as far as this is concerned.

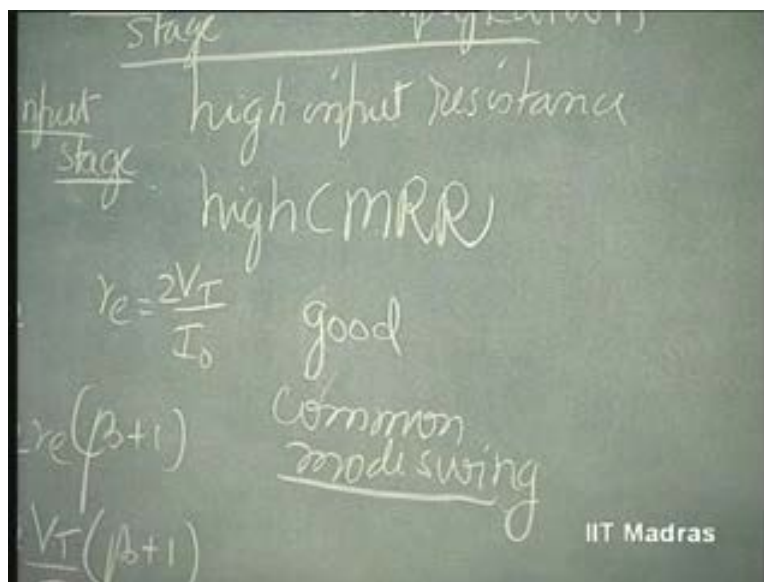
That means whatever this watchman can do in terms of entertaining their guests by talking some good words about their welcome, etcetera, so, that can be done by this person; but not further than that. Just a bit is going to be done inside, in the intermediate stage.

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So, major responsibility is amplification only; whereas, input stage - major responsibility is high input resistance, high CMRR and good common mode swing.

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This I have told you once again. The common mode voltage, we do not know what kind of input comes through. That, the common mode voltage may be there along with the

differential mode voltage. It may be zero; common mode voltage may be zero. It may be very nearly the supply voltage, positive. It may be very nearly negative supply voltage.

In all these things, it should be able to remove the differential mode signal and amplify it, without amplifying the common mode signal. That means the common mode signal should be capable of going from minus to plus without this stage getting any way affected; without...the watchman suddenly losing its role, because of the pressure offered. That should not happen; you should therefore design this.

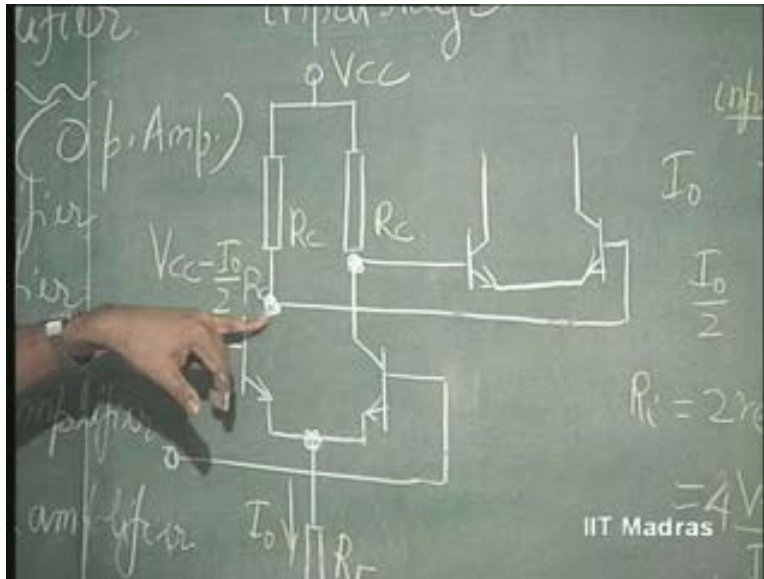
In this case, for example, this voltage is going to be  $V_{CC}$  minus  $I_{DQ}$  into  $R_C$ . Assuming that output swing is going to be very large and the gain is going to be very high, we will see that this swing, differential mode swing, here is extremely small. So, the voltage here remains unaltered at  $V_{CC}$  minus  $I_{DQ}$  into  $R_C$ . But, if you want this voltage to be very nearly  $V_{CC}$ , we should make  $R_C$  into  $I_{DQ}$  very small. But on the other hand, the gain of this stage is... The gain of this stage,  $g_m$  into  $R_C$  is nothing but  $I_{DQ}$  by  $2 V_T$  into  $R_C$ . So, gain of the stage is dependent upon  $I_{DQ}$  into  $R_C$  divided by  $2 V_T$ . So, we cannot make this too low because the gain decreases considerably.

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The image shows a chalkboard with handwritten mathematical expressions. At the top, there is a partially visible equation:  $= 4 \frac{V_T}{I_{DQ}} (\beta + 1)$ . Below it, the differential mode gain is written as  $g_m R_C = \frac{I_{DQ} R_C}{2 V_T}$ . The text "IIT Madras" is visible in the bottom right corner of the chalkboard image.

Now consider this. Input impedance can be maintained at whatever level you want. When input impedance is reduced for the sake of decreasing, increasing input impedance,  $R_C$  can be increased making  $I_{DC}$  high; but the moment  $I_{DC}$  is made high, the common mode voltage capability goes down. Now, how to tackle this?

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This was the major problem in the initial stages of op amp design. Then we solved this by a very intelligent technique. Why should we use resistors here? These resistors give you a DC drop as well as AC. They are going to be useful. I use a component which gives low DC drop but high equivalent resistance. So, I use what is called Active Load. What is it? That gives you equivalently high resistance, but using low DC drop; it is called active load.

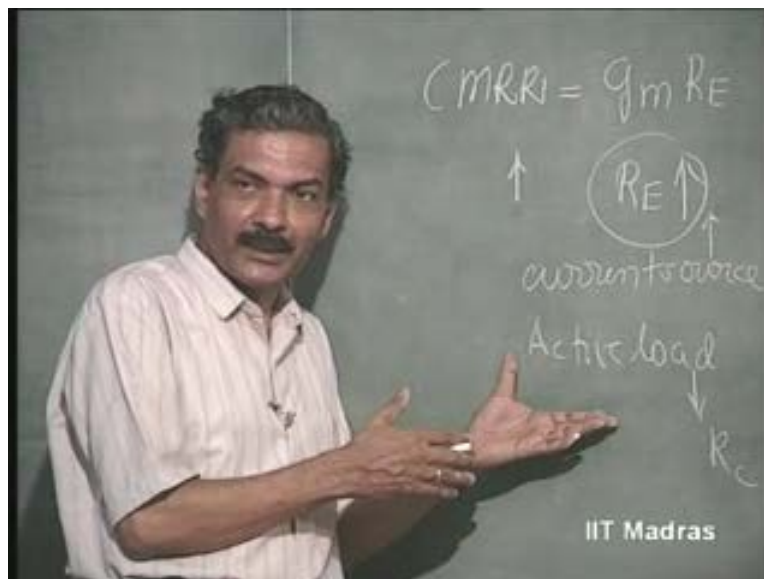
We will discuss the role of active load; as also, how to improve common mode rejection ratio and input resistance. Input resistance, as I told you, it can be merely improved by decreasing the operating current.

CMRR is equal to  $g_m R_E$ . So the CMRR of the input stage should be high. So, in order to increase the CMRR, we have to make  $R_E$  very high.

It is acceptable that  $R_E$ , when it is increased in order to decrease the operating current, CMRR improves. But, I would like to have an arrangement where  $R_E$  is of the order of mega ohms even when the current is of the order of milliamperes or even tens of milliamperes. That means I would like to use a current source which can simulate a large resistance here offering whatever current you want for biasing; so that, so that CMRR is isolated from other aspects of the amplifier design, which require a specific value of current.

So, by introducing what is called as a current source in place of  $R_E$  and by introducing what is known as active load in place of  $R_C$ , we can almost get rid of almost all the resistors required in our operational amplifier design. And the op amp will comprise of only transistors which take up minimum area compared to resistors plus transistors.

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Therefore, this kind of structure which performs better, takes up lower area, is highly suited; and not only that, it solves our problem regarding common mode swing, it solves

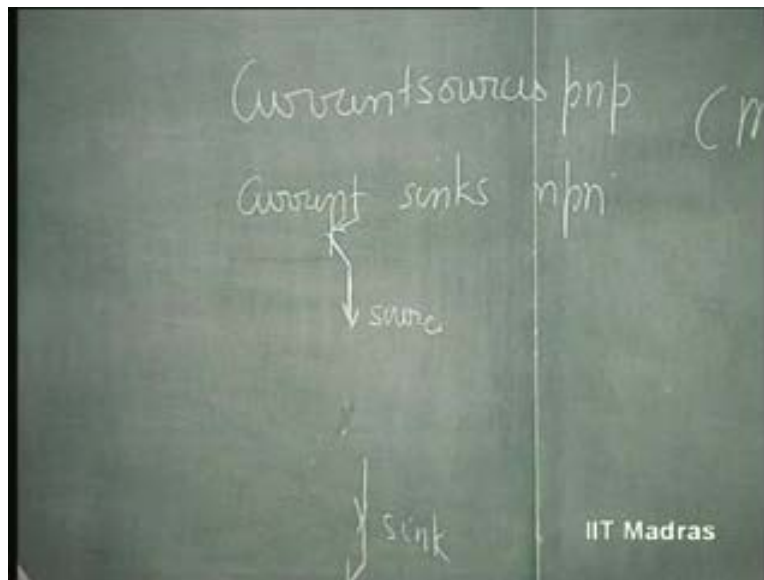


our problem regarding common mode rejection ratio, it solves our problem regarding low valued current being reached without basically using high valued resistors which take up lot of area.

So, we will discuss now how to obtain these current sources. Current sources... Now, when I say current sources, I also mean current sinks.

Now, unlike the network terminology where source means it can be either sink current or source current, here in integrated circuits, we say current source when it is delivering current and current sink when it is taking current. So, when it is delivering current it is a source; when it is taking current, this is a sink. This is a source. That means, automatically, sources can be realized only using P N P transistors and sinks can be realized only using N P N transistors. So, how to obtain sources and sinks?

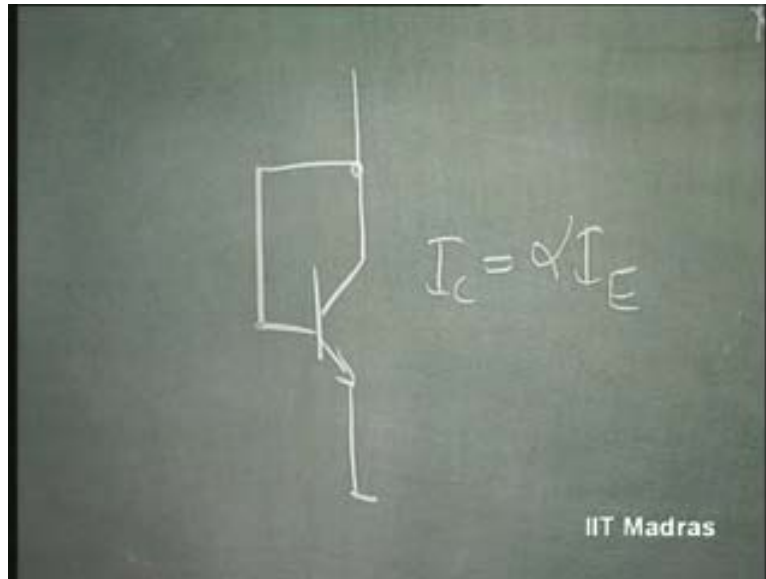
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Now, this part is very important. We all know that a transistor with collector base shorted still acts as a transistor. That means transistor action is there. What does it mean?  $I_C$  is equal to  $\alpha I_E$  is valid here. Transistor action is still there because  $V_{CB}$  is zero.

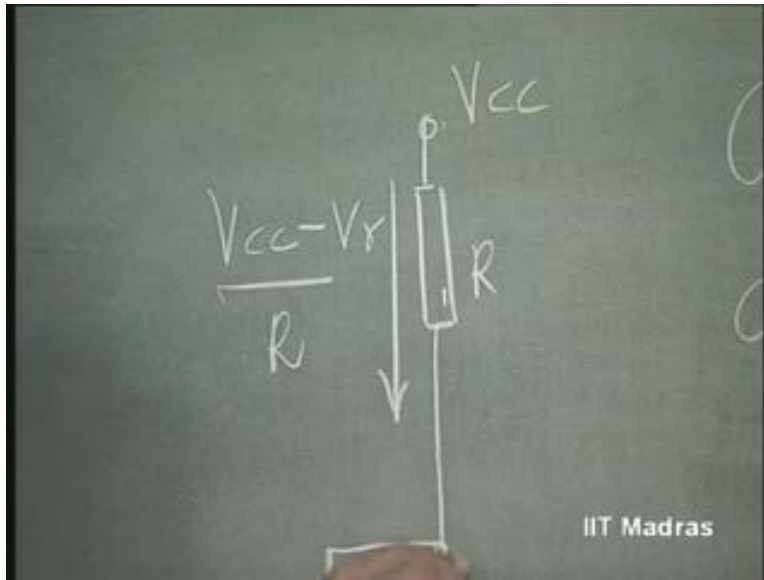
Up to this point we said the transistor is in the active region. So, this is a very nice structure, externally. This is looking like a two terminal element which is nothing but a diode. But internally, it is acting like a transistor. This is the most popular structure used in integrated circuit for biasing; a transistor connected as a diode.

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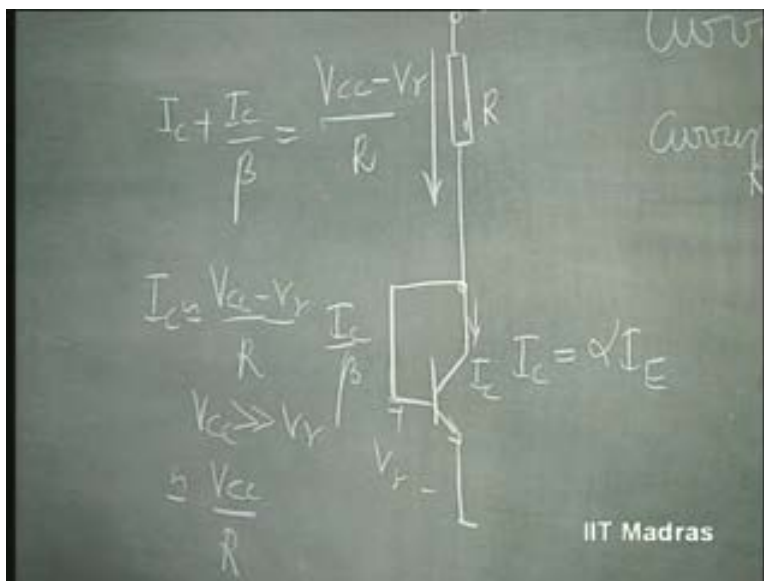
Let us see what happens when I pass a current through this. If I connect a resistance like this, the current in this is going to be  $V_{CC}$  minus  $V_{\gamma}$ ; this is  $V_{\gamma}$ , by  $R$ . The voltage here is  $V_{\gamma}$ . This is  $V_{CC}$ .  $V_{CC}$  minus  $V_{\gamma}$  by  $R$ .

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This current is  $I_C$ . This current is  $I_C$  by Beta. So, we get here  $I_C$  plus  $I_C$  by Beta equals this. If Beta is very high, then I can fix the current in this as  $V_{CC} - V_{\gamma}$  by R; almost nearly independent of the transistor. If I make  $V_{CC}$  very high,  $V_C$  much greater than  $V_{\gamma}$ , this is equal to  $V_{CC}$  by...this is equal to  $V_{CC}$  by R; almost independent of the transistor.

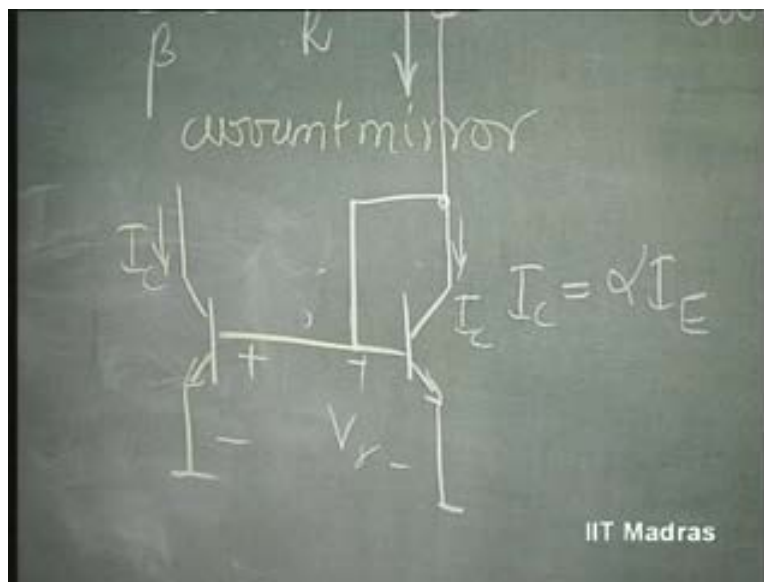
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This is a unique way of biasing because the collector current gets fixed at a value that you decide, independent of the transistor Beta and  $V_{\gamma}$ . That means it is a stable current of operation. What use of this kind of structure? Now, I will use this  $V_{\gamma}$  in order to bias another identical transistor. This is an identical transistor which when given the same value of  $V_{\gamma}$  will produce the same current,  $I_C$ .

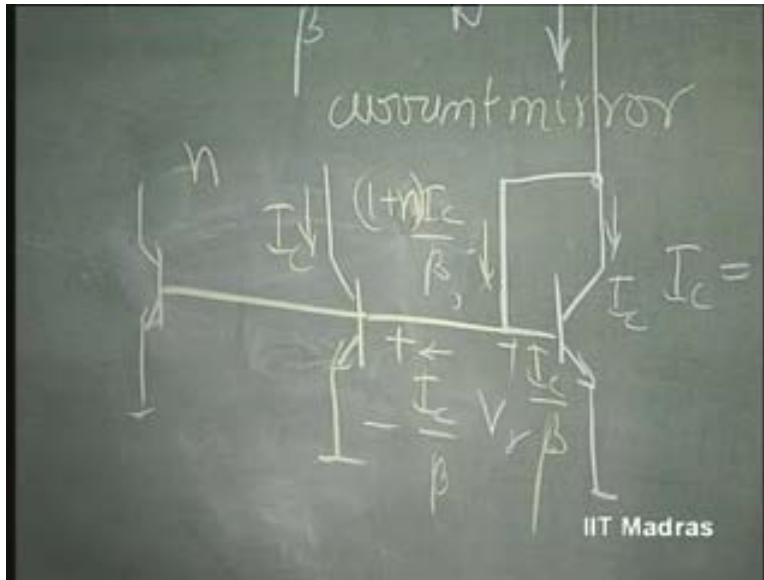
So you say, this current is mirrored here, if these two transistors are identical. And this is called a current mirror because this current is reflected here, because of these two transistors being identical, this structure with transistor connected as a diode connected to another transistor is called a current mirror; it reflects the same current here.

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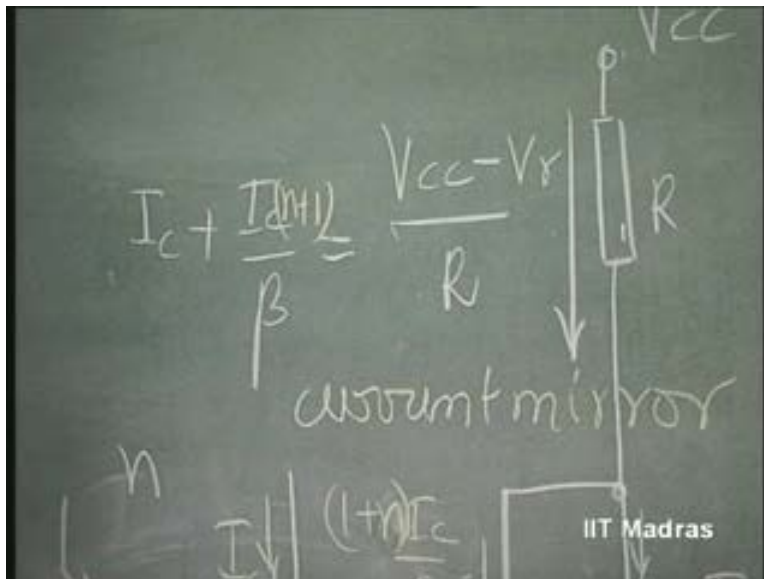
Only thing is, now this is  $I_C$  by Beta; this is also  $I_C$  by Beta. And therefore, this current is now twice  $I_C$  by Beta. If I connect another transistor, this will become thrice  $I_C$  by Beta. Therefore, if I connect  $n$  transistors, this will become  $n$  times  $I_C$  by Beta plus...if I connect  $n$  such transistors, it will become  $n$  times  $I_C$  by Beta plus 1 of this.

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So, that means, here you get this as  $n + 1$ , as long as Beta is very high compared to  $n + 1$ . Consider Beta of the order of 200 or so. That means  $n$  can go as high as 10. Even then,  $I_C$  is same as  $V_{CC} - V_{\gamma}$  by  $R$ .

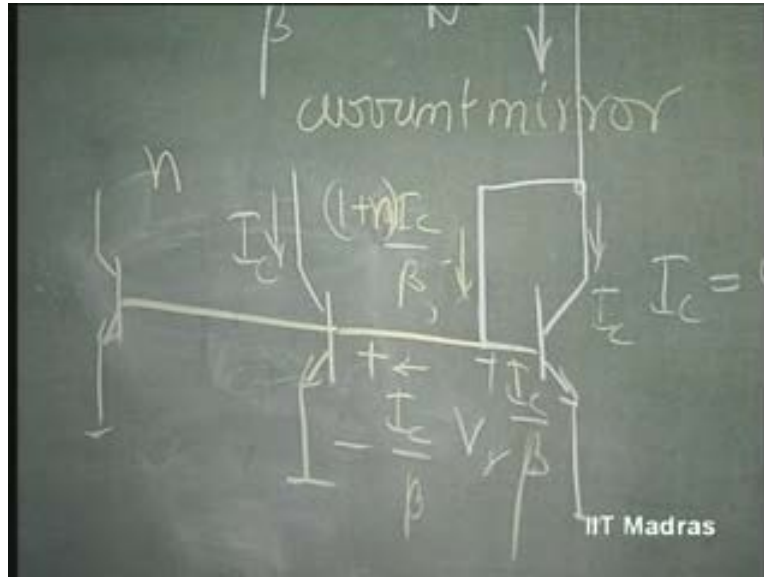
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That means I can have 10 such transistors getting biased at a stable current of  $V_{CC}$  by  $R$ . This is fantastic because I can use these current sources at ten different places for

biasing the various devices at the same current, which is  $V_{CC}$  by  $R$ , without using any extra resistor; just by using one resistor, which converts the voltage into current, which otherwise should have been done by ten different resistors.

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So, this is a common technique of biasing. Now, what will be the resistance seen from here? It is that of a current source;  $1/\beta r_{CE}$  which is typically of the order of mega ohms, I have told you. This is a common emitter configuration. Impedance seen here is typically of the order of mega ohms because of early effect, I told you, right? So, this impedance is very high. That means it is giving you current of whatever value you want and gives you an impedance of the order of mega ohms. So, this can be straight away used as current source. So, this is what is used as a sink, for example. This...these are all sinks. If you do the same thing using P N P transistor, they will be all sources.

So, we will see how this can be used in a differential amplifier, getting rid of resistors, in the next class.