**Electronics for Analog Signal Processing - I**
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Lecture - 34
MOSFET Differential Amplifiers

Now we will analyze MOSFET differential amplifiers. As far as the evolution of the differential amplifier is concerned, it follows the same lines as that of the BJT.

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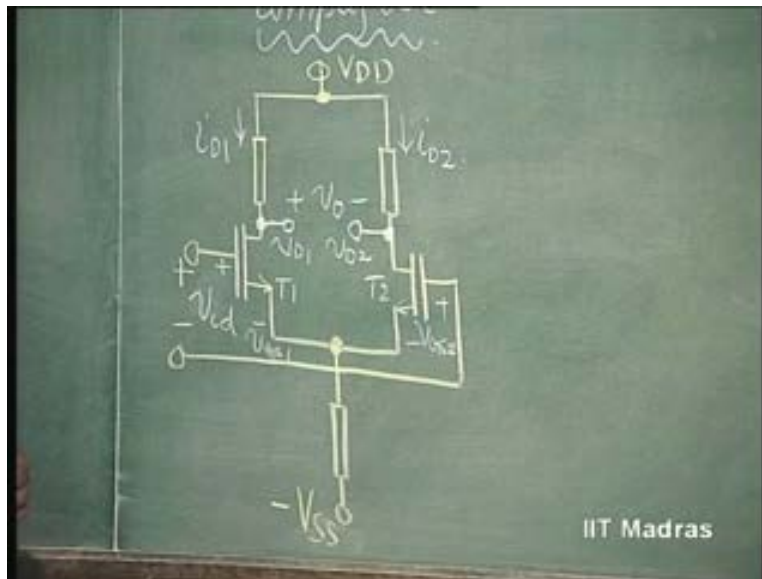
And, we can also conclude same thing about its gain. It is also equal to minus g m into R D. So, there is no difference except that in the last signal, it behaves differently. Let us see therefore how... So, as far as small signal, this thing, is concerned, its gain is the same – g, minus g m into R D; and input impedance is infinity, of course. Now, in the last signal situation, let us see how it differs. V i d in this case, the differential signal…only when differential signal is applied, we want to analyze this; when common mode signal is applied, once again, the gain is exactly similar. That is, it is dependent upon R D by, let us call this as R S instead of R E.

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So, R D and R S, ratios; so, exactly similar lines. We can split it into two separate blocks and evaluate it as R D by 2 R S; minus R D by 2 R S. So, V i d now is equal to, for large signal, V G S 1, instantaneous value, minus V G S 2, instantaneous value; V G S 1 minus V G S 2. Next, we know that…we will go from here. I, V D D minus i D 1 into R D… This is R D; this also is R D; equals V D 1, at this point.

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Similarly, V D D minus i D 2 R D is equal to V D 2, at any instant of time. And V naught is equal to V D 2, V D 1 minus V D 2 as defined here, which will be nothing but…let us see. It is i D 2 minus i D 1 into R D, from these two equations.

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V D 1 minus V D 2 is i D 2 minus i D 1 into R D. So, we have i D 2 minus i D 1 equals V naught by R D; an important equation. And what is i D 2 plus i D 1? To get it, I d 2 plus I d 1 is equal to, we will call this again, on similar lines as the BJT differential amplifier, as I naught.

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So, from these two equations, we can write down i D 2 as equal to...add these two; I naught by 2 plus V naught by 2 R D. Is this clear? 2 i D 2 is this plus this. So, i D 2 is this plus that by 2.

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$$= (i_{D2} - i_{D1}) R_D$$

$$i_{D2} - i_{D1} = \frac{v_o}{R_D}$$

$$i_{D2} + i_{D1} = I_o$$

$$i_{D2} = \frac{I_o}{2} + \frac{v_o}{2R_D}$$

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 And i D 1 equals, subtract this, this from this, you get 2 i D 1. So, I naught by 2 minus V naught by 2 R D.

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$$i_{D1} = \frac{I_o}{2} - \frac{v_o}{2R_D}$$

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$$i_{D1}$$

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So, you got i D 1 and i D 2 in terms of V naught and I naught. Now, i D 1 is also known to be equal to K into V G S 1 minus V T whole square; or, from which, we get V G S 1 as root of i D 1 by K plus V T. Similarly, V G S 2 is root of i D 2 by K plus V T. Therefore V G S 1 minus V G S 2 which is defined as V i d, V G S 1 minus V G S 2 defined as...V I D is nothing but root of I D 1 minus root of i D 2 by root K.

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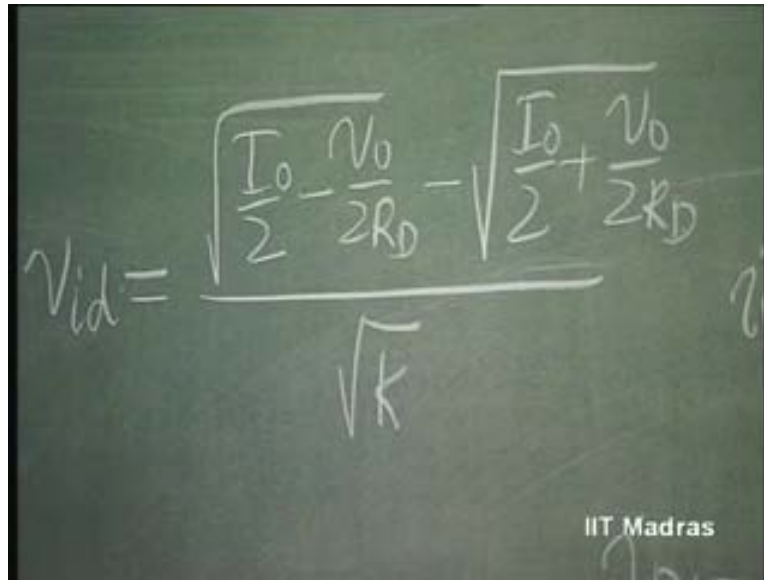
So now, i D 1 and i D 2; you substitute from that, you get this as... I D 1 was I naught by 2 minus V naught by 2 R D, minus I naught by 2 plus V naught by 2 R D, whole thing divided by root K is V i d.

$$V_{id} = \frac{\sqrt{\frac{I_0}{2} - \frac{V_0}{2R_D}} - \sqrt{\frac{I_0}{2} + \frac{V_0}{2R_D}}}{\sqrt{K}}$$

So, this is giving you V i d as a function of V naught. But we want V naught as a function of V i d. So, we can actually now see that root K into V i d whole square... I take this on to this side and square the whole thing. This is equal to...this minus this whole square which is I naught by 2 minus V naught by 2 R D plus I naught by 2 plus V naught by 2 R D. This square plus this square minus this into this; this into this. That is root of I naught by, I naught square by 4, minus V naught square by 4 R D square. This into 2; this whole thing is equal to K into V i d square. Is this clear?

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So, this I naught by 2 and this whole thing simplifies to simply I naught; or we get I naught minus K times V i d square equals 2 root I naught square by 4 minus V naught square by 4 R D square.

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Now, what do we do? We have to square, once again, I naught... We will take this as square plus K square V i d to the power 4 minus 2 K V i d square I naught. This is going

to be equal to 4 times I naught square by 4 minus V naught square by 4 R D square. Clear?

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$$\left(I_0^2 + k^2 V_{id}^4 - 2k V_{id}^2 I_0\right) = 4\left[\frac{I_0^2}{4} - \frac{V_0^2}{4R_D^2}\right]$$

So now, you have this getting cancelled with this. This is I naught square; that is I naught square; and we get this as minus V naught square by 4 R D square. 4, 4 gets cancelled. So, we make this plus. Or, we want V naught. So, V naught by R d, root of that. We take root of this. If we take root of this, we have V i d square V i d to the power 4 here. So, V i d we get; and we will take actually the whole thing out. 2 K, root of 2 K into I naught, when I am taking the root, I naught 2 K; root of that into V i d 1, root of 1 minus... I have taken out V i d square; so, we get V i d square remaining there. I have taken out K. So, K remains there. I have taken out 2. So, it will be divided by 2. I have taken out I naught divided by I naught. Is it clear? Please check that.

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So, this is the relationship between input and output. V naught into this. So, V naught is equal to R D into V i d root of this into that, square root. It could be plus or minus. So, it is strictly speaking minus because that is a phase shift of 180 degree as we have assumed the polarity.

So, this factor, if you verify, minus R D V i d root of 2 K into I naught. If you verify, please verify. This factor, 2 root of 2 K I naught is nothing but what? - the g m. If you verify, the g m of the whole thing will be this; g m into R D.

Then, each of the FETs will be operating at I naught by 2. See, operating current of the FET will be I naught by 2, from which we can obtain the g m of the FET, from its characteristic. So, you will see that this is nothing but g m, minus g m, into R D into V i d which is the small signal gain. Apart from that, we have a non-linearity coming into picture.

In order that it is perfectly linear, now we get an important factor regarding distortion. K into V i d square divided by 2 I naught should be much less than 1. So, K into V i d square divided by 2. I naught should be much less than 1. This is going to be small signal;

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then it is perfectly linear. So now, like, we have got in the case of differential amplifier using BJTs, we got V p square divided by 96 V T square or something like that; much less than 1. Similar to that, we have got a condition here.

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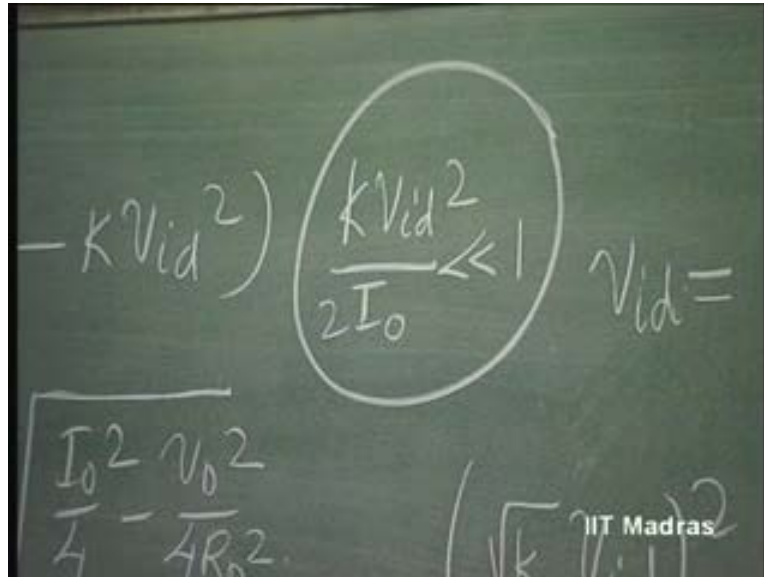
But here, please remember, we have not yet obtained the harmonic distortion. This is only the square root of 1 minus this kind of thing. If this factor is much less than 1, then I can make certain approximations. What are those approximations?

If this factor is much less than 1, the square root can be approximated as…you know mathematics…1 minus...if this 1 minus, square root of 1 minus x and x is small, what is square root of 1 minus x? 1 minus x by 2. So, square root of this. Therefore, approximation under this assumption, V naught is equal to minus R D root of 2 K I naught into V i d into 1 minus K V i d square divided by 4 I naught. Square root is gone.
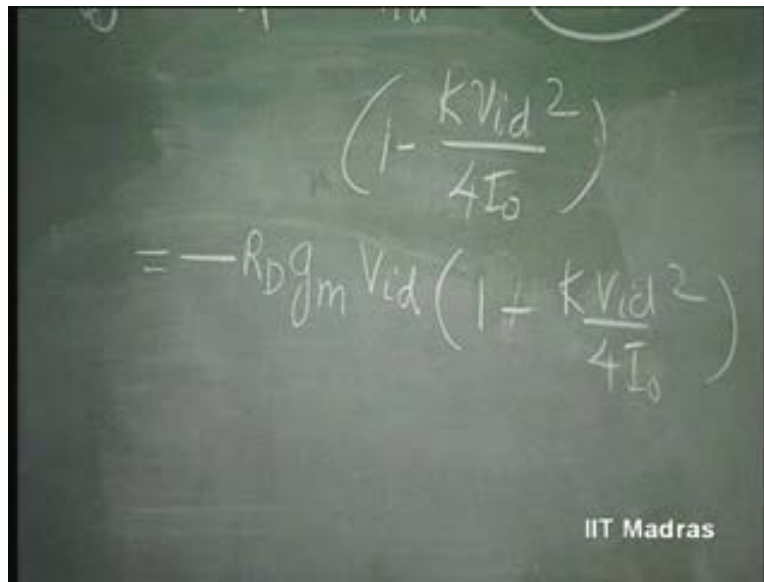
Now, what is the non-linearity existing? Again, you can notice something. This is V i d and there is V i d cube. So, if you go for only sort of amplifier using, let us say, common source amplifier instead of common emitter, using MOSFET you go for common source. The non-linearity will be square non-linearity; the second harmonic is the first component; in fact, the only component that comes into picture for distortion. But it is going to be dominant. Here, in the differential amplifier, you will see that the harmonic component is what? - third harmonic, like in the case of bipolar junction transistor.

Now in this, V naught is equal to minus R D into this factor is nothing but g m; and this is V i d. So, this is what happens to the signal; linear part of the signal component. This into 1 minus K times V i d square by 4 I naught.

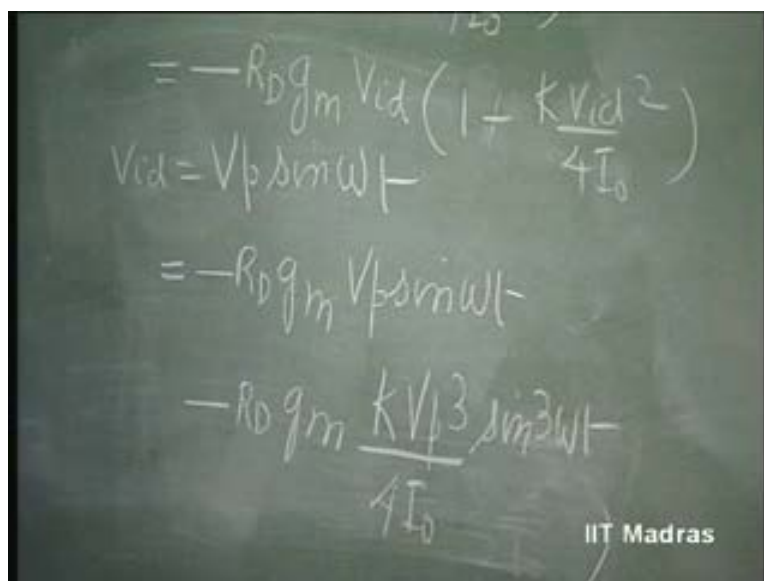So now, suppose V i d is taken as V p sine omega t. Then, what happens? Let us see. So, we have the fundamental component coming as minus R D g m into V p sine omega t. That is clear. So now, what is the component corresponding to the other part? Minus R D g m. Now, we will take this V p inside, sine omega t. So, we get K into V p cube sine cube omega t by 4 I naught.

Now, sine cube omega t... Yesterday also, we had converted into 3 sine omega t minus sine 3 omega t by 4.

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So, we can now see that this 4 combined with this, you get 16. So, the third harmonic component is going to be K V p square divided by 16 I naught as against V p of the fundamental. g m R D is a common factor for both.

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So, let us do the same thing that we did earlier. So, the fundamental component will be minus g m R D into V p; T component of the fundamental; and this one, the harmonic percentage dis… or ratio of the distortion is going to be again minus g m R D into V p K V p square by 16 I naught.

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$$D = \cfrac{+g_m R_D V_p \left(\dfrac{K V_p^2}{16 I_0} \right)}{+g_m R_D V_p} \left(\dfrac{1}{2} \right)$$

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Is this clear? So, you can see now that this K V p square by 16 I naught should be kept at whatever value you want; 1 percent – it means 1 over 100. That will give you the value of, maximum value of, V p for which it can be used.

Now, I want you to work out the same problem that we worked out with BJT differential amplifier compared with BJT common emitter amplifier. Here, compare common source amplifier which has square law distortion coming into picture at the output and second harmonic component coming at the output. Find out the V p required for 1 percent distortion at the output in both the cases and compare these and you will definitely see that differential amplifier is far superior to the common source amplifier. So, distortion wise, this amplifier is definitely superior. Therefore, again, we will never go for such common source amplifiers as discrete stages; we will go for the differential amplifier because it has superior large signal properties.

 Now, as far as the current switching, etcetera, that we discussed in the earlier situation is concerned, here also, it is valid. The current gets completely switched over to this when V i d is positive and large; and current gets completely switched over to this when V i d is negative and large. And therefore, the output voltage swing is again equal to twice i not into R D.

So basically, except for the non-linearity, the rest of the things remain the same. This output swing is once again obtained only when these transistors do not go to the triode

region when the full current is flowing through these; just like BJT not going to saturation when the full current is flowing through this. Only under this assumption we have this full swing of 2 I naught R D peak to peak, symmetric swing, because of the differential signal.

Now, as far as common mode operation is concerned, again the same thing is valid; that if I shot this, no V I d is there. Then, there will not be much of a change that is going to occur here. This voltage can keep on rising until this voltage, which is drain to gate voltage, becomes equal to minus V T; until the drain to gate voltage becomes equal to minus V T, at which point of time, it is entering the triode region.

So, that will be the limiting common mode signal, upper limit on common mode signal that you can apply to this differential amplifier. On the lower side, obviously, it can go on until I naught becomes equal to zero. So, these are the signal limitations of the differential amplifier, both for common mode and differential mode. When both of them are coexisting, obviously, the voltage here, the minimum voltage here, is likely to be V D D minus I naught into R D; and that will set up a limit on this.

Just as we have discussed offset voltages in BJT differential amplifiers, let us also consider offset voltages in mos differential amplifier.

Now, in the last class when we discussed the offset in BJT, what we said was there is an output offset voltage and that is very easily defined as…voltage is that voltage that appears at the output when input is made zero. So, V i d is zero. Under that situation, why would output have an offset?
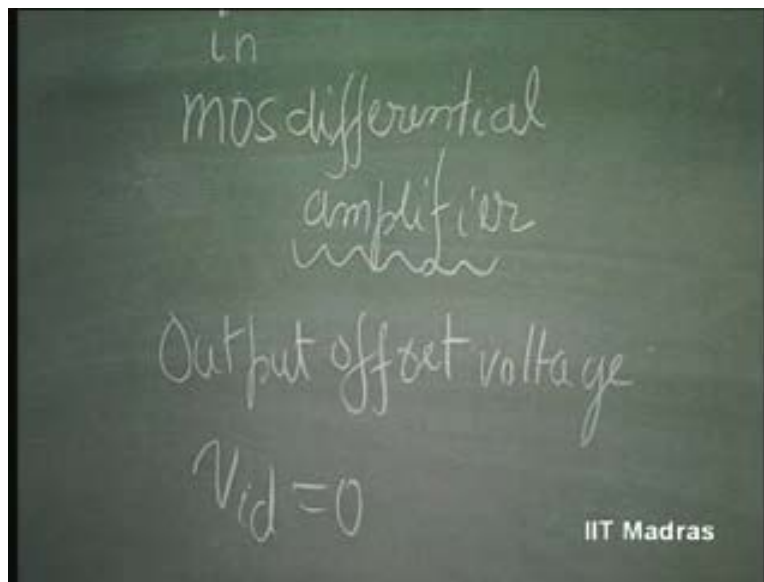
Obviously, i D 1 is not equal to i D 2 because i D 1 is equal to K times V G S minus V T and this V G S because…as far as the MOSFET is concerned now, input is grounded and the sources are connected together; both the inputs are grounded, sources are connected together. So, what happens? V G S will be the same for both. V G S 1 is same as V G S 2. So, V G S 1 is equal to V G S 2 is equal to V G S, under this situation.
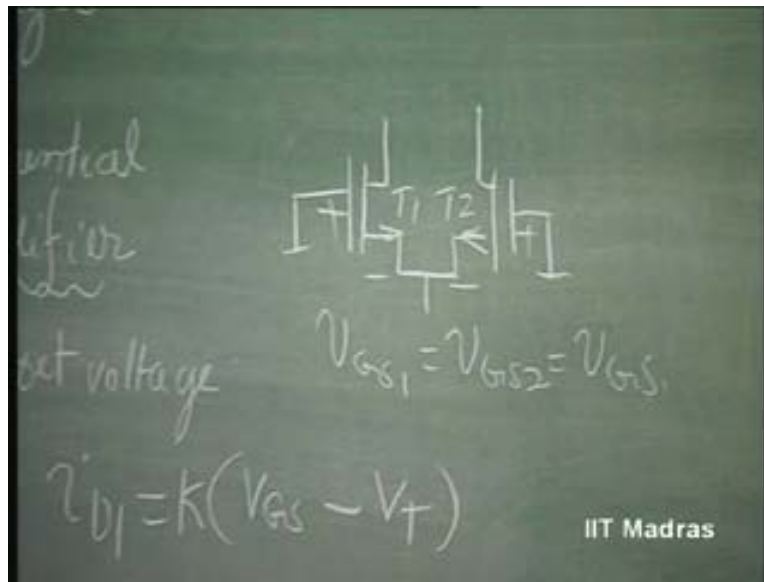
So, this is K times V G S minus V T whole square. i D 2 is also K times V G S minus V T whole square; but they are not identical. They can have the K as K 1 and K 2; and of course, V Ts also can be V T 1 and V T 2, but we are assuming that the threshold voltages are same. And threshold voltages are process dependent and this is process dependent as well as geometric bit dependent. We are assuming that there is mismatch only in geometry. So, K 1 and K 2.

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So then, we know that i D 1 is different from i D 2. So, V naught is simply i D 2, V naught offset, i D 2 minus i D 1 into R D. According to us therefore, this is equal to…we have here K 1 i D 1, i D 2, minus K 2 minus K 1 into V G S minus V T whole square into R D.

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So, it is the mismatch factor which is responsible for the output offset and V G S minus V T whole square is nothing but i D 1 by K. So, we can put this as i D 1 by K; and what is i D 1? i D 1...since these are...it is going to be very nearly equal to I naught by 2. It is going to be slightly different because of the fact that K 1 is going to be different from K 2. So, i D 1 by K into R D, K 1; i D 1 by K 1 or i D 2 by K 2 is equal to this. So, this is the output offset. Is it clear?
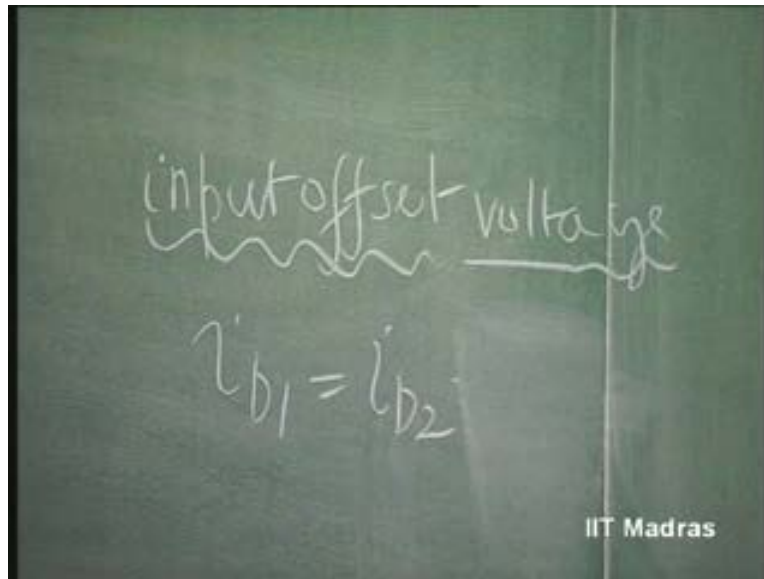
Now, in a good differential amplifier, i D 1 will be very nearly equal to i D 2; will be very nearly equal to I naught by 2, nominally. But, they will be different because of the fact that K 1 is slightly different from K 2. So, in this expression therefore, you can put i D 1 as I naught by 2 and this K 1 very nearly equal to K 2. Fine.

What about input offset? Now, as far as input offset is concerned, what is the basic definition? It is that voltage that I have to apply at the input, in order to make the output equal to zero.

That means under this situation of K 1 being different from K 2, I am making i D 1 equal to i D 2. If I make i D 1 equal to i D 2, output voltage will be, offset voltage will be, zero. So, i D 1 is made equal to i D 2 equal to I naught by 2. Under this situation, what is going to be the... I mean i D 1 is going to be equal to i D 2. We are not interested in this factor. i D 1 is equal to i D 2.

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Under this situation, we have K 1 into V G S 1 minus V T whole square equal to i D 1; or V G S 1 is equal to root of i D 1 by K 1 plus V T. V G S 2 is equal to root of i D s, sorry, i D 2 by K 2 plus V T.

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So, V G S 1 minus V G S 2 is the V i d, input offset. This is input offset voltage, when i D 1 is equal to i D 2. So, we have this equal to root of i D 1 or i D 2, whichever; both are same; into 1 by K 1 minus 1 by K 2; root of K 1 and root of K 2. This is the what? This is the input offset voltage.

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Here, please note that we had assumed K 1 and K 2 to be different. This could have resulted in the input offset...could have been resulted also because of V T 1 and V T 2 being different. That means this plus V T 1 minus V T 2 is going to be the further addition to this input offset. This is what you should bear in mind.

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And therefore, because of such uncertainties in these two parameters, typically a MOSFET differential amplifier has about 20 millivolts offset voltage, as against, what did we get for BJT? - of the order of 1 to 2 millivolts; an order of magnitude higher input offset voltage for MOSFET. This is to be borne in mind by a design engineer because we will therefore never use a MOSFET as a differential amplifier stage at the input of any amplifier, if offset has to be reduced.

Obviously, this is what is called Delta V G S offset because primarily it comes because of V G S being different for the same current. This is called Delta V G S offset as against in BJTs it is called Delta V B E offset. So, this is of the order of 20 millivolts as against 2 millivolts in ((meter Refer Slide Time: 32:50)).

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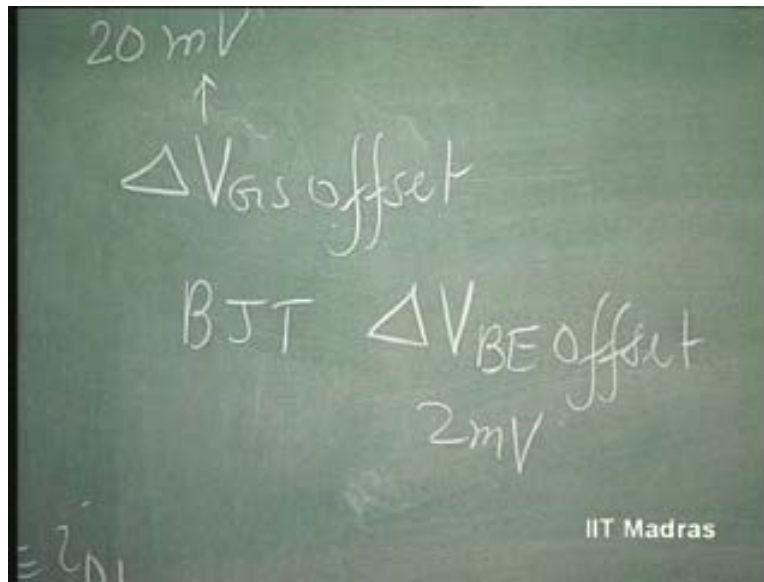
So, at any time you can say therefore that, as far as Delta V B E or Delta V G S offset is concerned, BJT is the one to be selected. And also in this I said, if you go for higher input impedance by pairing Darlington transistors as differential pairs, then the uncertainty here will go to double; instead of 2 millivolts it will become 4. If you use 3 such transistors, it will become 6 millivolts, even though the Beta is progressively increasing and the base current is progressively decreasing for this; or, input impedance is progressively increasing.

This is the configuration with the highest input impedance, infinity; and there you have maximum offset. This is the case with any amplifier configuration. If you try to increase the input impedance, input offset will increase. There is always a price that you pay, somewhere or the other. So, when you try to increase the input impedance by any means, the input offset voltage will increase. This is a serious problem particularly in D C amplifier or low frequency amplifiers.

So, where the input offset is of no consideration, where other offset voltages are more dominant, there you can use MOSFET differential amplifier. Now, what are the other

offsets that can come about is what I would like to discuss in the few minutes that are left.

First, consider the bipolar transistor. Now, this is what is called Delta V B E offset. When both the bases are connected together, V B Es are the same. At that point, the two currents are different.

Now, you can have, apart from this, because of finite base current and finite base resistance that you are putting some base resistance, let us say, R B 1, R B 2 in your circuit. That means it is not grounded straight. It is grounded through a D C resistance of R B 1 and R B 2 through the respective bases. In such a situation, in this case, you have what is called I B 1; and in this case, you have I B 2.

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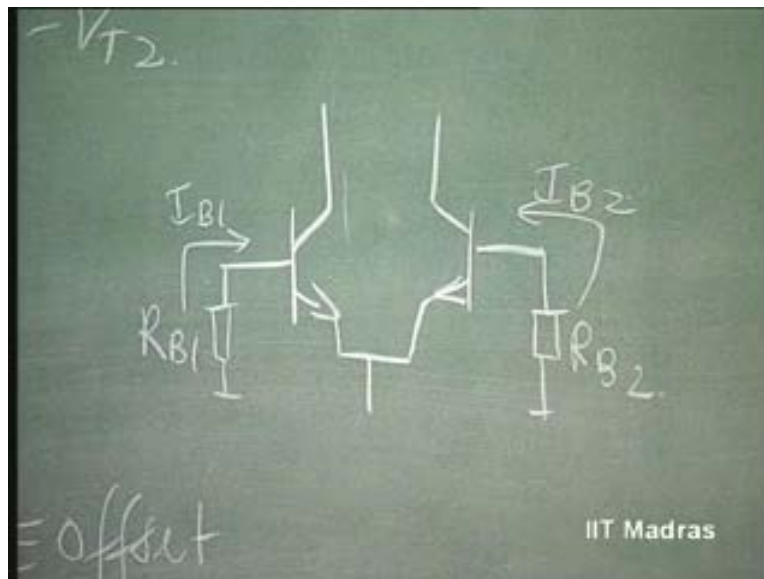
So, this will develop a voltage of I B 1 into R B 1 and that will develop a voltage of I B 2 into R B 2. The differential voltage applied to the base now is I B 1 R B 1 minus I B 2 R B 2. This is the differential voltage. If I B 1 is same as I B 2, R B 1 is same as R B 2, this voltage is zero. So, R B 1 should be same as R B 2; I B 1 should be same as I B 2. R B 1

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and R B 2 are external resistances that are put. So, even if I B 1 and I B 2 are not equal, we can make these resistances such a way that this whole difference is equal to zero.
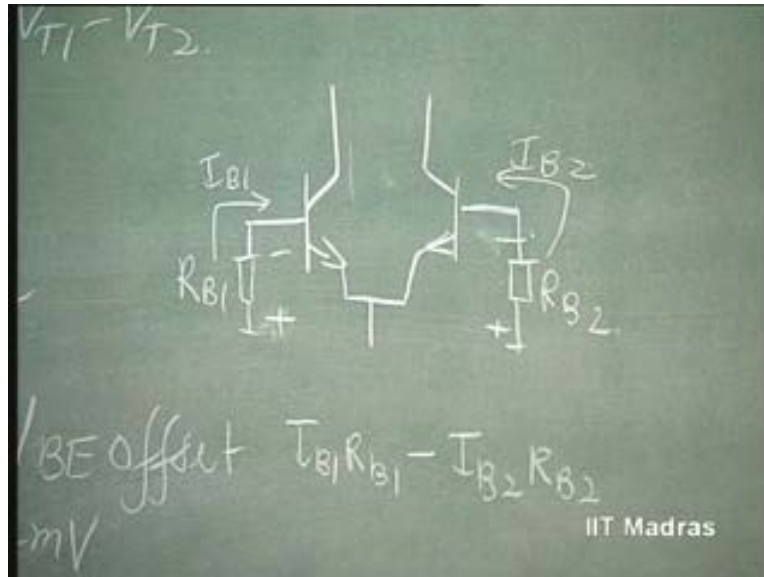
This kind of offset is called bias current, input bias current offset. That means this arises whenever I B 1 is not equal to I B 2. This can happen because even if these two currents are the same, even if these two currents are the same; because, the Betas are drastically different. Alphas may be very nearly equal to 1. One Alpha may be point 995; another Alpha may be point 994. That means Alphas are very nearly the same; but Betas can be now drastically different. And therefore, these two base currents may be different for the same matched pair. Base currents may be different because Betas are going to be different; and therefore, the bias current flowing through the different base resistances through this will create an offset.

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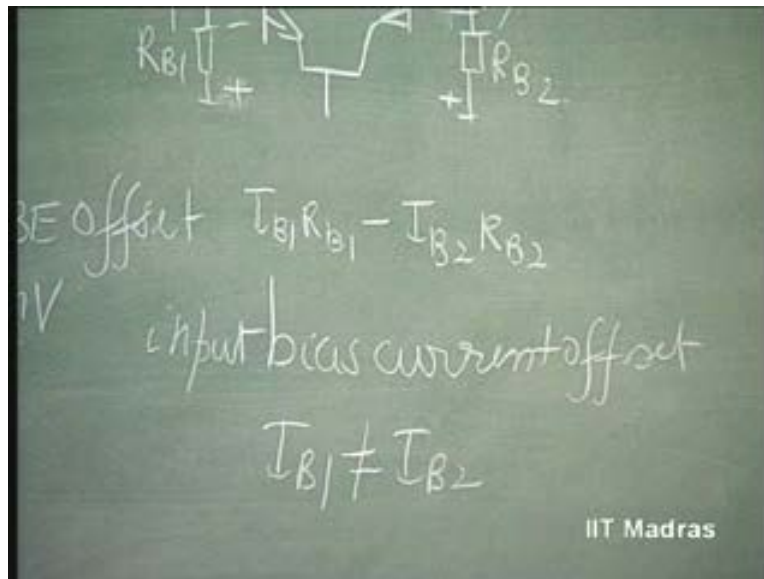
And this is an important design requirement; that if you are worried about biased current flowing through resistance, this bias current may be very low. That depends upon the value of Beta. It will become still lower when we are using the Darlington pair. So, that means using Darlington pair or using MOSFET or JFET, we will make this bias current offset progressively come down.

It is very bad in the case of a single pair of transistor. So the bias current offset is a serious problem in the case of a BJT and when it is a single pair. It is of no concern when it is a MOSFET, because bias current is almost zero. So, it is almost non-existent in the case of a MOSFET. So, if you have the sources coming with large resistances at the inputs which were therefore called bias current offset, then you will use MOSFET as input stage.

But, if you are sure of sources with low valued resistances coming at the input, where the bias current offset is going to be extremely small because the impedance R B 1 and R B 2 are going to be very low, then we will use bipolar junction. So, application depends upon the source that you are going to choose for your application. So, this amplifier...what it is going to be; whether it is going to be MOSFET input or BJT input depends upon the

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source impedance and whether it is a low frequency application or not. So, this is an important aspect about offset. The total offset is going to be bias current offset plus Delta V G S offset, or Delta V B E offset; and the voltage may be able to drift either because of bias current offset voltage or because of Delta V B E or Delta V G S offset or both.

Let us now work out an example using this MOSFET differential amplifier - Example 15. Determine the following for the MOSFET differential amplifier shown biased at I naught equal to 2 milliampere.

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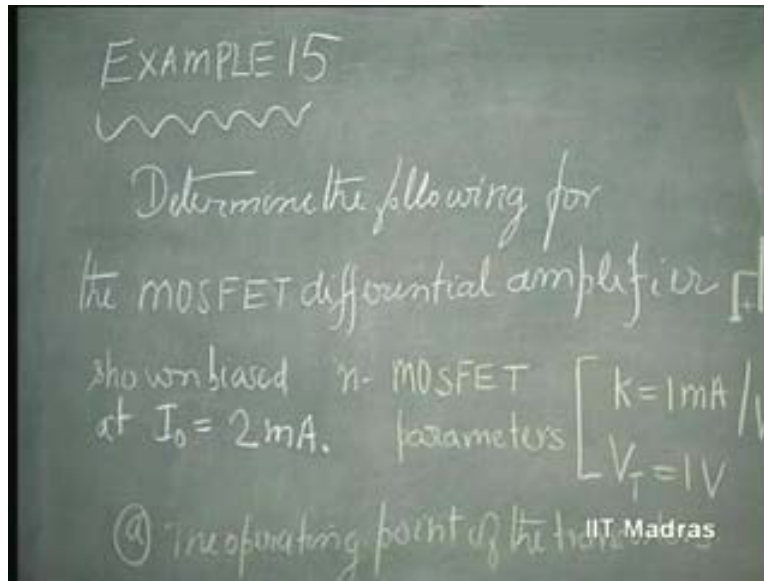
The MOSFET differential amplifier is shown here. T 1, T 2 biased at I naught equal to 2 milliamperes. If it is 2 milliamperes here, then we know that this current and this current being equal will be equal to 1 milliampere each.
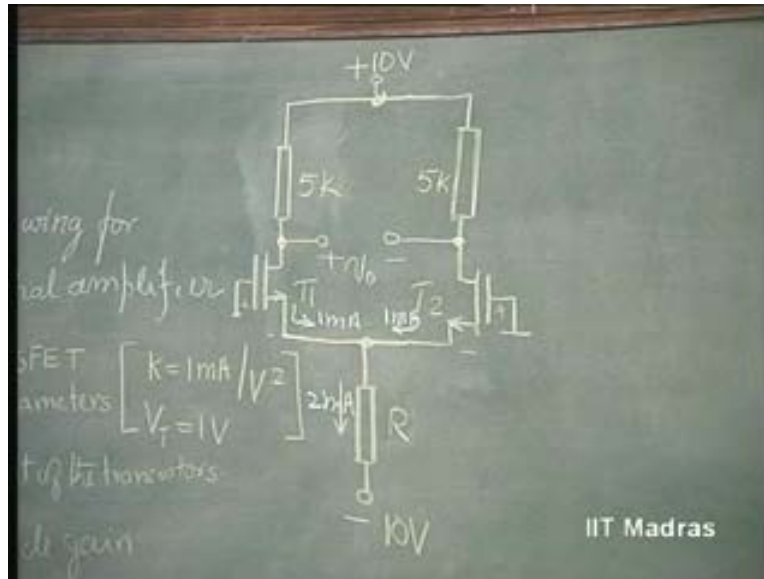
So, we know that I D S Q is equal to 1 milliampere; is equal to K into...which is 1 milliampere per whole square into V G S Q minus V T whole square. So, this is 1. So, V G S Q is equal to 2 volts from this; 2 minus 1 is 1, equal to 1.
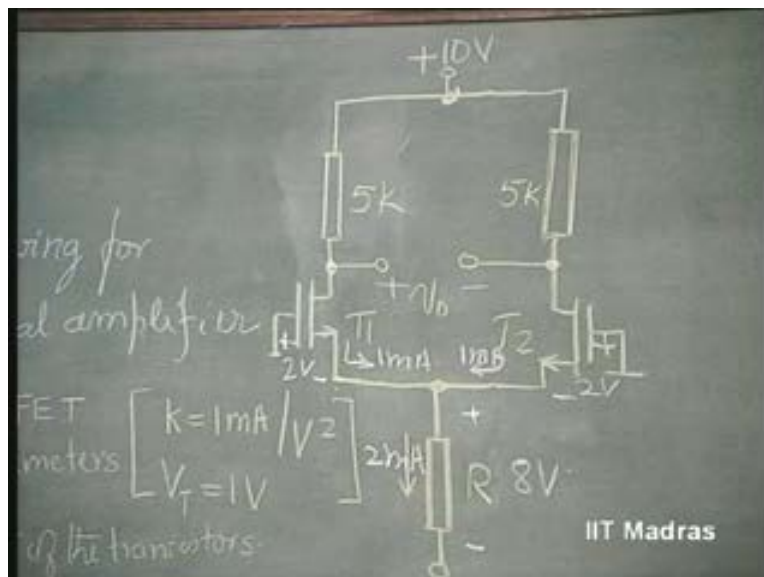
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$$I_{DSQ} = 1mA$$

$$1 = 1\left(V_{GSQ} - 1\right)^2$$

$$V_{GSQ} = 2V$$

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So, we get from this relationship that V G S Q here becomes 2 volts each. So, this is plus; this is minus; this is plus; this is minus; this is 2 volts; this is minus 10 volts. So, the drop across this is 8 volts.

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We want to have 2 milliamperes through that and 8 volts is the drop across it; and therefore, R is equal to...R is equal to 8 volts divided by 2 milliamperes which is equal to 4 Kilo ohms.

So, we get the value of R required to bias this at 2 milliamperes as equal to 4 Kilo ohms. Now we are in business. We can first find out the operating point of the transistors. This is already given as 1 milliampere because this is 2 milliamperes. So, the voltage here is going to be a drop of 5 volts; 1 milliampere into 5 K is 5 volts. So, this is 10 volts. So, this voltage is 5 volts; this is 5 volts. So, V D G Q is 5 volts and I D S Q is already given as 1 milliampere. So, this is the operating point.

Then we want the differential mode gain. We would like to now find out the g m of the FET. g m is equal to...we know that it is 2 K into V G S Q minus V T because I D S Q is equal to K into V G S Q minus V T whole square. Differentiating with Delta I d by Delta V G S comes as 2 K into V G S Q minus V T. That is, V G S Q minus V T into K, this whole square is equal to I D S Q.

So, strictly speaking, in this case, I D S Q is always equal to I naught by 2 for the differential amplifier. So, I would like to express g m of a differential amplifier in terms of I naught. So, I D S Q is always equal to I naught by 2 for differential amplifier. That means V G S Q minus V T is equal to root of I naught by 2 K from this, always. Therefore, g m of the differential amplifier is equal to 2 K into root of I naught by 2 K which is always equal to I naught into 2 K.

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So this...earlier also I have mentioned...you have substituted for g m; root of I naught into 2 K, given I naught as 2 milliamperes and K as 1 milliampere per whole square. We have g m equal to root of I naught. This is 2 milliamperes into 2 K, which is milliampere per volt square. We get 2 millisiemens as the g m of the differential amplifier.

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So, the gain of the differential amplifier is simply g m into R d. This we had established. Minus g m into R d; this is the differential mode gain. So, this is equal to minus 2 into R d is 5 K. So, this is minus 10. So, this is the differential mode gain single ended output. This is equal to minus 5. That is, it is minus g m into R d by 2. So, the b part is over, differential mode gain.

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Now, we have to discuss about common mode gain. So, common mode gain also, we can replace the whole thing by its equivalent circuit and do it; and we can show that it is similar to what we obtained in the case of a bipolar junction transistor.

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So, one way is you can replace the whole thing by its equivalent circuit 5 K. This is connected to ground; and you have the g m into V g s and we are having it at the source;

and from the source, we have to the ground, a resistance of now, 2 R. R is already known as 4 K. So, 2 R is equal to 8 K. So, this is the ground; g is... So, this is the equivalent circuit that we have to solve.

So, we would like to now find out the output here; and through the output, we have this current flowing, g m into V g s. So, g m into V g s into 5 K is the output. That divided by the input... Now, this is actually...the same current is going to flow through this particular thing. And therefore, the V g s is going to be the input.
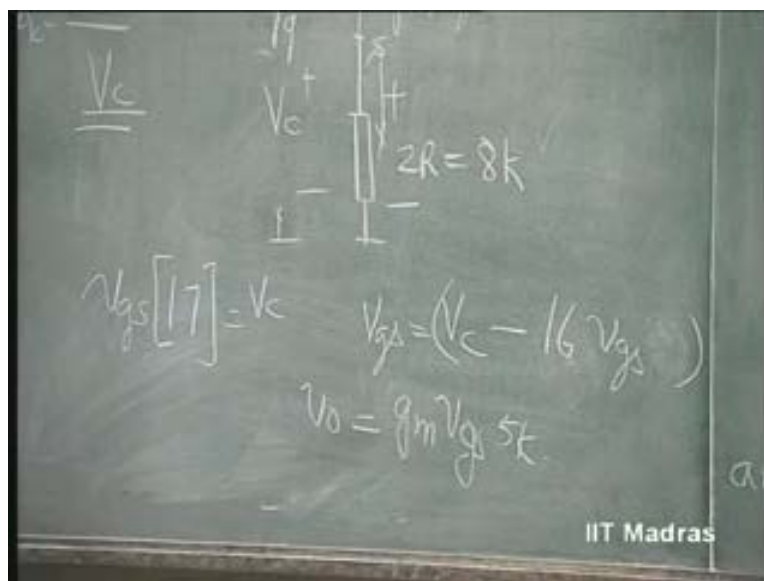
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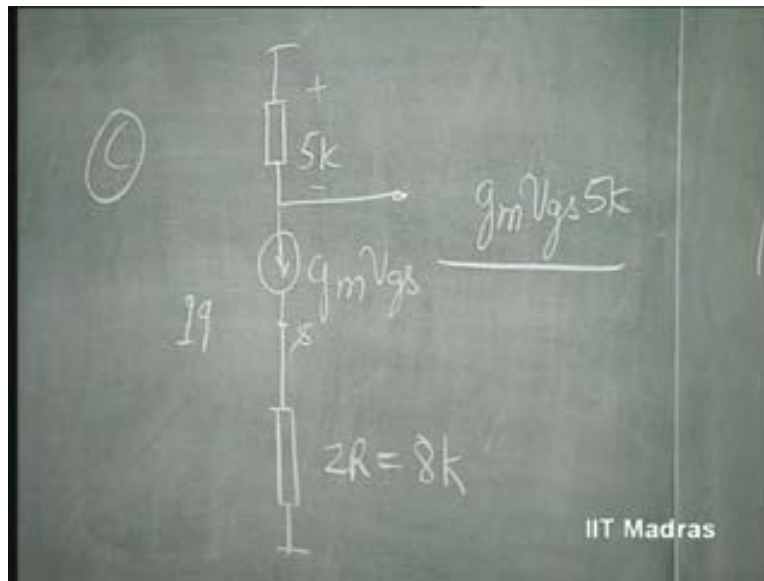
So, actually speaking, we are going to apply a voltage here from this point to ground which is the common mode voltage. So, the input is going to be V g s, which is V C minus g m V g s, g m into V g s, because this is going to develop a potential like this. So, into 8 K; this is the V g s here. V g s is V C minus the drop here; g m V g s into 8 K. So, output is, V naught is equal to g m V g s into 5 K.

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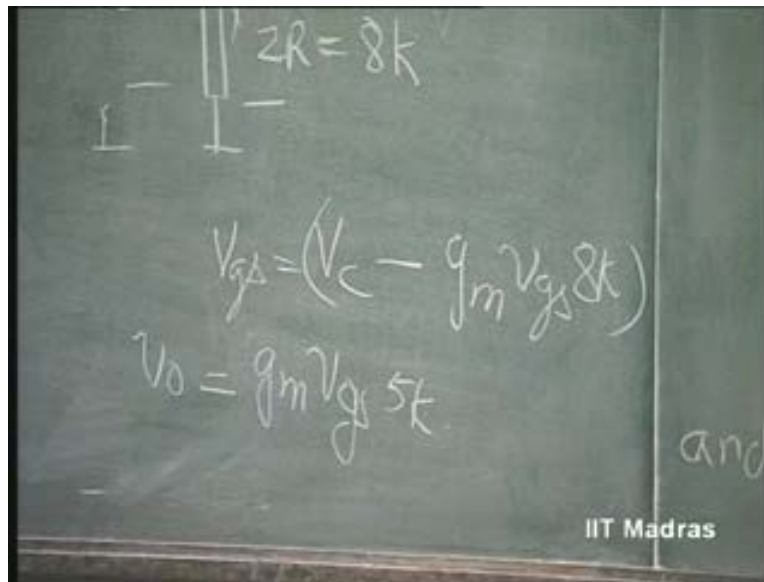

So, we can actually eliminate V g s from this and obtain V C divided by... That is V naught divided by V C as the common mode gain. So, V g s is equal to V C minus g m V g s 8 K. That means V g s into, g m is already given as 2 millisiemens. So, this is going to be 2 into 8 K. 2 into 8 K is 16. So, V g s into 17 is equal to V C.
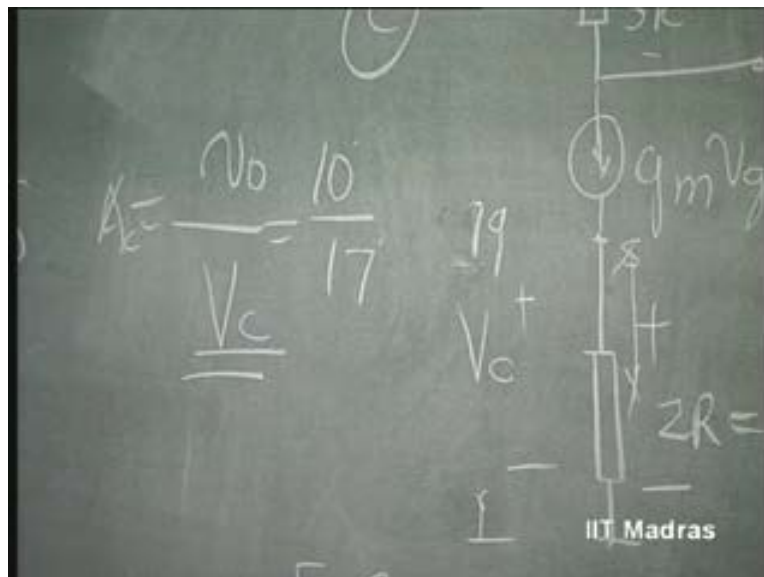
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So, we have got V C in terms of V g s. So, we substitute it there. V naught is equal to g m V g s into 5 K. So, g m V g s into 5 K. So, this is g m into V g s; is going to be equal to 10 V g s; g m into V g s is 2 into 5 K; so, 10.

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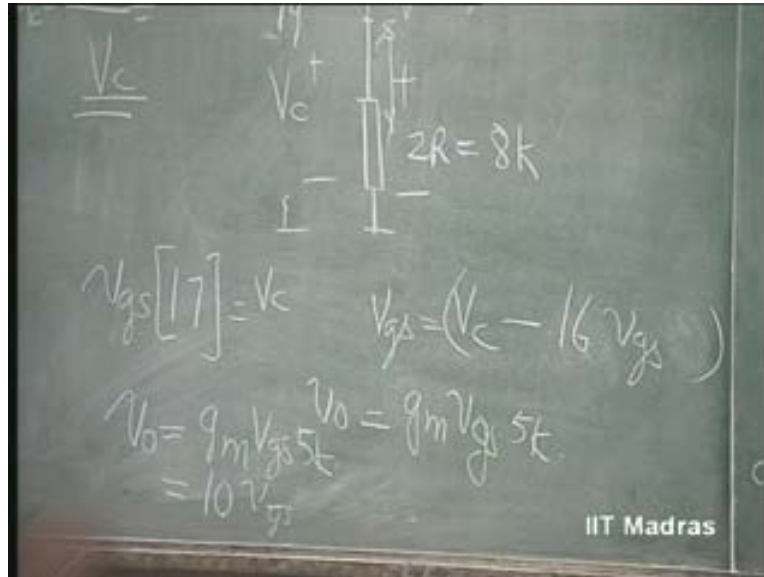
So, 10 V g s divided by V C which is 17 V g s. So, you can see that the common mode gain is 10 by 17.

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So, common mode rejection ratio, CMRR is A d by A c which is equal to 5 divided by 10 by 17; or this is 8 point 5.

So, we have now worked out for this differential amplifier, all these - the operating point of the transistor, differential mode gain, common mode gain and C M R R.