Electronics for Analog Signal Processing - I
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Lecture - 33
BJT Differential Amplifiers

Continuing our discussion about differential amplifier, we saw in yesterday's lecture how V i d is V B E 1 minus V B E 2; and i E 1 minus, i E 1 plus i E 2 is I naught at all times.

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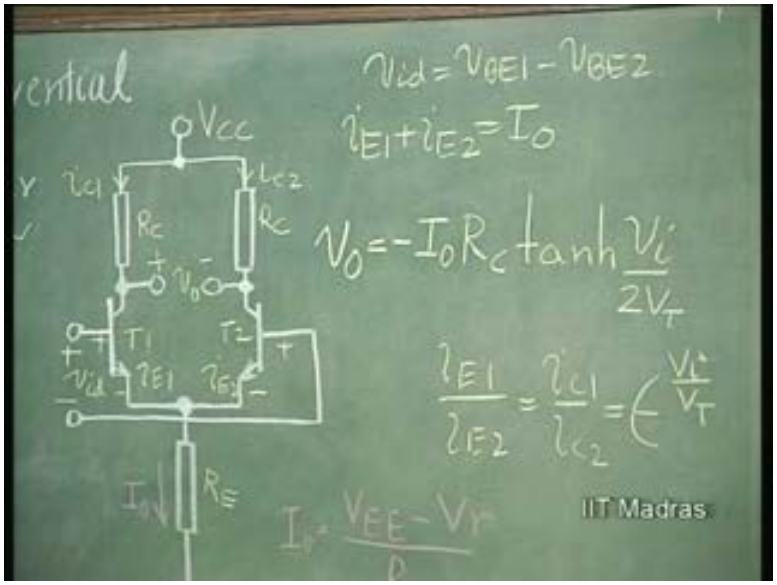

And then we saw that i E 1 by i E 2 ratio is exponent V i by V T, from which we derived V naught as equal to minus I naught R C tan hyperbolic V i by 2 V T, I naught being equal to V E E minus V Gamma by R E. Then we said we will plot this; and this plot tells us that for V i negative, output is going to be positive; V i negative... This is going to be minus 1 and there is minus 1 here; so, it is positive I naught R C.

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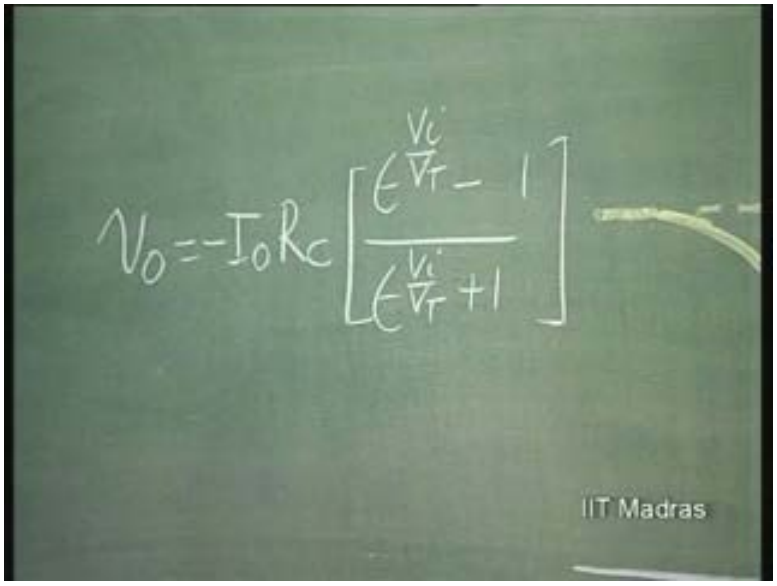

V i large positive; this one will become negligible; and this will go to 1. So, this actually switches between plus 1 and minus 1. This is the characteristic of hyperbolic tan function; and this goes from I naught R C to minus I naught R C; and that is the output swing of a differential amplifier.

Now, let us see how this is equal to minus I naught R C; and if e to power x, you expand it as when x is small; that means for V i by V T, much less than 1. You can say that this is 1 plus x plus x square by factorial 2 and so on... So, you can see that out of this, if you just put it as 1 plus x, ignore the higher order terms; then, this is minus 1 and this is plus 2; because again, compared to 2, V i by V T is negligible.

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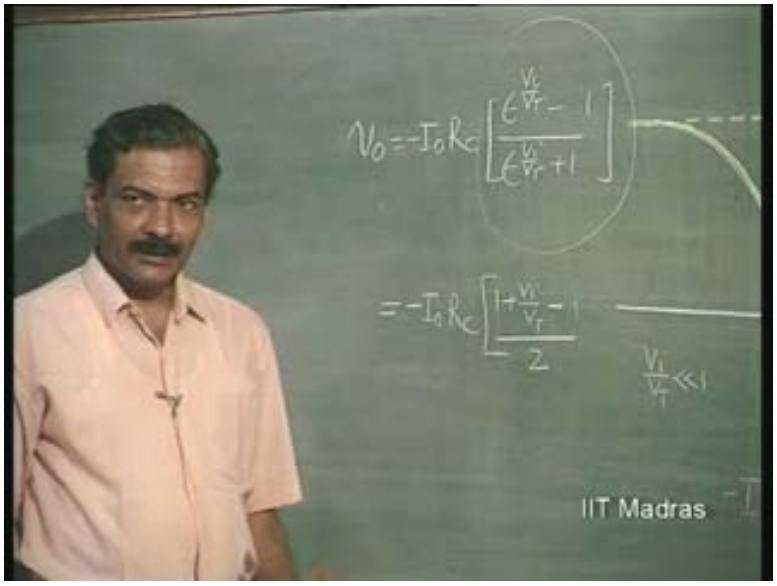

So, even V i by V T is neglected there; whereas here, this one gets cancelled with this one. So, V i by V T becomes dominant factor. So, you cannot neglect it. So, this becomes, minus I naught R C into V i divided by 2 V T which is nothing but...if you look at it, minus g m into R C, because g m is I E Q by V T. I E Q is I naught by 2 for each transistor. So, g m is equal to I E Q by V T. This is I naught by 2 for this differential amplifier.

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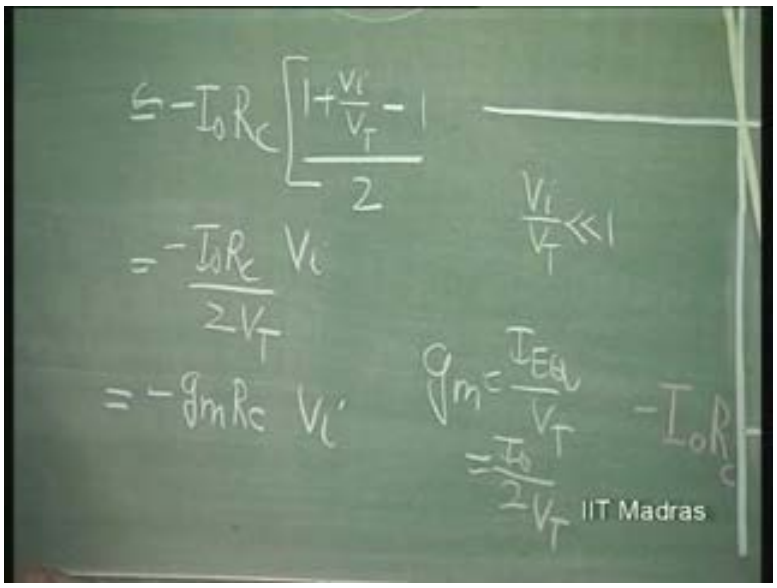

So, we know that this is I naught by 2 V T. That is g m ((the ...Refer Slide Time 5:05)). This is what we had earlier surmised from small signal equivalent. That means small signal here means V i is again, much less than V T. So, V i is much less than V T; same thing that we had used earlier for common emitter amplifier. So now, this defines what is meant by small signal in the case of differential amplifier.

Now, what is a hyperbolic tan function, really speaking? Hyperbolic tan V i by 2 V T can also be expanded as what? Can you from this, conclude what it is? Hyperbolic sine function by hyperbolic cos function. So, if that is the case, what is hyperbolic tan function, strictly speaking? It is true that we will have minus I naught R C into V i by V T as one term, first term; V i by 2 V T. So, V i by 2 V T means tan hyperbolic x, is x; Then, what else?

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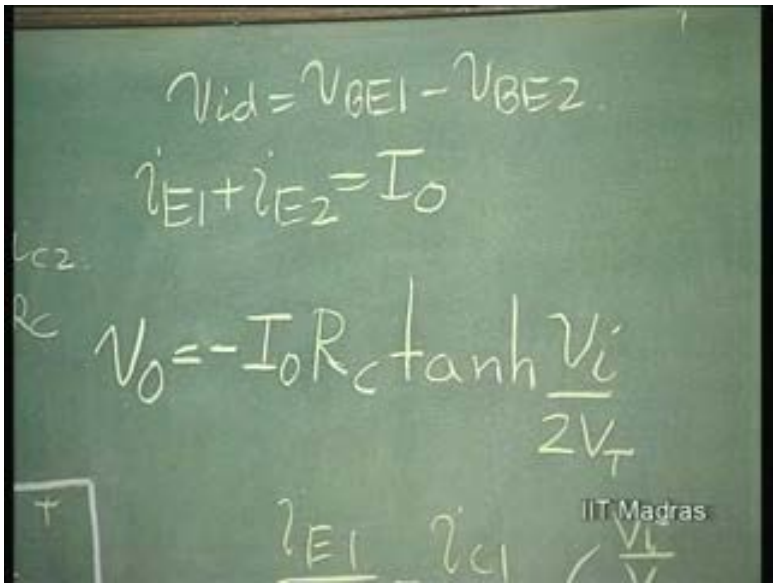

The next term is not squared but cubic. In the hyperbolic tan function, you will not have the square function coming into picture. Why? This is because they get cancelled with one another.

These square functions, V i by V T whole square and V i by V T to the power 4, all these things; and then you get cubic and fifth order, like that; it is an odd function. So, you will see that, as far as the differential amplifier is concerned, the nonlinearities will be less than the nonlinearities in common emitter amplifier, where you have what? What kind of nonlinearity? - exponential nonlinearity. That means e to power x is: 1 plus x plus x square by 2 factorial, so on... So, all the terms are existing. So, after x, you have x square by factorial 2.

Here, after x, you have x cube by factorial 3; and therefore, obviously, the extent of distortion here is much less than that in the common emitter; and it will give the same small signal gain, input impedance, etcetera, but distortion is less. Is it clear?

Now, we will illustrate it later by an example. However, here we can see that tan hyperbolic nonlinearity results in only what kind of harmonics at the output? Only odd

harmonics existing at the output, if I apply a sine wave; whereas, in the case of a common emitter amplifier, all harmonics are invariably present. That can be seen. How is it obvious for us here? Now for...if it is fundamental that is applied, you have for the fundamental, a phase shift of 180 degree here; and no phase shift between this and this.

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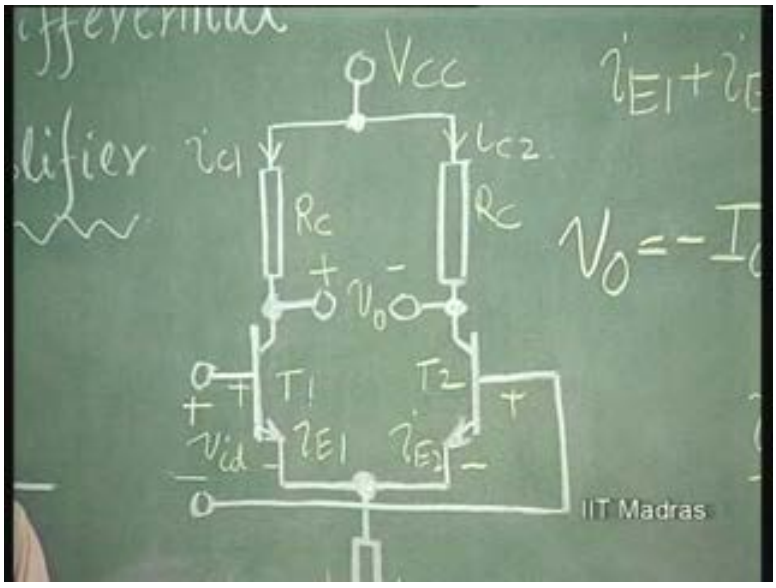

And for the, let us say, since it is a function where the square law gets eliminated, because of the difference, the...how it happens is, because of the difference, there is no phase shift between the even functions and they get cancelled with one another; and only the odd functions remain.

Now, that is illustrated very clearly by this hyperbolic tan non-linearity. Now, this slope here - this is nothing but Delta V naught by Delta V i,...

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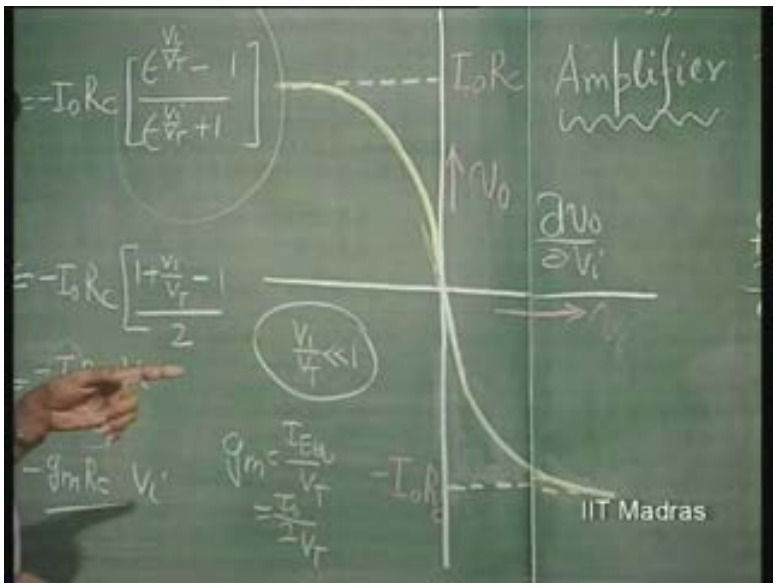

... is nothing but this.

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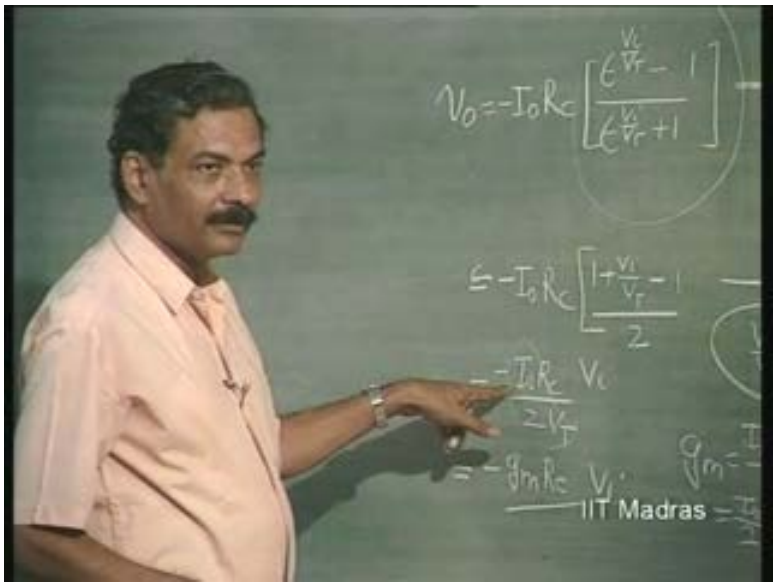

It is going to be...if you do that, please do the differentiation of this from...using the hyperbolic tan function and show that Delta V naught by Delta V i is nothing but the gain; is the same as minus I naught R C by 2 V T into V i.

It is the slope; that we have illustrated here by making approximation. You can do that mathematically by finding Delta V naught by Delta V i, Delta V naught by Delta V i as minus I naught R C by 2 V T, from this.

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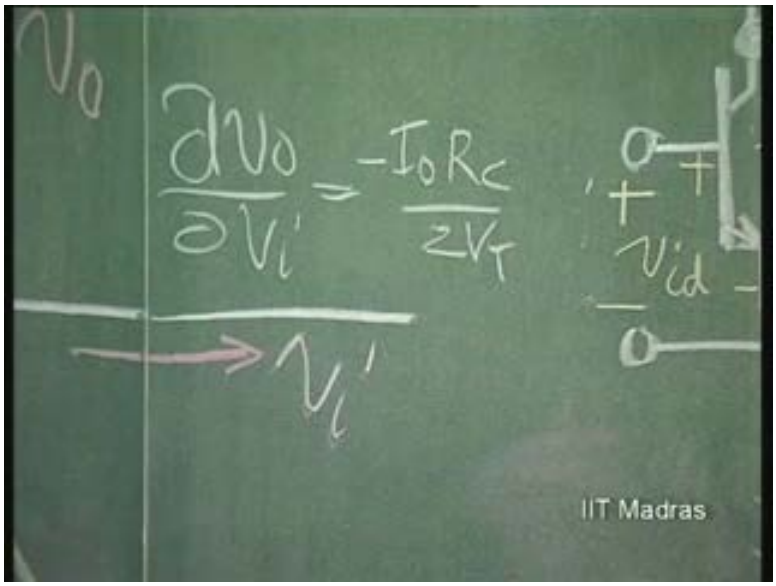

Now, the negative sign is also indicated by the negative slope here; and the slope will keep on decreasing. That means, if there is an offset in this differential amplifier, the gain is going to be less. Small signal is going to be... small signal gain is going to be less; and not only that, this swing also is going to be less, if there is an offset, if the operating point is not this.

What is an offset? Even when V i d is zero, this voltage is not zero. Why is it going to happen? Simply because, these two transistors are not so matched. I E naught of this transistor is not same as I E naught of this transistor; in which case, even when this is zero, then these two currents will be what? – different, even though the base to emitter voltages are the same.

So, the output will be having an offset. Now, I would like you to understand something about the offset now. What is the offset? Offset, output offset is that voltage that appears when the input is zero.

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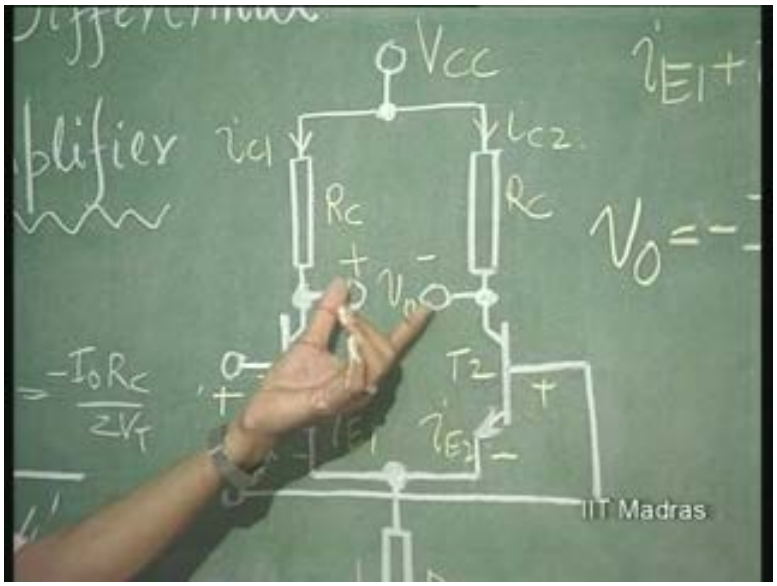

Output offset is that voltage that appears at the output when the input is zero. So, we have what is called output offset. Why does it happen that there is an offset? That is because the transistors may not be, that is, I E naught... Transistor 1, T 1, is having I E naught 1 and transistor T 2 is having I E naught 2 as its reverse saturation current. Then, what will be i E 1? i E naught 1 exponent V B E 1 by V T. i E 2 is equal to I E naught 2 exponent V B E 2 by V T.

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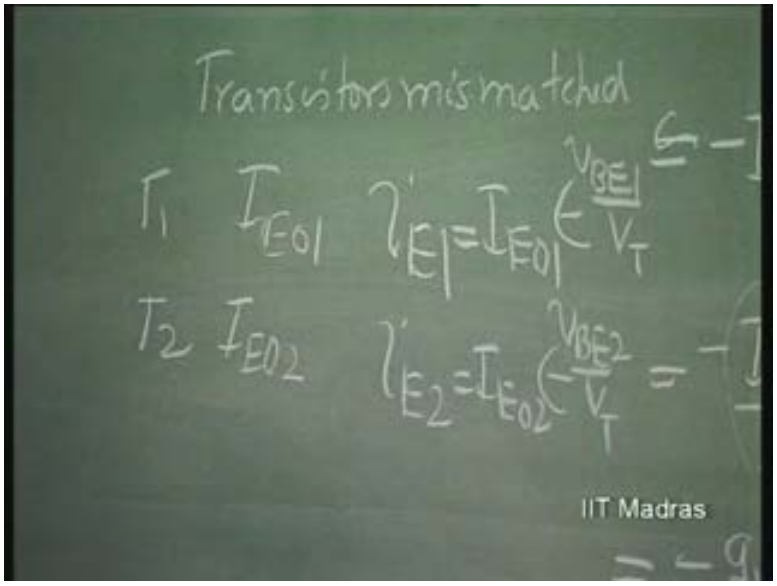

So, what will be the ratio of the currents when the input is zero? If V i d is equal to zero, then V B E 1 is equal to V B E 2. Is this clear? If V i d is zero, V B E 1 is equal to V B E 2. If this is a shorted, this voltage is always same as this voltage.

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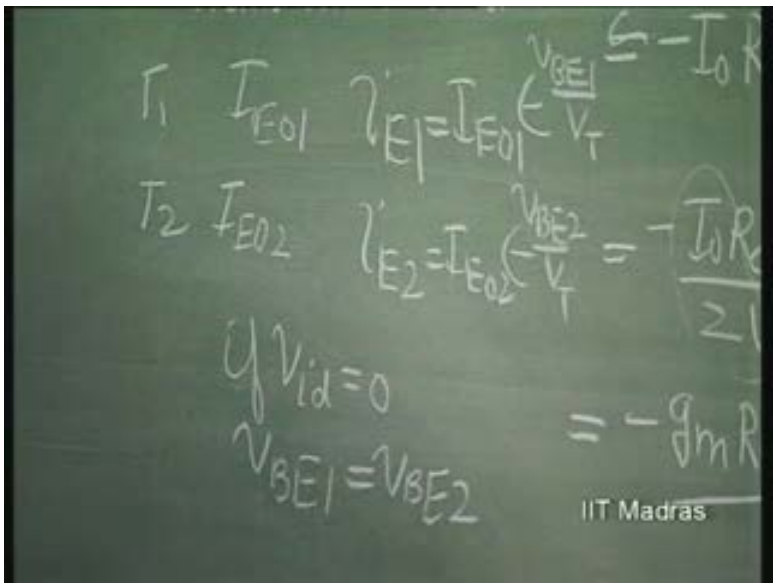

Then, V B E 1 is same as V B E 2. Therefore, i E 1 by i E 2 is not equal to 1. You take the ratio. It is I E naught 1 by I E naught 2.

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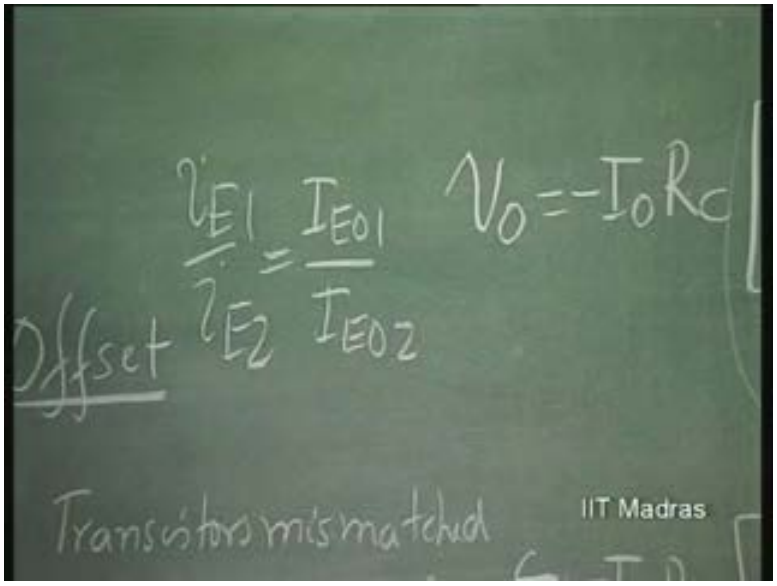

Is this clear? It is understood or not? And i E 1 minus i E 2 by i E 1 plus i E 2 equals this ratio; I E naught 1 minus I E naught 2 by I E naught 1 plus I E naught 2.

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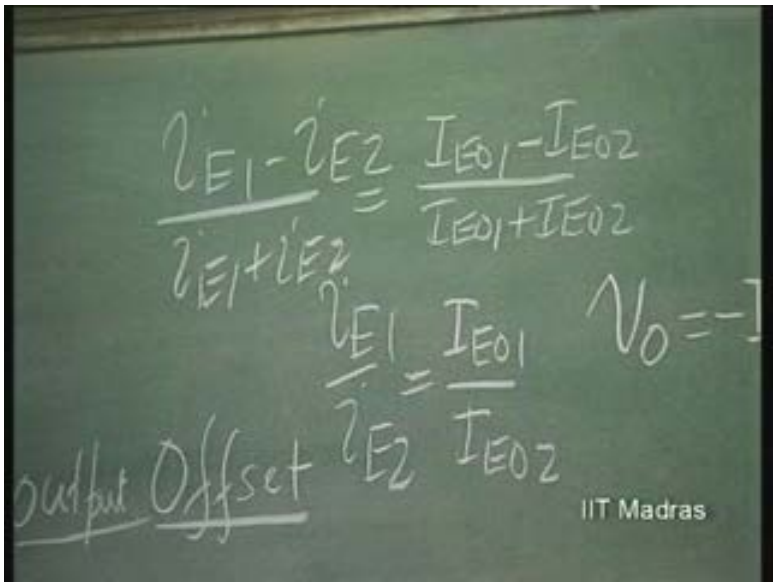

What is this? I E 1 plus I E 2. That is always equal to I naught and I E 1 minus I E 2 is equal to i c 1 minus i c 2 by Alpha. i c 1 minus i c 2 by Alpha.

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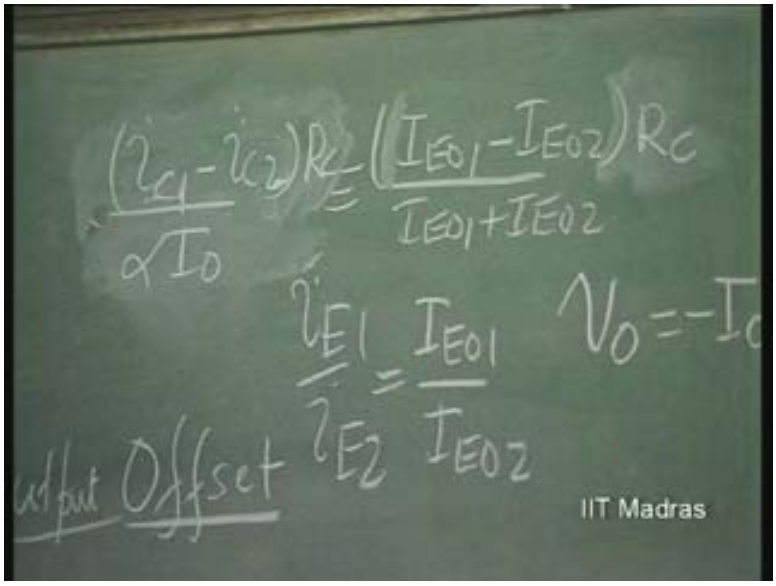

i c 1 minus i c 2 into R C is equal to minus V naught; that we had already written earlier. i c 1 minus i c 2 into R C is equal to minus V naught and therefore V naught...now this offset, this is what is called the offset voltage, output offset voltage; equal to minus Alpha I naught R C into I E naught 1 minus I E naught 2 by I E naught 1 plus I E naught 2.

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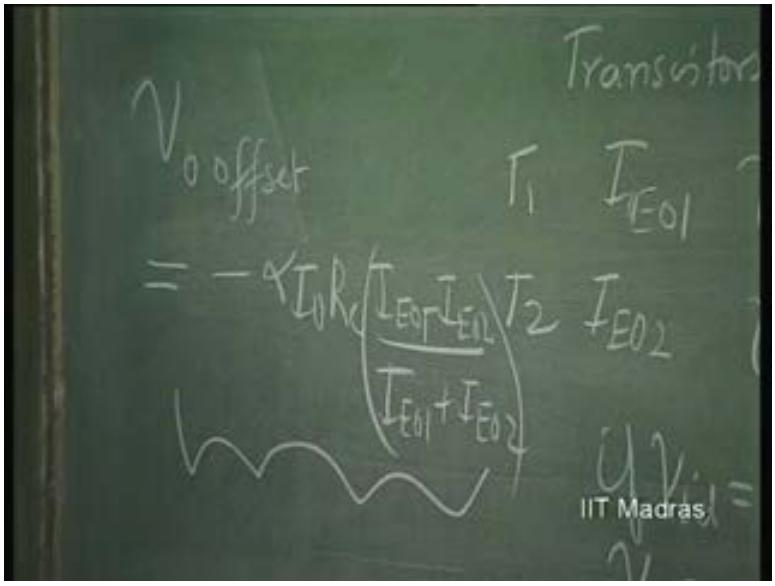

So, if you know the extent of mismatch of I E naughts; I E naught 1 minus I E naught 2 is the mismatch; I E naught 1 plus I E naught 2; then, you know the output offset as minus Alpha I naught R C into this mismatch factor. So, this is an important aspect of output offset. So, if there is a mismatch you can tell based on the extent of mismatch what the output offset is going to be; and our effort should be to make I E naught 1 as close to I E naught 2 as possible so that this V naught offset is always close to zero.

So, if it is close to zero, fine. We get the maximum gain which we intend to have; but otherwise, the gain will keep decreasing depending upon the offset. Therefore, the offset itself is not a serious problem. It can be compensated. It is a constant voltage. If it is a constant voltage, it does not vary with time; then it is not a problem.

Unfortunately, it is a D C which drifts with time. This is what I have told you. So, it keeps changing with respect to time because of dependence of I E naught 1 and I E naught 2 with respect to temperature; and they may not track exactly. And therefore, this fact that these vary with respect to temperature causes the output voltage to drip with respect to time.

So, even when the input signal is not there, it is indicating an output signal which is time dependent. This is adding to the noise; this itself is now generating some amount of noise. Particularly, this is of great nuisance in the case of low frequency amplifier where the signal also changes very slowly with respect to time. We cannot separate out this from the signal.

So, it interferes with the signal. Therefore, in a good amplifier, we must make this as close to zero as possible. Not only that, then it should not further drift with respect to time. These are two important things. Now that we know the origin of this offset, with...it will be clear for us how to compensate for this offset also, so that, if that it is not zero, how to make it equal to zero.

Now therefore, input offset definition is... This is output offset. Is this clear? When the input is zero, what the output is? This is called output offset. Input offset, we will now talk about. Input offset is that voltage that has to be applied to the input in order to make the output go to zero, input offset. These are all important parameters associated with the differential amplifier. The input offset is that voltage that we have to apply at the input in order to make output offset, output voltage go to zero. Is the definition clear?

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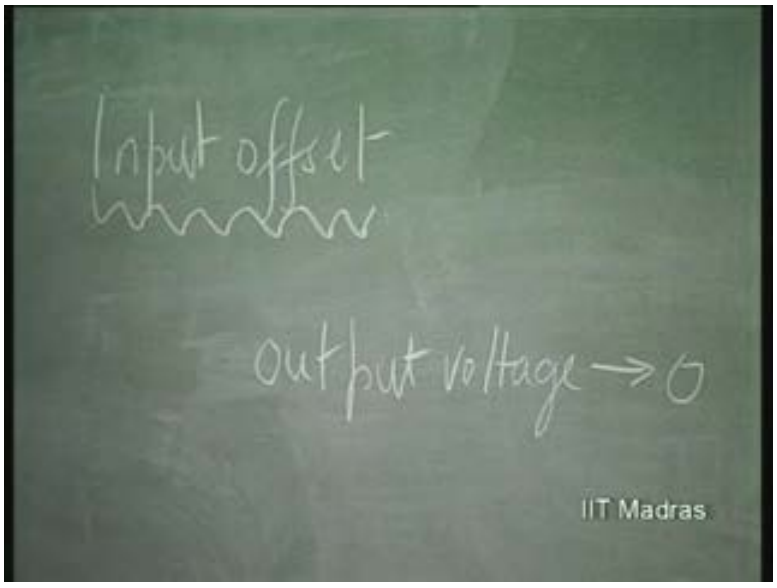

Now, how do we find out input offset? It is very clear. Input offset is that V i d that I have to apply so that exponent V i d by V T, this becomes equal to what? - this becomes equal to... What is this normally? i E 1 by i E 2 equals i c 1 by i c 2; that is what we have put.

In order to make the output offset zero, I have to have I E 1 equal to I E 2; i c 1 equal to i c 2; that means this should go to 1. So, that means V i d for that...this should go to 1.

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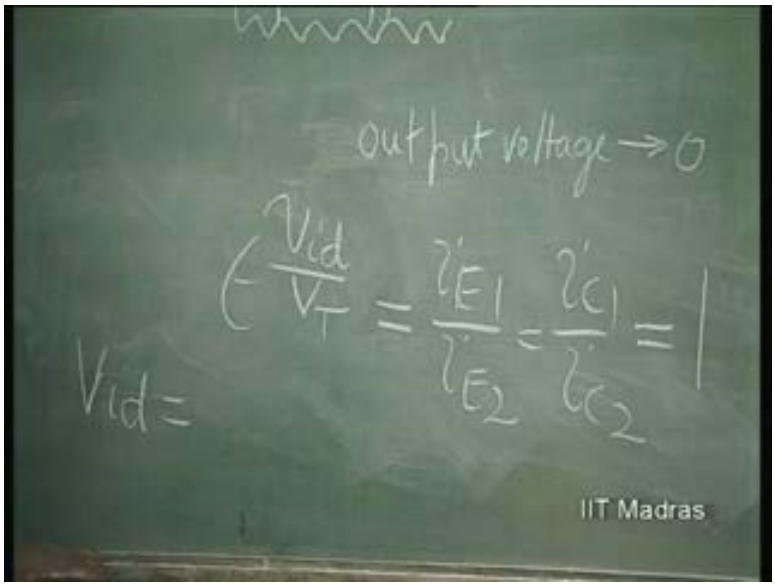

So what is that? This is equal to I E 1 is I E naught 1 into exponent, what? – V i, V B E 1 by V T; and this is I E naught 2 exponent V B E 2 by V T. Is this clear?

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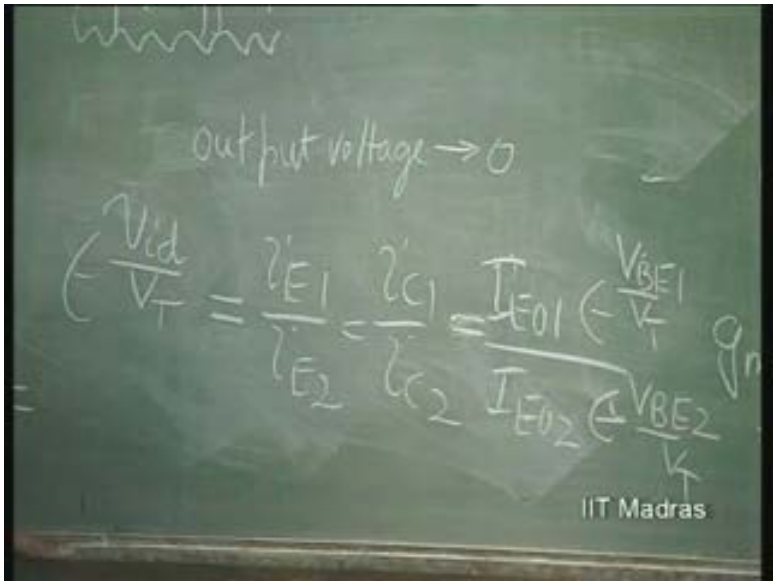

Strictly speaking, when I E naughts were matched, this was going to, what? – one, this was becoming equal to exponent V i d by V T. Is this clear or not? This was equal to I E 1 by I E 2.

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I E 1 or I E naught 1 exponent V B E 1 by V T; I E 2 is equal to I E naught 2 exponent V B E 2 by V T; I E naught 1, when it was equal to I E naught 2, this was going to exponent

V i d by V T. And, this should then become equal to 1. So, in this case, this is 1, when I E naught 1 is not equal to I E naught 2.

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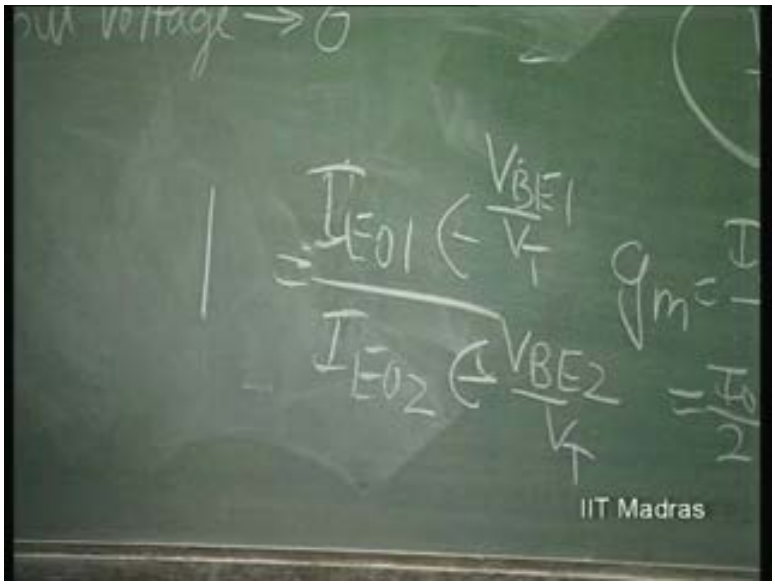

If I E naught 1 is equal to I E naught 2, then we will get exponent V i d by V T equal to 1 or V i d equal to zero. That is the input offset. If I E naught 1 is not equal to I E naught 2, then, even when I E 1 by I E 2 is equal to 1, exponent V i d by V T is equal to I E naught 2 by I E naught 1.

Earlier, it was equal to 1. And therefore V i d was equal to zero. Now obviously, V i d is equal to the offset voltage. So, this is equal to V T log i E naught 1 by i E naught 2. So, this is an important thing.

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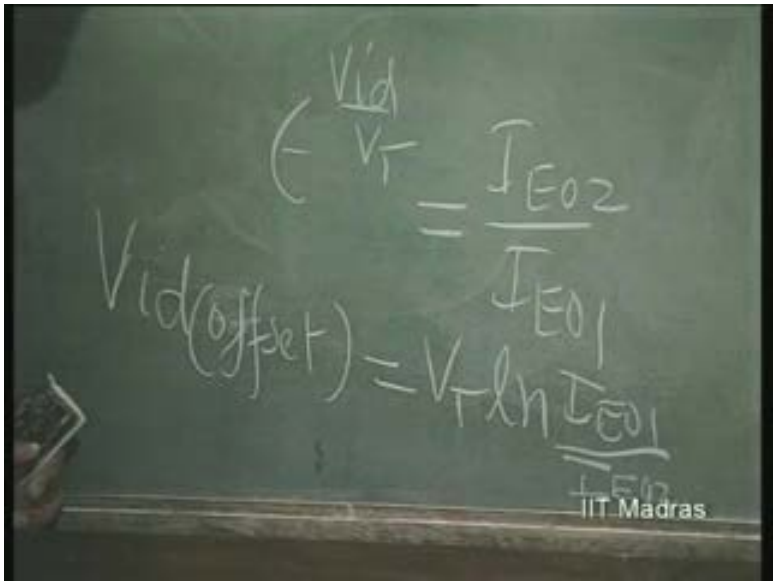

Input offset is equal to V T log I E naught 1 by I E naught 2. So, it may be positive or negative depending upon whether I E naught 1 is greater than I E naught 2 or I E naught 1 is less than I E naught 2.

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The order of this is typically about a few millivolts, say 1 to 2 millivolts typically; because this is about 25 millivolts; and I E naught 1 by Ii E naught 2 is practically close

to 1. That means log of 1 is pretty close to zero, I E naught 2. So, the offset voltage is minus V T log. That only changes the sign.

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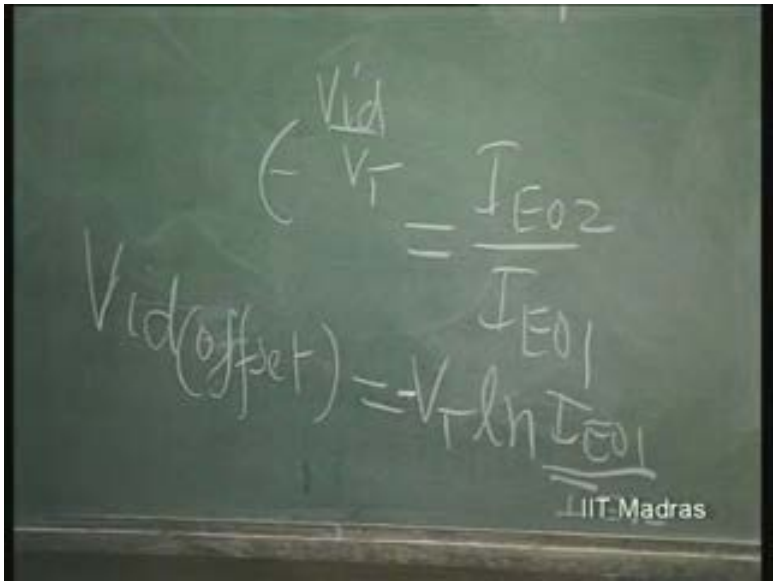

So, the sign can be positive or negative; that is of no consequence, depending upon whether i E naught 1 is greater than i E naught 2 or i E naught 1 is less than i E naught 2, because we have not said which is really the input offset. So, it can be plus minus V T log i E naught 1 by i E naught 2. So, typical value for BJT is, this input offset is, 1 to 2 millivolts. Therefore, you must always know this; that a single stage circuit like this with one pair of transistors will result in something like an offset of 1 to 2 millivolts.

If you put Darlington pair here... Darlington pair means, actually, to connect a transistor like this and another transistor like this, in order to artificially boost up the Beta of the transistor.

Now, there are two pairs coming into picture. The uncertainty will be doubled. So, it will be 2 to 4 millivolts. So, using more pairs of transistors will result in more input offset even though you might put this, in order to improve the beta of the transistor. You will degrade the transistor differential amplifier in terms of its input offset.

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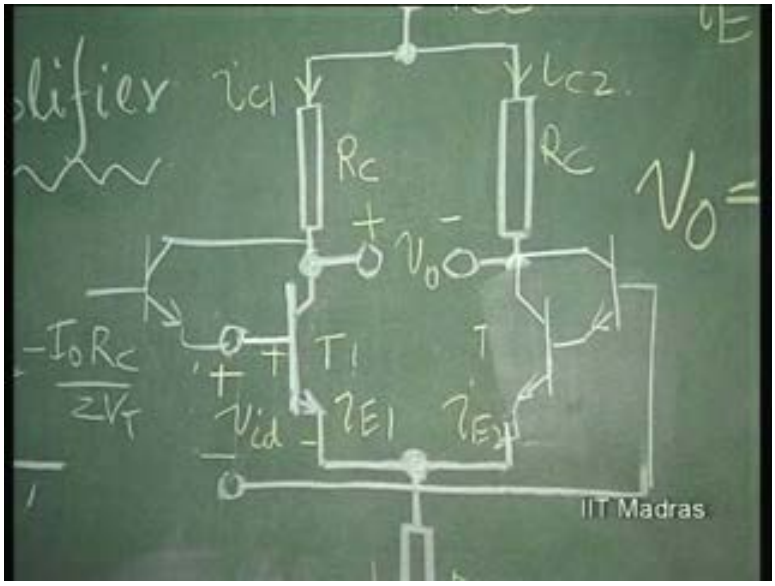

So, the best for lowest input offset is a single pair; not these modifications. Never modify this. The best thing is just a single pair, if you are interested in maintaining minimum offset.

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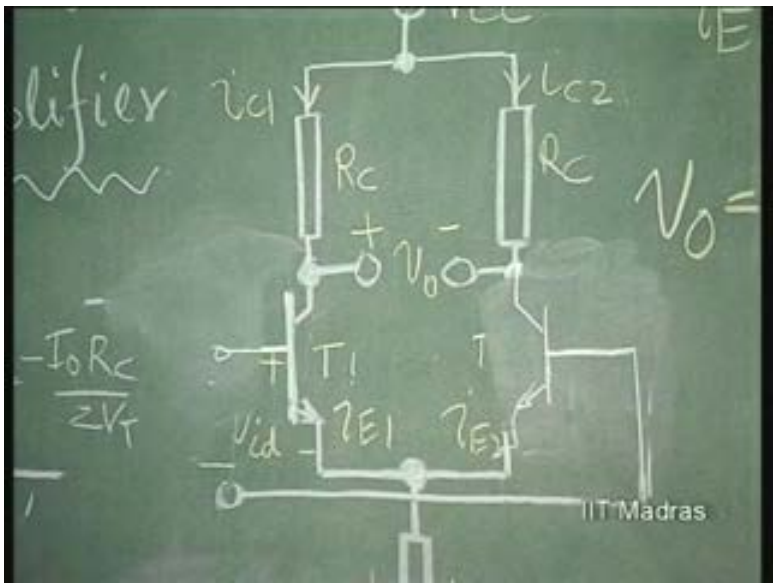

Such is the case with amplifiers, particularly usable for very low frequency, where this offset has to be kept at a low value in order to prevent the output from drifting.

We have seen that the current ratio i E 1 by i E 2 is same as i c 1 by i c 2; is equal to exponent V i d by V T, if the two transistors are matched. Otherwise, of course, it is going to be I E naught 1 by I E naught 2 into exponent V i d by V T and from which we could get the input offset, etcetera.

Now, let us discuss once again about how this V i d can swing this current; portion of this current is going to flow through this. Initially, this will be I naught by 2; this will be I naught by 2, when V i d is zero, if the two transistors are matched.

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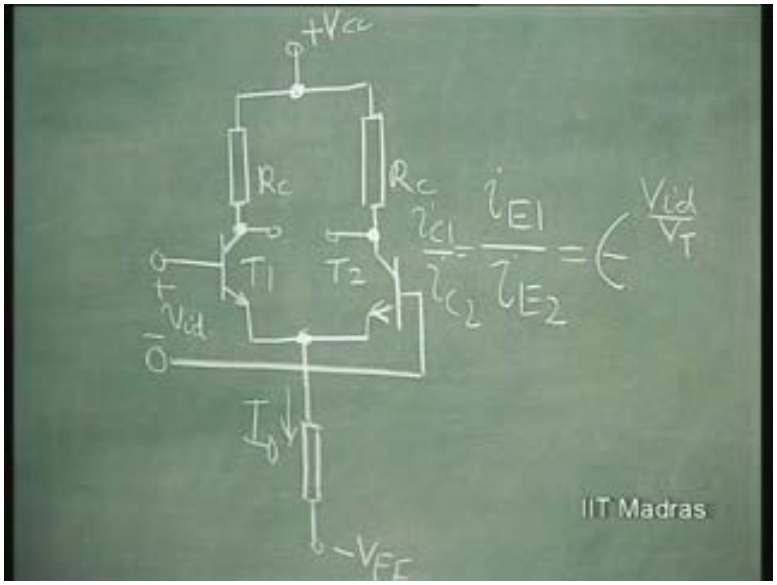

Now, let us apply V i d. The current ratio is going to be varying according to this. If V i d is zero, this will be 1; and I E 1 is equal to I E 2 equal to I naught by 2. Now, by therefore applying V i d, I can make the current I E 1 much greater than I E 2, this current will...can keep on increasing; this current will keep on decreasing. Ultimately, what happens?

This transistor will have the total current I naught and this will have zero. That is the limit. This is off. T 2 is off. T 1 is fully drawing the current. At that point of time, this voltage is going to be V C C minus I naught R C. This will be V C C, because there is no

current here. Therefore, this output voltage will be V C C minus I naught R C minus V C C and therefore it is minus I naught R C. When V i d is a large positive, output voltage will go towards minus I naught R C.

Then, I make V i d now negative. This current will increase; this current will decrease as determined by this ratio. And this will keep on increasing, if I make it more and more negative; and ultimately T 1 will go to off state and T 2 will take the complete current and this voltage will be V C C minus I naught R C and this will be V C C and V naught will be I naught R C.

This is called current switching. What has taken place now by applying a V i d of positive polarity and going to negative polarity, as far as V i d is concerned; the current here has totally switched from this transistor to this transistor. This is called current switching and any logic circuit using this for driving the transistors of this logic circuit is called current mode logic circuit.

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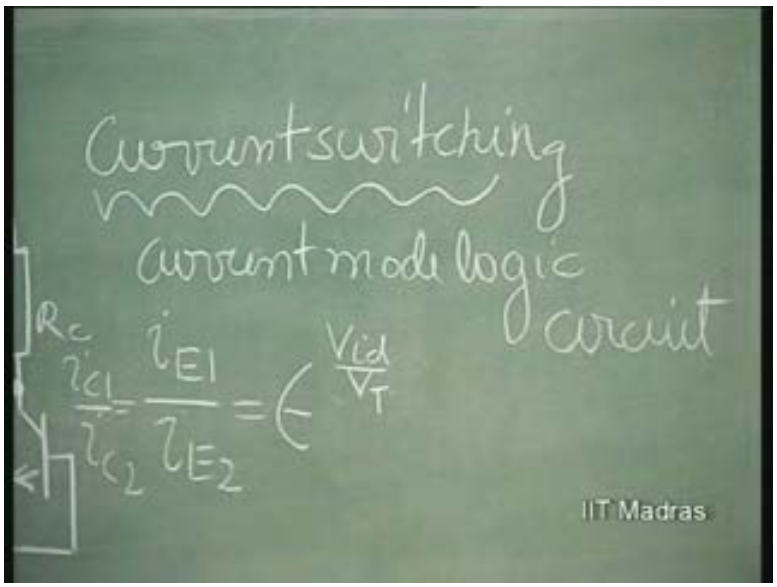

So, a differential amplifier is belonging to a family of logic circuits called current mode logic circuit; or, it is in this particular case popularly called emitter coupled. Emitter is coupling this transistor. It is coupled at the emitters to a common point. So, this is called Emitter Coupled Logic or popularly, E C L; or, Current Mode Logic, E C L or C M L, current mode logic.

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This by nature, because only the current is switched from this to this; by nature, is the fastest known logic family resulting in... Any computer designed using this logic family will be the fastest computer run. As far as transistors are concerned, any computer using such logic family is going to be the fastest logic family computer; and therefore fastest computer.

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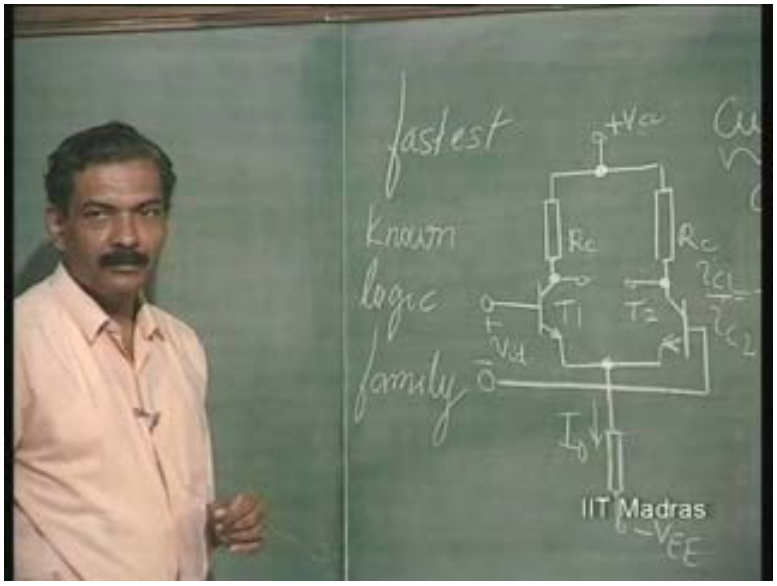

Why is it fastest compared to other logic families? When the current is completely switched to this, the potential here is V C C minus I naught R C. At that point of time, T 1 should not go to saturation. That means there should be enough collector to base potential, which is positive in this case, in order to retain T 1 in active region. This is an important aspect.

If...when this current is completely switched over to this, this transistor goes to saturation. Everything is lost. It has to come out of saturation before it can really respond to the input signal that is causing a certain amount of delay. All your T T L circuits got into the problem of low speed only because they were going into saturation. Then came about what is called Schottky T T L where V C B was forced to be retained close to zero, preventing such transistors from going to saturation.

They were faster than the ordinary T T L. However E C L, by nature, is the fastest without the requirement of introducing Schottky barrier transistor junction diodes; so, between collector and base... So, this is the fastest logic family here. We have the current switching taking place and the logic level in this particular case is going from V C C.

You consider one side; V C C to V C C minus I naught R C. On the other side also, V C C minus I naught R C to V C C.

Or, if you take the differential, it will go from I naught, minus I naught R C, to plus I naught R C. However, if you connect an identical differential amplifier as its output, this is again connected. Normally, that is the state of most of the logic circuit. This logic circuit will be further connected to another logic circuit; so, the extent of voltage variation will get limited, just like this happening at the input.

At the input, we need only a change in voltage of the order of few tens of millivolts to switch the current from one transistor to other. Let us investigate this. How much voltage is needed at the input in order to switch the current totally from one transistor to other? This is an important aspect of finding out the drive requirement for such logic families.

So, the question is what is the V i d required to take the current from one transistor to the other and vice versa? Now, if you see the relationship, it is exponential. That means, when V i d is plus infinity, and V i d is equal to minus infinity only, this takes place. But in all such situations, we say that the current is completely switched over to this transistor, when this transistor gets 90 percent of the total current; this transistor has 10 percent of the total current. Is it clear?

This is always the case in making a measure of what kind of voltage you require for such drive. So, I want this transistor to get 90 percent; this transistor to get 10 percent. That will be 1 voltage; the other voltage will be... When this is 10 percent and that is 90 percent.

Let us therefore call V i d 1 as that voltage where exponent V i d 1 by V T is equal to... I E 1 is 90 percent and I E 2 is 10 percent of I naught. Is this clear? This is 1; then exponent V i d by 2 V T corresponds to this 10 and this 90.

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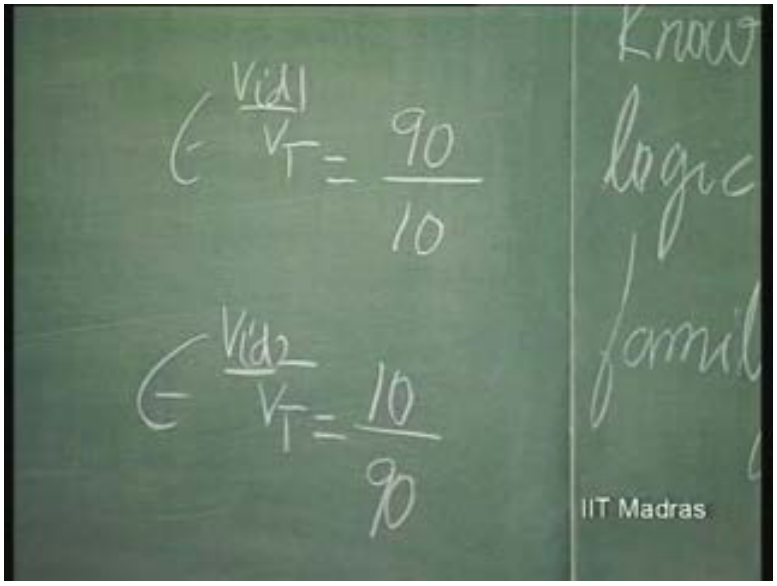

And, what do we need? We need V i d 1 minus V i d 2. What is the extent of variation in this, which will cause this switching from one transistor to other and vice versa? So, you divide this one by other; you get exponent V i d 1 minus V i d 2 by V T equal to... How much is it? This is 9 and this is 1 by 9. Dividing one by the other, we will get it as 81, clear?

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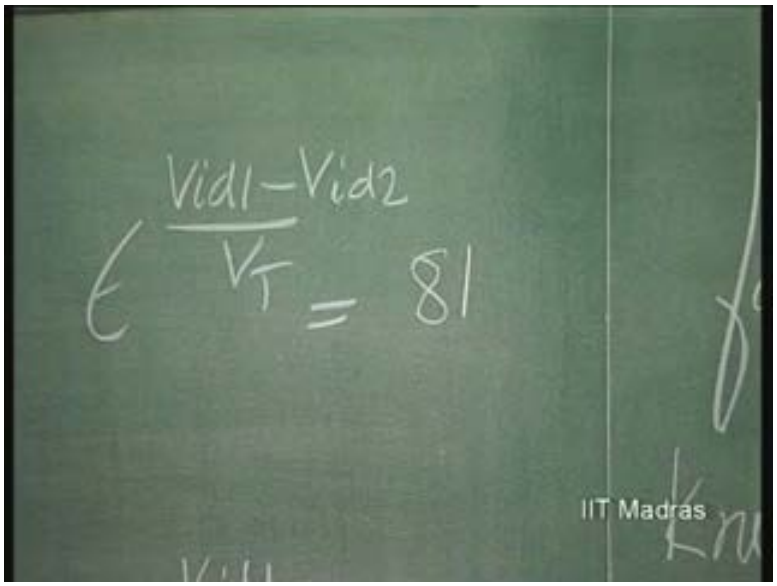

And therefore, V i d 1 minus V i d 2 is equal to V T log, natural log of 81. V T, please remember, natural log of 81. So, that comes out to be, how much? 114 millivolts. This is an important conclusion. The voltage swing that is required to switch the transistor from one to the other and vice versa is only about 114 volts, millivolts.

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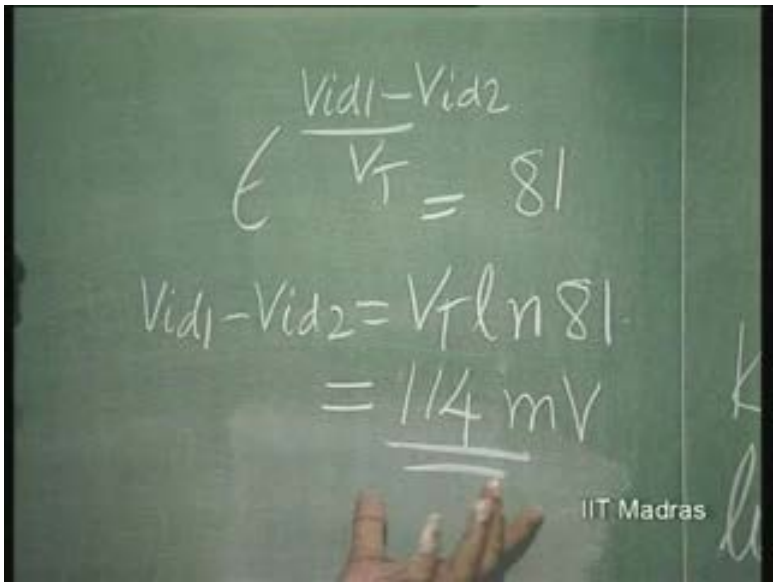

Please remember this always; and how it can be derived. So, the...in the case of emitter coupled logic, you will see that the logic level, for zero to logic level to 1, should only swing from one value to other by an extent of 114 millivolts. Unlike in the case of T T L, etcetera, where the swing is about 5 volts, this is the kind of thing.

Next problem. We will come back to our analog circuitry now. We would like to know what is meant by distortion; what should be the small signal; what is the quantitative measure of the small signal in order to maintain distortion at a certain level. This, we did in the case of BJT tran... common emitter configuration as well. What will ... should be the magnitude of V i d, if it is a sinusoid that I should apply here in order to retain distortion at the output lower than a specific value; and this will also facilitate comparing this with that of common emitter amplifier.

So, we have seen that this V naught is equal to I naught R C. That is, minus, tan hyperbolic V i d by 2 V T. Now, we are taking V i d as equal to... What is it? V p sine omega t. I am applying a sine wave as the input. So, as far as the x factor is concerned, we know that this is straight away coming as V i d by 2 V T.

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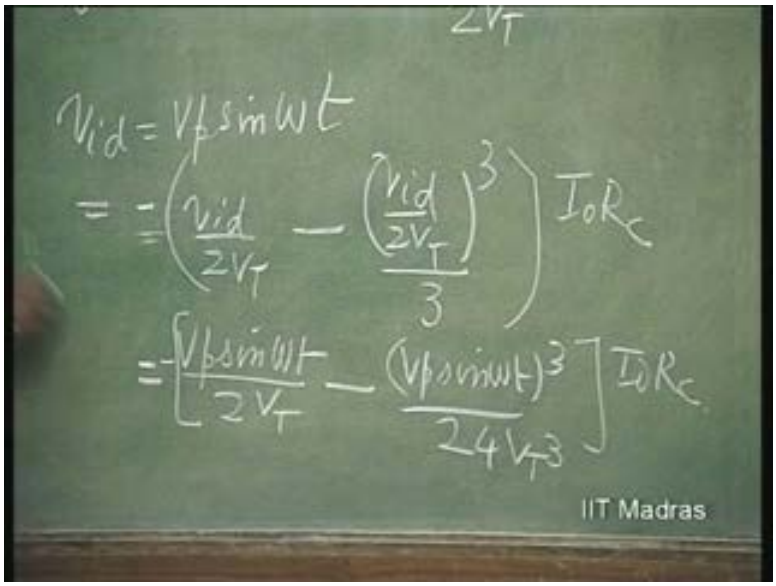

This tan hyperbolic V i d by 2 V T can expand as...this, if it is x, it is x minus x cube by 3. That means V i d by 2 V T minus x cube, V i d by 2 V T whole cube by 3 and so on... The other factors are going to be ignored. So, if we now consider V p sine omega t as V i d equals V p sine omega t, this whole thing into I naught R C with a minus sign is the output. If V i d is V p sine omega t, this is going to be minus V p sine omega t divided by 2 V T minus V p sine omega t whole cube. That is V i d. This will be 8 V T cube. Therefore, this will be 24 V T cube. This into I naught R C.

Now, as far as the gain is concerned, we can see that I naught R C divided by 2 V T... So, output will be corresponding to V p sine omega t into I naught R C divided by 2 V T, with a minus sign. What does it indicate? This is the gain; this was the original signal and there is an inversion; there is a phase inversion. This is nothing but...this whole thing is nothing but g m of the differential amplifier; g m into R C. Each transistor is operating at

I naught by 2; and therefore, that I divided by V T is the g m. Thus, g m into R C. So, this is g m into R C; minus g m into R C into V p sine omega t. This is actually the wanted input.

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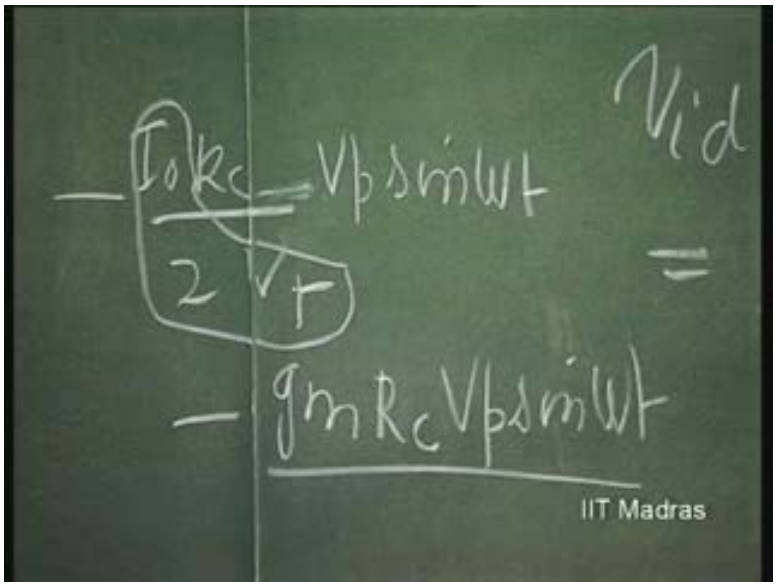

This factor is going to cause certain amount of distortion in the signal, because apart from sine omega t component, we will have other components also coming into picture. So, this V p sine omega t whole cube could be expanded as...that is equal to V p cube 3 sine omega t minus sine 3 omega t by 4. That is, sine cube omega t.

So, that divided by 24 V T cube is what is going to remain of this. So, this factor, therefore is going to contribute to certain amount of distortion because of the third harmonic. So the third harmonic distortion is going to arise here. Now, let us compare it with the fundamental; the fundamental component was V p by 2 V T, peak value; V p by 2 V T. This is the fundamental component.

As against that, we have this; which is going to be the amplitude of the harmonic; which is going to be, let us say, V p cube by 96 V T cube. So, we have this equal to V p square by V T square into 48. So, this is the ratio of the third harmonic to the fundamental. This

is also going to be the ratio of the... I mean percentage distortion. If you multiply it by 100, this will give you the percentage distortion.

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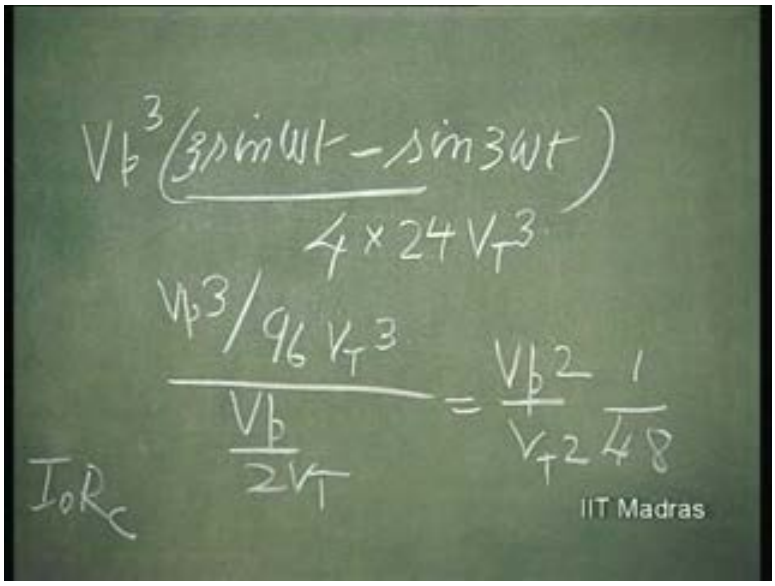

So, this will give you an idea as how to control the percentage distortion in your differential amplifier. This, if it has to be 1 percent, then this factor should be less than point 01. Now, that is how you have to control the differential signal amplitude.

Now, we have another aspect of the amplifier to be taken care of in the differential amplifier. If this is operating at a current of I naught apart from the differential signal, you have a common mode signal which is coming into picture, V c i.

So, if there is no differential signal, only common mode signal is present, how do we now fix up the sort of signal limitation at the input? If this is R C, this is also R C. This is V C C. Then, the current in this will be I naught by 2; I naught by 2. And, since the common mode signal is not going to cause any change in this current...so, this common mode signal, when it is increasing, the reverse bias voltage applied to the transistor will keep decreasing.

So, this can go on up to V C C minus I naught by 2 R C; at this voltage is going to remain almost constant at V C C minus I naught by 2 R C. So, this cannot rise above that; particularly, if such an amplifier is the input stage of an op amp or something like that. If the common mode voltage changes above this, this transistor will lose its active nature and it will come to saturation and the polarity is going to change from negative; that is, feedback is going to change from negative to positive; and that will cause what is called as this instability, signal dependent instability.

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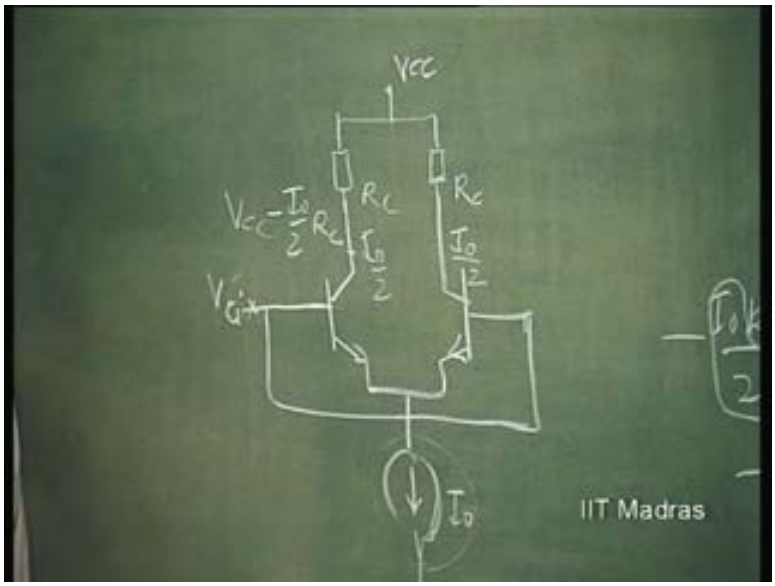

So, this kind of thing can be prevented if you take care to see that this common mode voltage does not exceed this here. On the other side, this voltage can go down and this voltage will follow this. V c minus V Gamma will be the voltage here. And at that time, this current source should remain still active. So, that is the condition. So, there is a limit on V c max as well as V c minimum, as far as the input stage is concerned.