Electronics for Analog Signal Processing - I
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LECTURE - 29
CHARACTERISTICS OF MOSFET

In the last class, we saw that the inverter formulated using MOSFET or junction FET has a characteristic as shown. This is the transfer characteristic. We saw that initially the transistor is OFF when V i is starting from zero.

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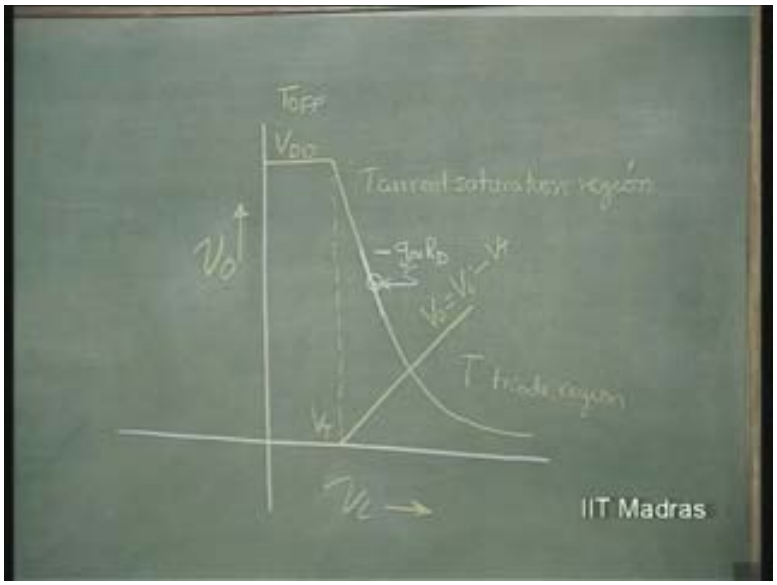

Until V i reaches V T the volt... no current will be flowing through this and therefore this will be at V D D. Thereafter, this is an important point; thereafter, the current starts flowing because V i has exceeded V T. So, the current starts flowing. The question is, in which region this is working. Obviously, when the current starts flowing, the potential here is going to be very nearly V D D. So, V D S is very nearly equal to V D D and V i has just started making this FET go into conduction; and therefore, this FET is in the current saturation region.

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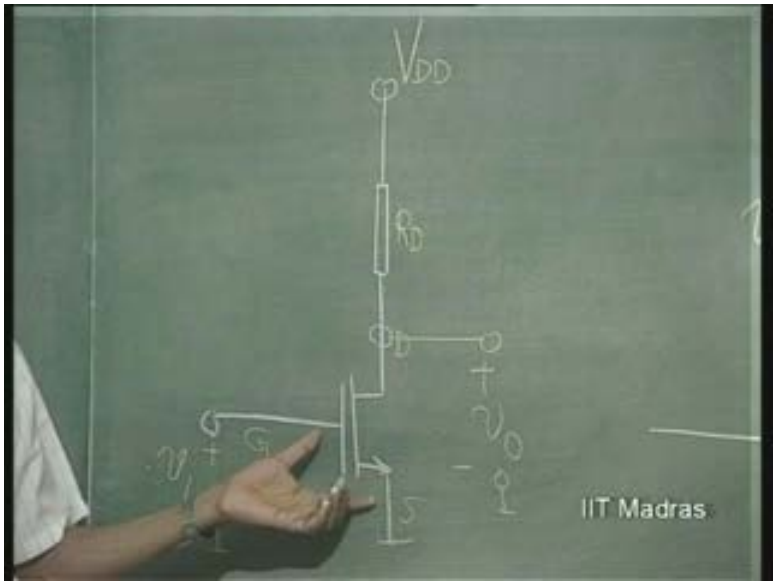

Primarily in the characteristic curve, you will see that this is the current saturation region. When V i is just equal to V T, the point at which current saturation region is reached is V D S equal to V i minus V T itself; which itself is very nearly zero. That means at the origin itself, this would have gone to current saturation. That means when the low current is there, even when there is a very low voltage V D S, it would have reached the current saturation region.

So, this is in the current... this is involved. So first, it starts off with current saturation region. Therefore, the equation to be satisfied is that I D S equal to K times V G S minus V T whole square is valid, and using that information, we could get the slope of this characteristic as minus g m into R D, where g m was equal to 2 K into V G S minus V T, V G S being V G S Q, the quiescent voltage here, which is V G S Q or V i Q.

So, that slope corresponds to g m into R D; it is negative, indicating inversion. That is this small signal gain of the amplifier. This is the common source amplifier; and this g m keeps changing as you go further and further. As the current is lower, the g m is going to be lower, because g m is really 2 K into V G S minus V T; and current is K into V G S minus V T whole square.

So, as current is lower, g m is going to be lower. Same thing happens in the case of a bipolar junction transistor. As current is increased, g m is increased. So this, at this particular point, when V naught or V D S becomes equal to V i, which is V G S minus V T; that is the line separating this current saturation region from triode region. The transistor enters the triode region. The equation to be used is I D S equal to 2 K into V i minus V T into V naught minus V naught square by 2. That is for I D S.

And, this relationship is what? So basically, we are using the equation V naught is equal to V i, that is, V naught is equal to V D D minus i D S into... So, this is the equation that is plotted there, I D S being taken as different depending upon the region.

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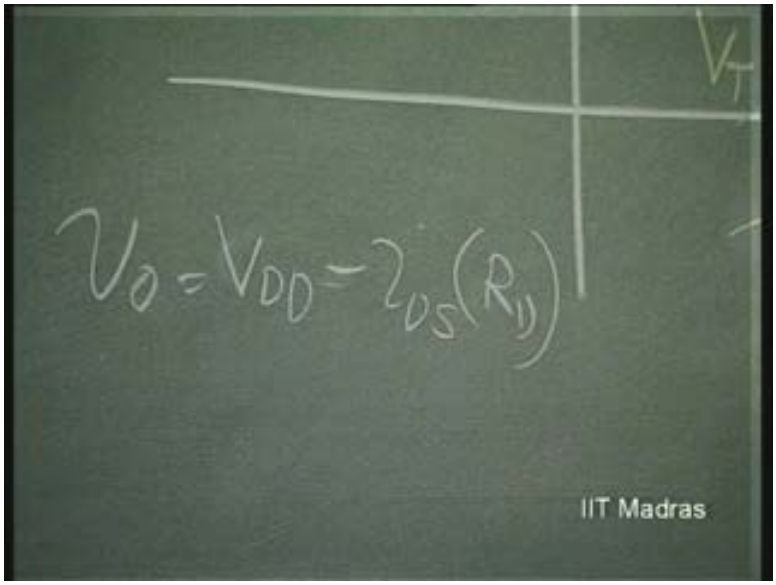

Here it is zero; here it is 2 K into V G S minus V T whole square or V i minus V T whole square. Here, sorry here, it is K into V i minus V T whole square. Here it is 2 K into V i minus V T into V naught minus V naught square by 2. All these things, we had done in the last class.

Now therefore, for small signal; and we have also now understood what is meant by small signal; it causes second harmonic distortion. And, in order to keep the second

harmonic distortion low at a particular value, percentage, compared to the fundamental, we have to use this small signal approximation; and therefore, in this power signal region, the equivalent circuit... this is what we had included. The equivalent circuit is going to be – this is gate, the source is grounded, this is gate; and to this, we are applying let us say, a small signal Delta V i; and current is defined.

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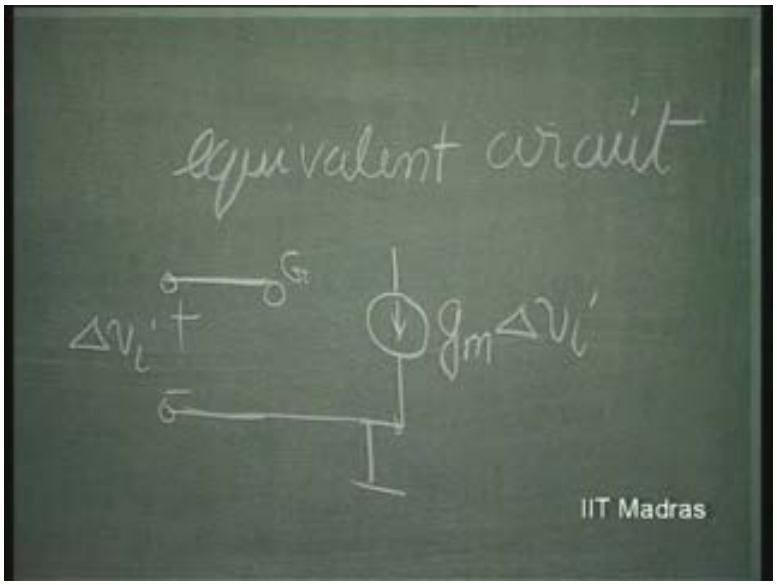

What is g m? g m is defined as Delta i D S by Delta V G S at a particular value of V G S Q. This is the definition of g m. So, if I want the current here, Delta V G S is same as Delta V i, change in V i; because, V G S is same as V i in this case. So, if there is a change in Delta V G S because of change in Delta V i, then we have this current as g m into Delta V i, because g m into Delta V G S, which is Delta V i, is Delta i D S; the change in output current, by definition. So, this is a very simple equivalent circuit.

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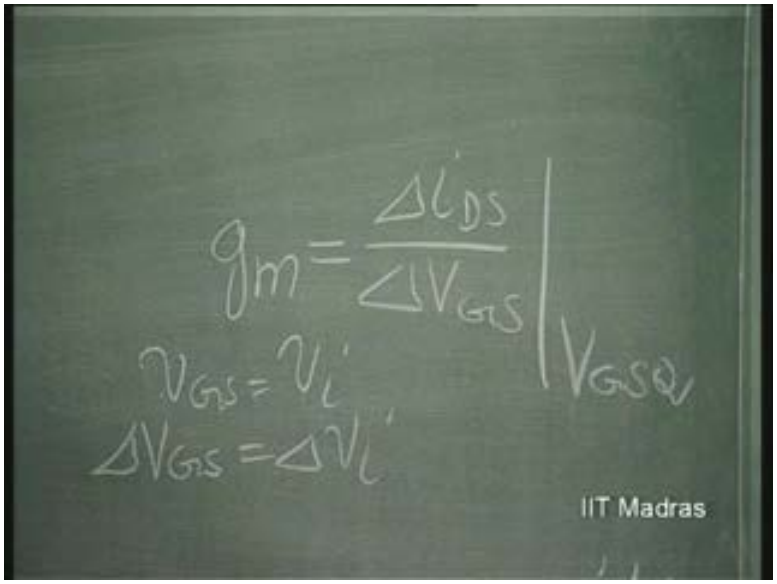

A current source which is inducing a current which is g m times Delta V i; that is occurring at the drain. So, you can see that this is identical to the bipolar equivalent circuit between base and emitter if the voltage was V B E. The current, source current, was g m into Delta V B E which is Delta V i; exactly same. Gate being replaced by base; source by emitter, drain by collector, if you want the bipolar.

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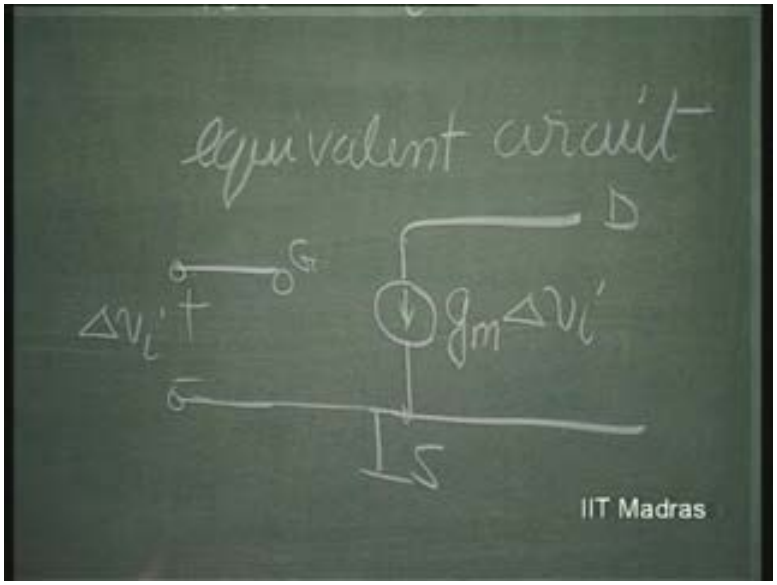

So, as far as equivalent circuit..., the only thing is that at this point, it was very nearly a short circuit. It was current controlled; it was a forward biased junction; whereas here, it is an open circuit. Now, that is the difference. Between base and emitter, even though it was a forward biased junction, we had negligible base current, if Alpha were exactly equal to 1. So, this current was very nearly zero even in the case of base; which really means that, if you take an ideal transistor with Beta infinity or Alpha equal to 1, even this impedance would have been infinite.

But in practice, it is not infinity. It is of the order of few Kilo ohms; whereas, in the case of field effect transistor it is of the order of tens of mega ohms. So, you can keep it as open circuit. At this point, once again, just like the case of a transistor, we have here the channel resistance not being infinity; not an ideal current source. Characteristic is not exactly horizontal; there is a small increase. That we have explained in terms of Lambda, if you remember. In the equation, the current I D S was given as, I D S was given as K into V G S minus V T whole square into 1 plus Lambda times V D S. So, it was dependent upon V D S. It was not all that independent.

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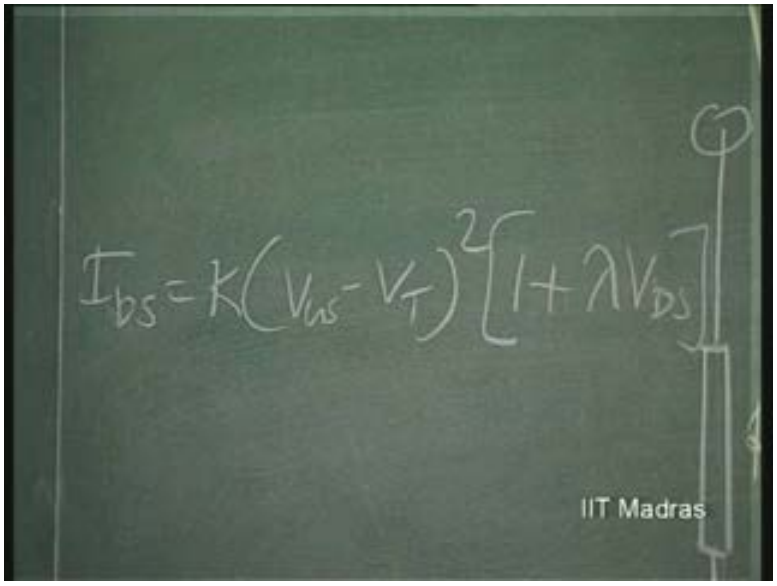

The saturation current, the so called saturation current, was not really remaining constant. It was increasing with respect to V D S and this Lambda factor we brought in. That is therefore responsible to result in what? – an r d s. So, what is r d s? By definition, r d s is defined as Delta V D S by Delta I D S, in the what? – current saturation region. Ideally speaking, this should be infinity; whereas now... or how much is it going to be equal to? This is going to be only dependent... So this is Lambda times K times V G S minus V T square. That is, 1 over that.

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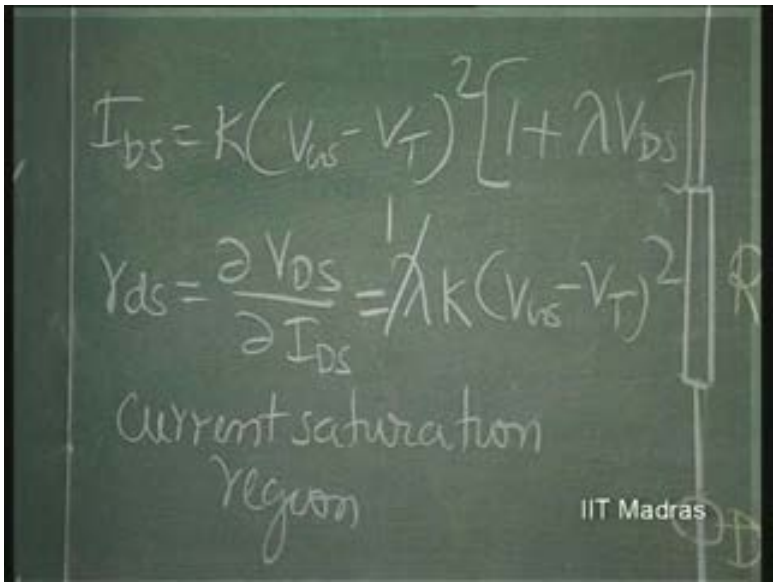

Delta I DS by Delta V D S is Lambda times this. So, Delta V D S by Delta I D S is 1 over Lambda into K into V G S minus V T whole square. So strictly speaking, K into V G S minus V T whole square is really the current, quiescent current, of the transistor; because, you are going to evaluate it at a particular operating point. So, we will put this as V G S, V G S Q. So, K into V G S Q minus V T whole square is really speaking I D S Q. So, you can therefore obtain this as 1 over Lambda times I D S Q.

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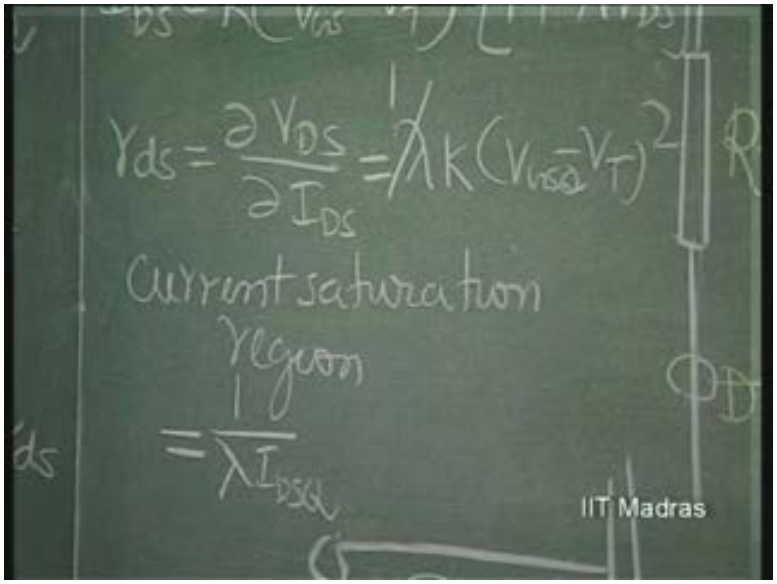

So, this Lambda should be given by the manufacturer; or, you have to make some arrangement to measure it. This also is an important factor associated with a field effect transistor. What is the order of impedance that it results in? It will be of the order of hundreds of Kilo ohms, this R D S. Unlike in the case of common emitter transistor, which is of the order of a few mega ohms, up to 10 mega ohms, this here is going to be of the order of hundreds of Kilo ohms. So, this particular thing is to be normally taken into account in the equivalent circuit; and the composite equivalent circuit now, using all these non-idealities, is simply this.

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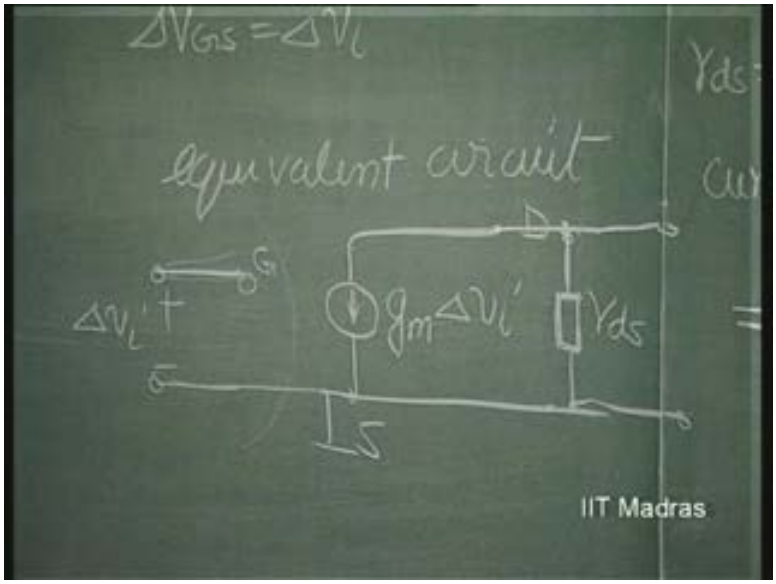

So, using this information, we can now connect R D because this R D is connected to ground, A C wise. So, R D comes into picture. So, the gain of this amplifier which is Delta V naught by Delta V i is equal to... What is Delta V naught? This is the voltage here across R D. So, Delta V naught by Delta V i is going to be minus... Why minus? Because, this current is going to increase as V i increases. So, you are putting it this way. Therefore, this potential will be plus and this will be minus. So, what is marked as Delta V naught is going to be really negative, times g m into r d s parallel R D. This is the effective gain.

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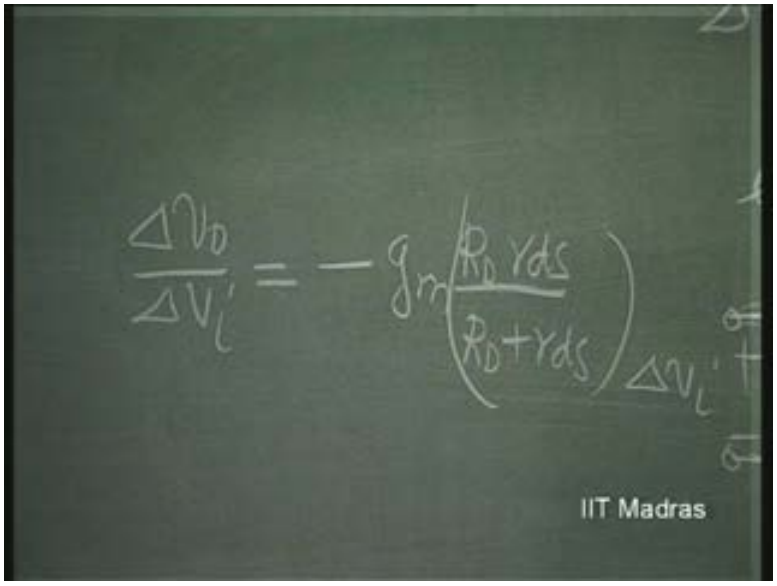

If it is infinity, we get back what we have earlier assumed, which is g m into R D, if r d s is infinity; otherwise, if it is finite, we say, it is g m into R D parallel r d s; R D r d s by R D plus r d s. This is going to be the voltage gain of a common source amplifier, biased towards at a voltage of V G S Q.

What is the input impedance? Input impedance R i is going to be infinity here. This is normally the case with this, field effect transistor; it is infinity here between gate and source. And, output impedance seen from here; always output is, you remove the so called load and then look at the output. In this case, it is how much? Nothing but r d s.

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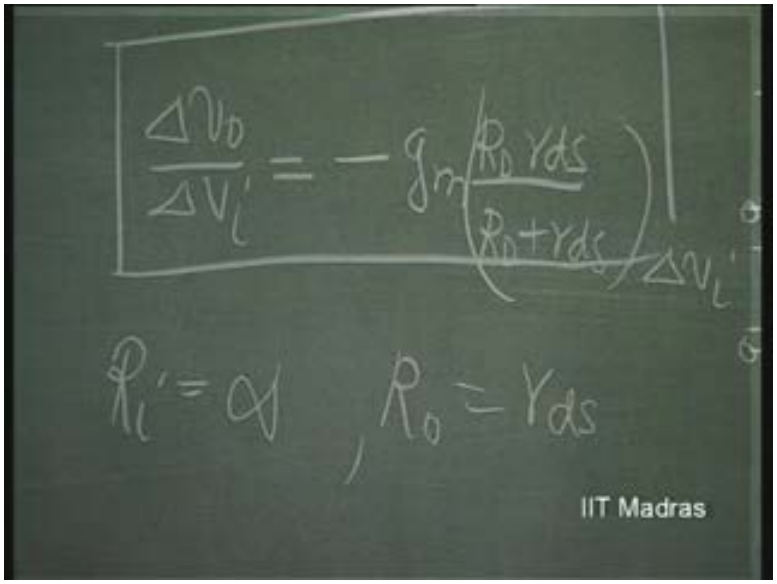

So, we now know the basic stage parameters: input impedance, output impedance and the gate. So, once again, I have to tell you that all the analysis that we have adopted for bipolar junction transistor, common emitter amplifier, is also valid here; it is exactly similar.

Once we know how to bias these things, etcetera, the analysis in terms of replacing it by an equivalent circuit is exactly similar; only the symbols are named differently. That is all. The parameter, for example, g m remains same as g m. This, instead of calling this as G S, we will be calling it as base emitter. Instead of this being infinity here, there will be some resistance R B B here. And this is, r d s is replaced by r c e here, collector to emitter. That is all. So, it is the similarity that is important; because, the same analysis is adopted for all the circuits whether they use a field effect transistor or bipolar junction transistor.

Now, we will just see how, therefore, the biasing arrangement also is similar to that of bipolar junction transistor. We will just therefore see the similarity between this and bipolar junction transistor. I have to bias this at a certain voltage called V G S Q. Otherwise, it is not possible to operate this. So, if I want to use it as an amplifier, I have

to put here a voltage of how much? V G S Q. Then, everything is alright. That I could do. But, I do not want to get a separate voltage. I will... I already have V D D applied here. So, I would like to generate this V G S Q from V D D. What did we do in the case of a bipolar junction transistor? We put R 1 and R 2 and attenuated this. So, we can do that.

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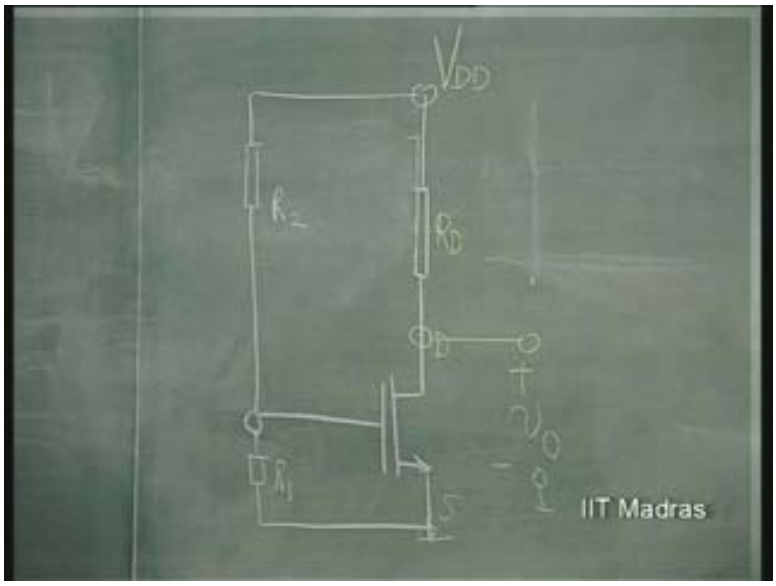

So, we get this Thevenin's voltage which is the same voltage as V G, which is equal to V D D into R 1 by R 1 plus R 2. This was the same in the case of bipolar junction transistor. We did the same thing. What we said was it is not only generating a Thevenin's voltage, but it has a series resistance; Thevenin's resistance, which was equal to R 1 parallel R 2, which is, in this case, is going to be called as R G. Earlier, it was R B B we had called it; R B B we had called it. And this was V B B, Thevenin's voltage. So, this therefore is equivalent to V D D. Then R D, ground; then we have R G and V G as given by this. This is pretty convenient because there is no gate current and therefore it does not make any difference what the value of R G is. The gate voltage is going to remain same as V G.

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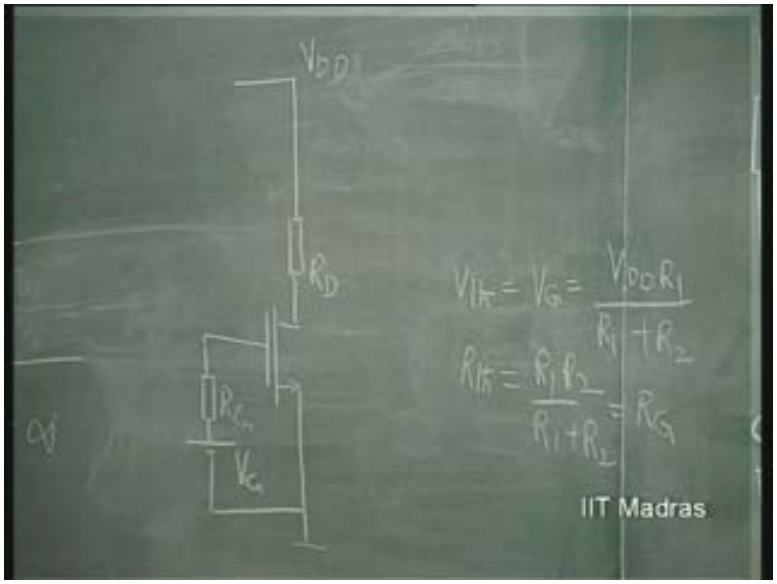

This is the advantage of the field effect transistor input as compared to the bipolar junction transistor. In the case of BJT, we had this trouble that there was current flowing through this R B and we had to make that current... or, we had to make that voltage drop across this resistance very small, in order to make it become negligible compared to V p. So, this we had to do in the case of ...; whereas here it is...

On the other hand, while applying a signal using a coupling capacitor, it had to be now coupled by capacitor because this is at a D C potential; I want to add the A C without disturbing the D C. So, I will now couple this by means of a capacitor Cc 1. This, we had used in the case of bipolar junction transistor also. So, when I do this, this particular thing definitely takes away current, signal current.

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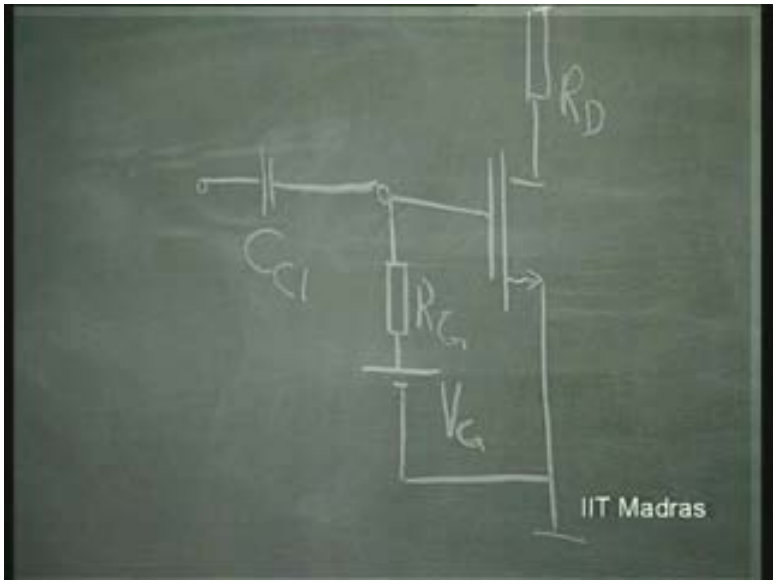

Because, as far as the FET is concerned, it is not taking away any current. It is this ((... Refer Slide Time: 23:00)) that takes some amount of signal power. So, R G has to be made very large. R G has to be made very large in order to make it take away as little amount of signal power as possible. So, this R G is made pretty high in the case of field effect transistor; of the order of, let us say few hundreds of Kilo ohms we can make, because actual impedance of the field effect transistor is of the order of what? This is an open circuit. It is a field offset. So, it is of the order of 10 to the power 12 ohms or so; almost nearly. So, you can put even resistances of the order of mega ohms if they are available readily. No problem.

So, this impedance is not going to get affected at all. It is this impedance which will dominate. So, in the gate of a MOSFET, you can put resistances of the order of mega ohms, if they are readily available. In the gate of a field effect transistor, since it is a junction, and junction resistance is of the order of tens of mega ohms, you better put resistance of the order of hundreds of Kilo ohms.

So, this kind of design, we have to remember here, in obtaining the voltage V G S Q that you would like to have. Now, in earlier situation, we said we wanted an operating point.

Now, this is an operating point which is fixed without any problem. But, are you happy with it? I am not very happy because, if I change the field effect transistor which is having a different value of K, the I D S is going to change, because the I D S Q is equal to K times V G S Q minus V T. So, I D S Q still depends upon this equation. It depends upon K. It depends upon V T.

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So, if I change the FET, the operating point will be different for the same value of V G S Q. So, this will cause problems. Why? Because, the operating point here is important in terms of what V D S Q it is having. V D S Q is equal to how much? V D D minus I D S Q into R D.

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This is the V D S Q. If I D S Q changes, this V D S Q changes. If V D S Q changes, I am not sure, when the signal comes, whether this V D S Q is sufficient to maintain it in the current saturation region. So, this is an important thing. For a given value of R D, this V D S Q depends upon I D S Q. Higher the I D S Q, lower will be the V D S Q; and therefore, I may have this FET operating in the triode region which is not the right region for keeping it in the active region. So, this keeps shifting.

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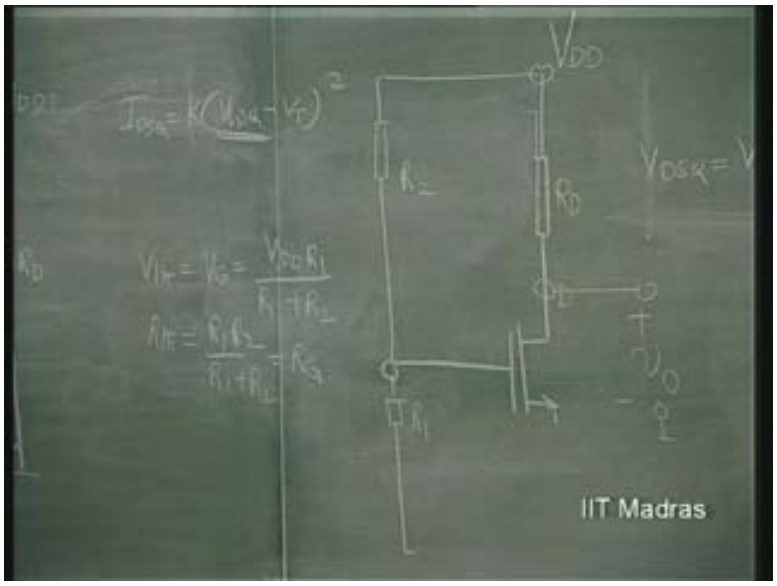

So, in order to obtain stable operating point, I should definitely, clearly, make I D S Q independent of the field effect transistor property. That is K r V t. How do I do it? This is very simple. It is necessary; therefore that this voltage V G should be shared between the FET and R S. I am introducing a resistance R S here.

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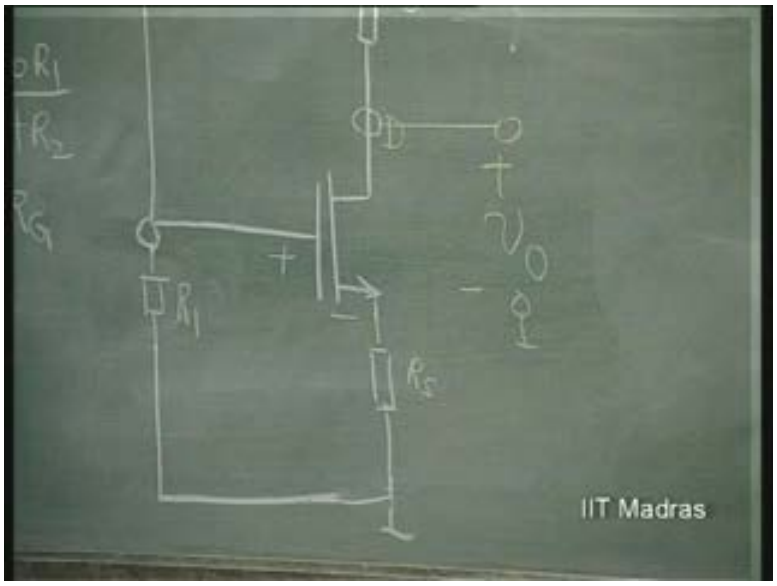

So, this voltage V G now ... this is what we have got, V G, is going to be dropped between this and this. Is this clear? So, if I have this arrangement, now, this is the equivalent. So we get, V G equal to V G S Q plus I D S Q R S.

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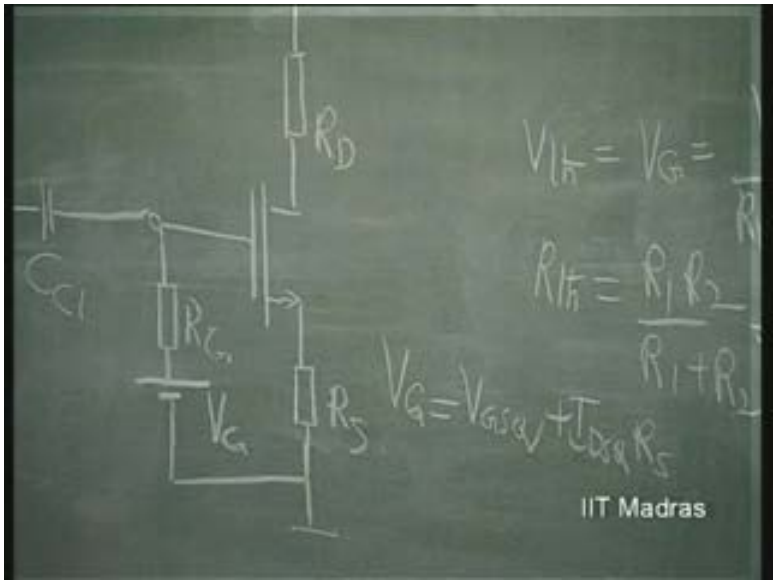

Is this clear? This voltage earlier was becoming totally equal to V G S Q. That was giving problem. So, what I did was put a resistance in series with the FET so that the drop across the resistance is dominant compared to the drop across this. So, if this becomes now negligible compared to this, I D S Q becomes equal to how much? V G by R S; totally independent of what? – the field effect device that you are putting here. So, if V G S Q is, if V G S Q is much less than I D S Q into R s.

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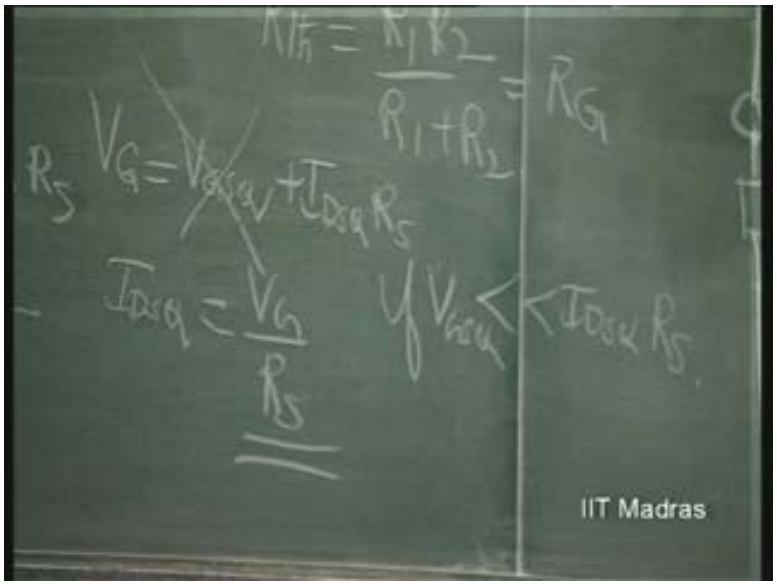

Is this point understood? What is V D S Q? V G S Q? V G S Q, strictly speaking, equals root of I D S Q by K. Take this square root, plus V T.

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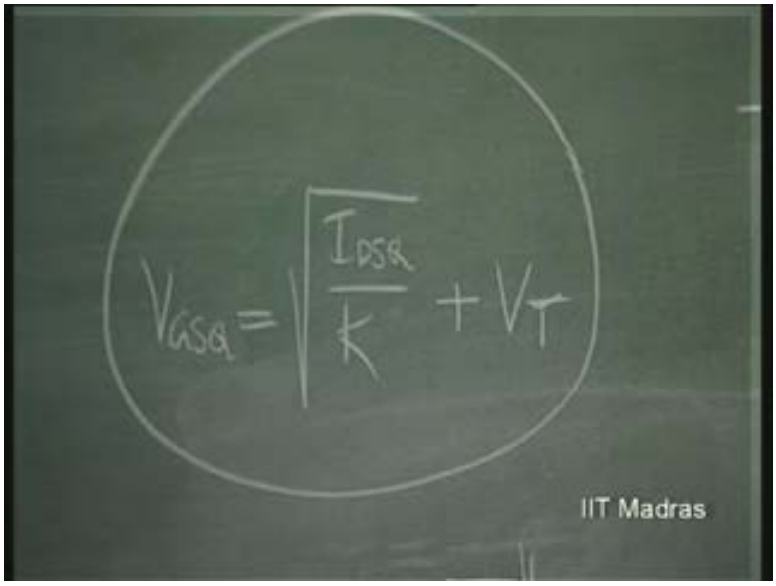

From this equation, V G S Q is root of I D S Q by K plus V T. Now, let me tell you; if you are designing a good FET, K is made very large. K is directly proportional to g m; g m is directly proportional to K. So, if you want high value of g m, K should be high. That is number one.

V T has to be made as small as possible so that most of the FETs operate in the current saturation region, even at very low values of voltages, V D S. So, V T is kept small, K is made large; that means, this factor, V G S Q will be, in most of the devices, very close to V T itself. So, you can use this information in sort of finding out the value of R S suitable for a certain value of operating current. This, when I take an example, you will understand it better.

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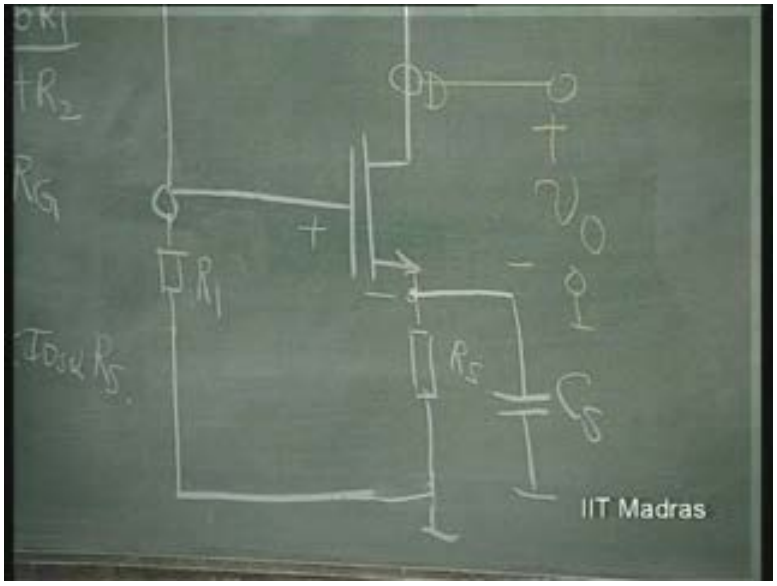

So, this particular thing later has to be bypassed by using a capacitor C S. This also we had seen earlier; how to select the value of the bypass capacitor. It should be selected in such a manner that it is a short circuit compared to any impedance seen from it, seen across it. So, it should appear as a short circuit. At the minimum frequency of interest of the amplifier, the reactance of this should be much less than impedance seen from this, or resistance across it.

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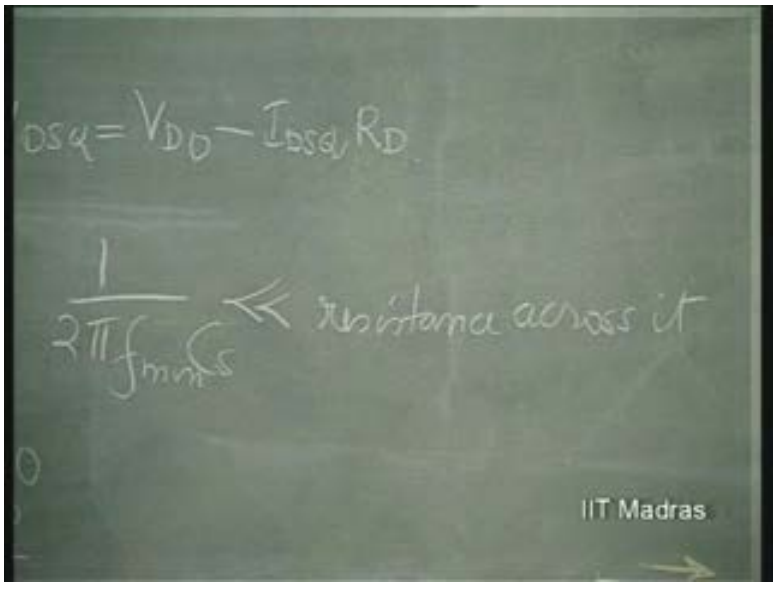

That part of it, we will see later – what should be the resistance across this, etc. But now, if this is a short circuit, then it is very nearly equivalent to, as far as A C is concerned, this is going to be a short circuit here.

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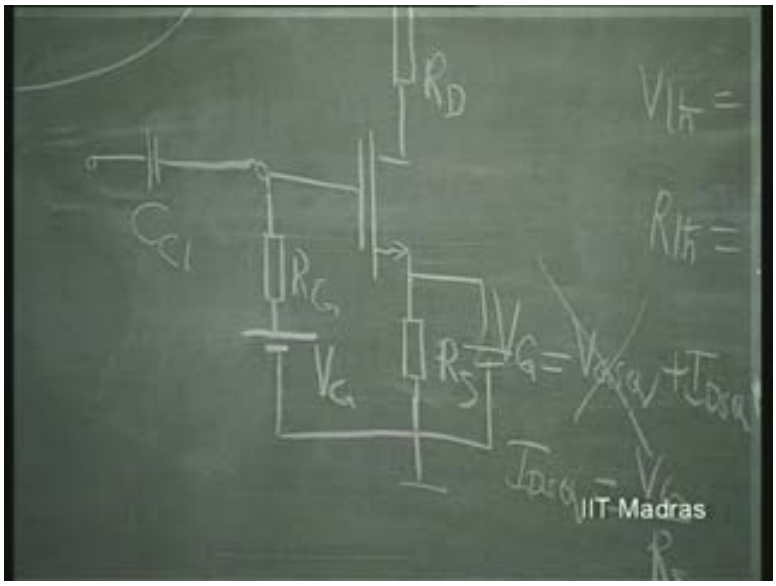

In the equivalent circuit, this is a short; that is a short. So, you get back your common source amplifier. This is only a biasing arrangement, in order to bias it at a specific operating current.

Now consider this Example 11. Design a common source amplifier using n MOSFET with V T equal to 1 volt and K equal to 1 milliampere per volt square to operate at I D S Q equal to 1 milliampere and V D G Q equal to 10 volt. V D D is given as equal to 20 volts. Determine its voltage gain.

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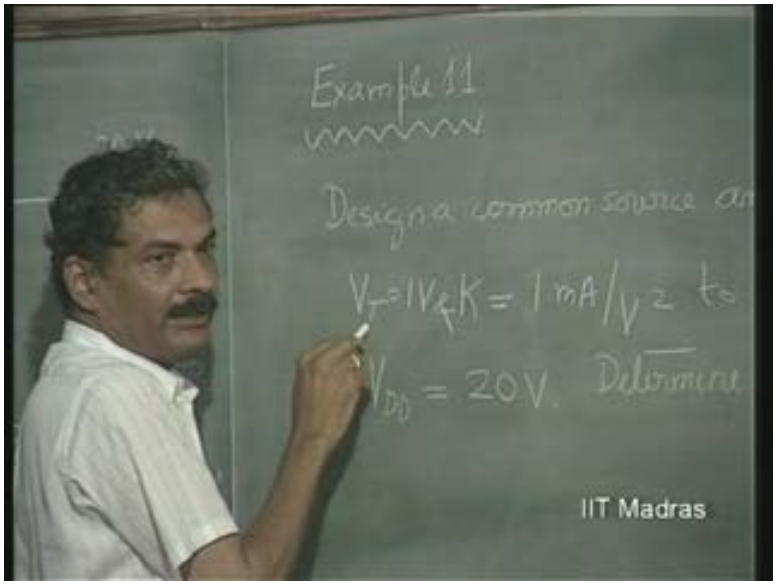

So, this is the problem. So, let us see how we can go about designing this in a fairly simple manner, without much of a difficulty. We know that we are going to use this V D D of 20 volts in order to derive whatever V G S Q that is required for this. It is required to operate this at a current of 1 milliampere; and K is 1 milliampere per volt square.

So, V G S Q equals root of I D S Q by K plus V T. I D S Q is required to be made equal to 1 milliampere. So, this is 1 by 1, which is 1, plus, V T equal to 1 volts. So, this should be equal to 2 volts.

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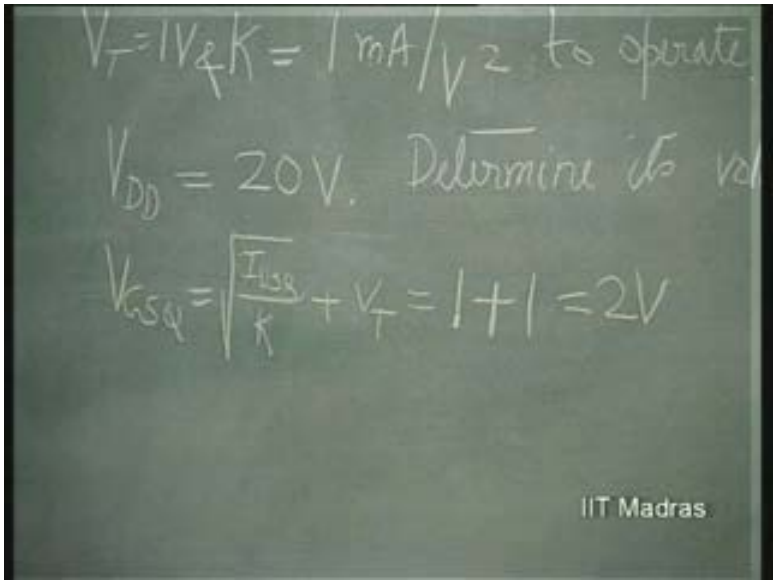

And, we are required to have V D G Q equal to 10 volts. So, let us indicate it here. This should be 10 volts. This should be 2 volts. So essentially, V D S Q, V D S Q is V D G Q plus V G S Q which is 12.

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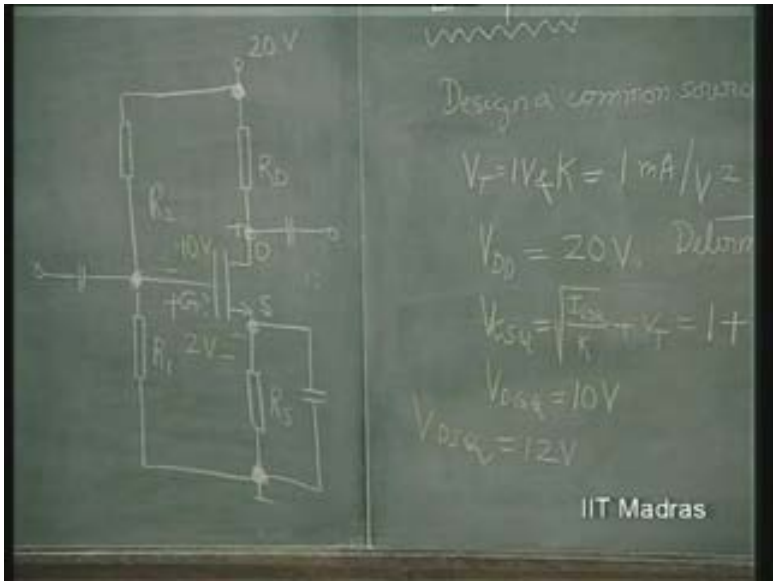

So actually, we have exhausted 12 volts already in this, from here to here, out of 20 volts. So, you have only 8 volts left for a drop across R D and a drop across R S; which is going

to be 1 milliampere into R D plus R S. So, if your intention is to make R S high, you have to make R D low. Please remember this. So, that is, we cannot therefore make R S as high as you please. There is a restriction on this. Further, we have this V G now. V G equal to these 2 volts plus 1 milliampere into R S.

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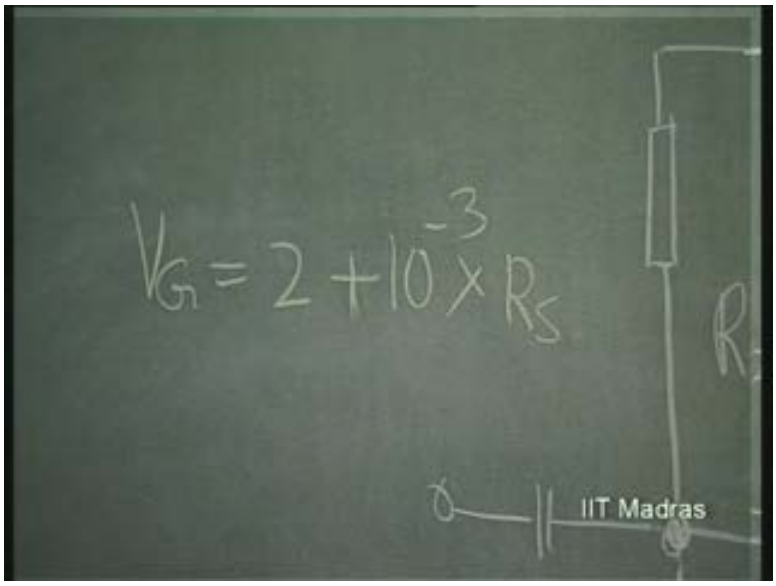

This is V G. This is already given as 10 volts. So, above this V G, we must have further 10 volts. Rest of it only has to be given to R D. Why am I emphasizing on R D is, R D should be made pretty large, strictly speaking, in order to make the voltage gain which is g m into R D into R D S divided by R D plus R D S. So, if our voltage gain has to be made very large, we have to have R D as large as possible, compatible with this idea.

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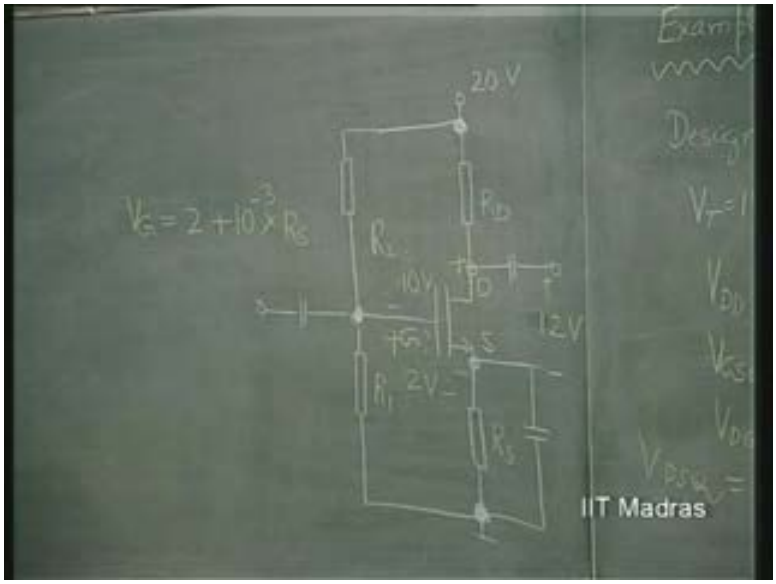

So however, this is already given as 2 volts. In order to make this drop negligible, this drop here negligible, compared to the drop across this; then only, it is a good operating thing. So, I have to make R S as large as possible, for this. For example, let us say, suppose V G is made 10 volts. This is 2 volts and this will be 8 volts. This is fairly good situation. This is 2 volts. Compared to 2 volts, I have chosen 8 volts. But you might say, why 10 volts? If this is 2 volts, I would like to have here, say 10 volts or even 12 volts or even 20 volts. Is it possible? It is not possible because, compared to 2 volts, if you want to make this very high, strictly speaking, you should have chosen it as 20 volts. If this is 2 volts and this is 20 volts, this is 22 volts. We have only 20 volts. So, this is a problem.

So here, for this given problem, I cannot make the operating point very stable. Do you understand this situation? I can make the operating point very stable only now, if I make this very high. Suppose I am given liberty to select the voltage here such that I can make the operating point stable. Then, what would I do? For 2 volts, I will straightaway take this drop as 20 volts. So, this resistance will be straightaway fixed at 20 Kilo ohms because 1 milliampere is flowing through it.

So, this is straightaway 22, 22. And then, 10 volts here. So, you have 32 volts. And then, R D, whatever you want, so that, R D into 1 milliampere will be the supply voltage here. So, I can select that supply voltage. So here, the supply voltage is restricted; therefore, you cannot make this operating point very stable. However, let us take this as now 4 volts, or 8 volts. If you take it as 8 volts, straightaway, this will be 10 volts. This is 20 volts. No drop here. That means you cannot have R D at all. So, we will take it as, let us say, 6 volts.

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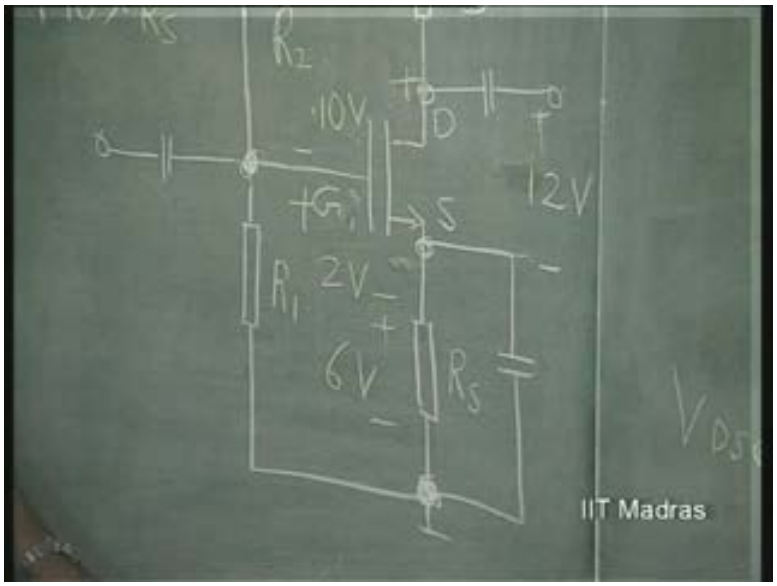

So, if this is 6 volts, then R S is 6 K, 1 milliampere flowing through it. So, V G is going to be 8 volts.

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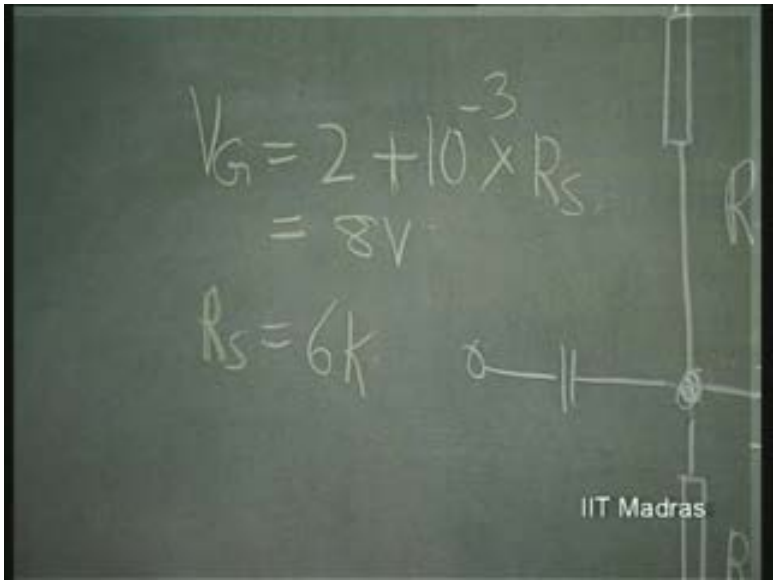

This is already what? 6 volts plus 2 volts plus 10 volts; that is 18 volts. So, what is required for R D is, 20 minus 18, 2 volts. So, R D is automatically fixed as 2 Kilo ohms. So, R D is going to be 20 minus 10 plus 2 plus 6. This is, that divided by 1 milliampere, which is, how much is this? 2 K.

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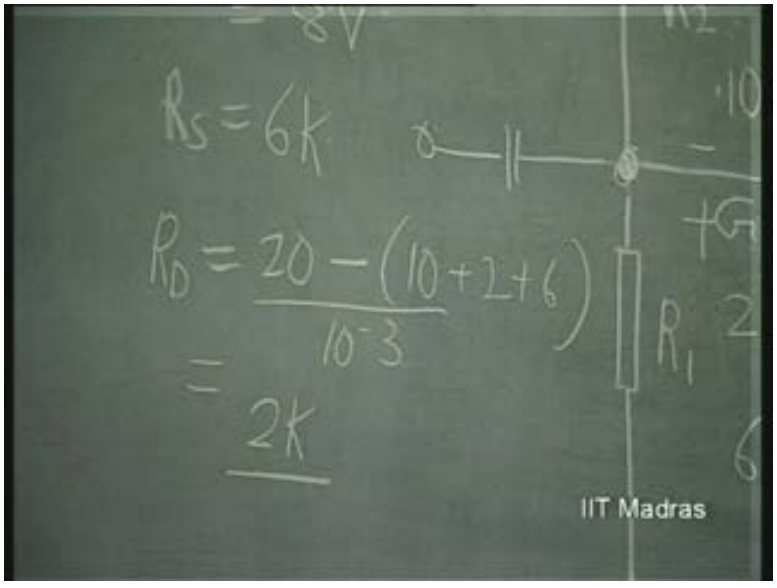

Another design would have been if I had chosen this as 4 K. I could have had this as, again, 4 K. Is this understood? What is therefore now fixed is 20 minus 12, 8 volts drop is fixed; and current is 1 milliampere. So, 8 K. R D plus R S cannot be greater than 8 K. It is just 8 K. It is fixed at 8 K. So, if I select R S as 6 K, this has to be 2 K. If this R S is chosen as 4 K, this will be 4 K. If this is chosen as 2 K, this can be 6 K.

So, let us therefore limit at this 2 K; and what else has to be done? You have to fix up R 1 and R 2. So, how do you fix up R 1 and R 2? R 1 by R 1 plus R 2 times 20 volts should be equal to 2 plus 6,8 volts. So, R 1 by R 1 plus R 2; that ratio is fixed now as 8 by 20 or 4 by 10. One way is, if I select R 1 as 4 mega ohm, R 2 is going to be 6 mega ohm.

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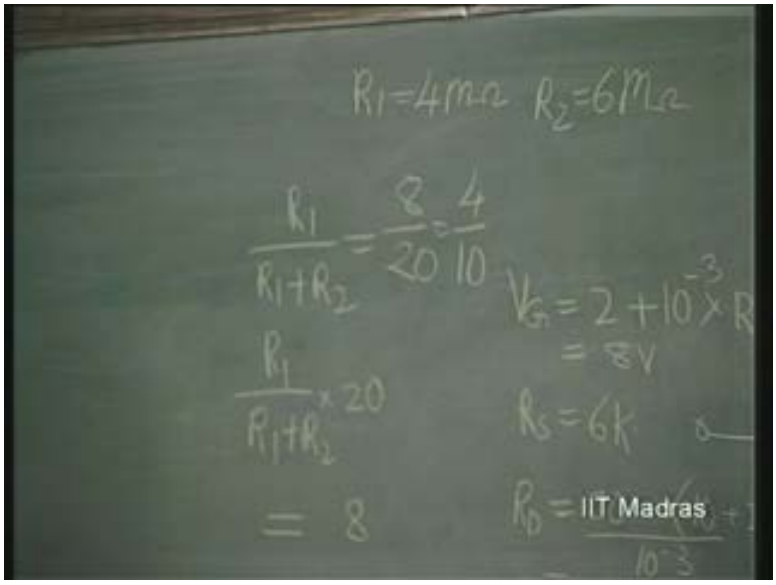

So, the design is complete except that now I have to find out the gain. So, how do we fix the g m? It is nothing but 2 K into V G S Q minus V T. So, this is 2 into... K is 1. V G S Q is 2. V T is 1. So, this is equal to 2 millisiemens. At the operating point, the g m of the FET is 2 millisiemens. Therefore, the gain is... R D S is not given; so, R D S, when it is not given, we will assume it as infinity. So gain, voltage gain is equal to minus g m into R D; it is minus 2 into... 2 minus 4; so pretty low voltage gain.

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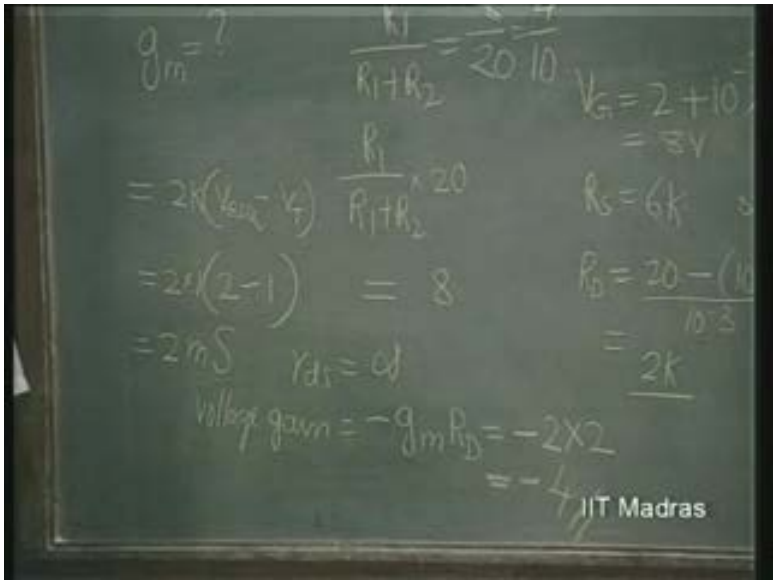

I had warned you that g m of a comparable, what is that? – dimension, bipolar junction transistor, will be of the order of 40 millisiemens or so at 1 milliamperes; so whereas, g m of this is only 2 millisiemens. And therefore, correspondingly, the gain is pretty low. It is very rarely therefore used as what? – amplifier. Field effect transistors are not so popularly used as amplifiers compared to bipolar junction transistors for this reason; that the gain of this stage is pretty low.

So, this example illustrates the problem of a field effect transistor amplifier design. What should be highlighted here is that this drop normally should be small compared to this drop, if you want the operating point to be independent of the FET characteristic. So, let us say, if you were asked to select V D D properly so that that is the case, then, for a 2 volt drop, you would take a 20 volt drop here. So, 20 volt drop, 2 volts drop, this should be 22 volts, and a substantial gain for the field effect transistors.

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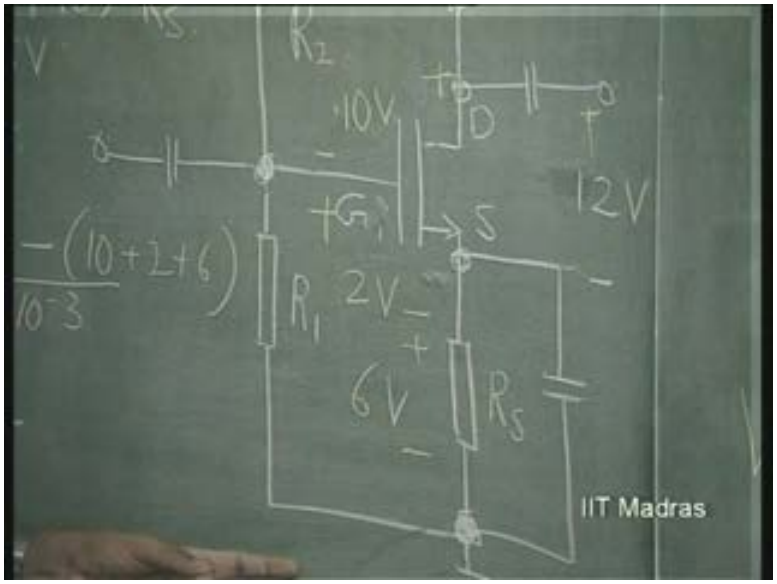

So, you can select R D as a high resistance compared to this. So, if you have taken R S itself as, let us say, 20 Kilo ohm, you would definitely select this also of the order of, let us say, 20 Kilo ohms. So, 20 Kilo ohm means further 20 volts drop. So, 20, 20 plus 12; 40, 52. So, V D D would have been 52. The cost of making the operating point independent of the field effect transistor is that the supply voltage V D D will be of the order of 52, in this case.

So, this kind of design, you must always remember. If you are given the choice of selecting supply voltage fixed, etcetera, for these amplifiers, another way that we had also discussed in the case of bipolar junction transistor is to use dual supplies. This is using single supply. How to use dual supply and bias the field effect transistor? That is pretty simple. So, we have this FET. Instead of using single supply, I will ground this and now use here. This is V D D. I will use V S S here and put an R S here. This is the alternate way of biasing.

In the case of bipolar junction transistor, we started with dual supply and went over to single supply. In this case, we have started with single supply and going over to dual supply, just to make you understand the basic concept properly. If you are given the

choice of biasing this using dual supply, we will fix the current using R S itself here. So, it is very simple. Now, for the same problem, this should be 2 volts, we are told.

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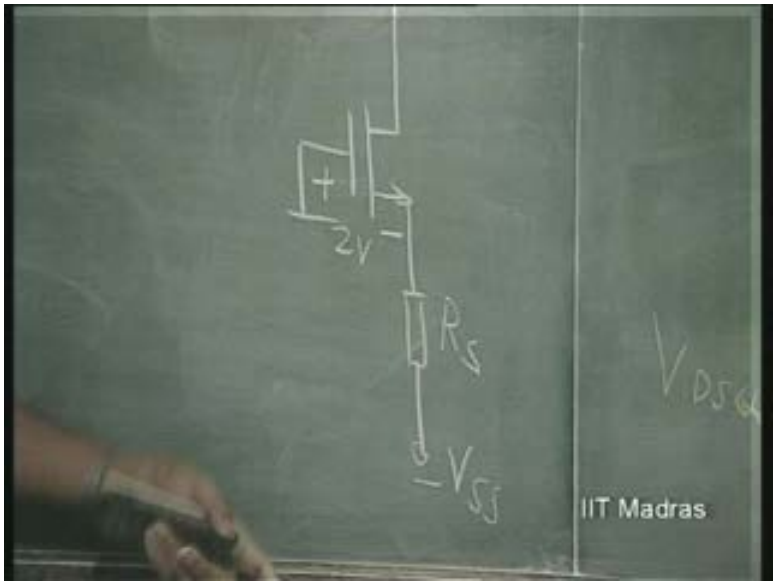

Now, I have the choice of R S as well as V S S, in order to make it, whatever current i WANT. Obviously, now I will select this straightaway as 20 volts, let us say. 2 volts is very small compared to 20 volts. So, V S S becomes automatically equal to minus 22 volts.

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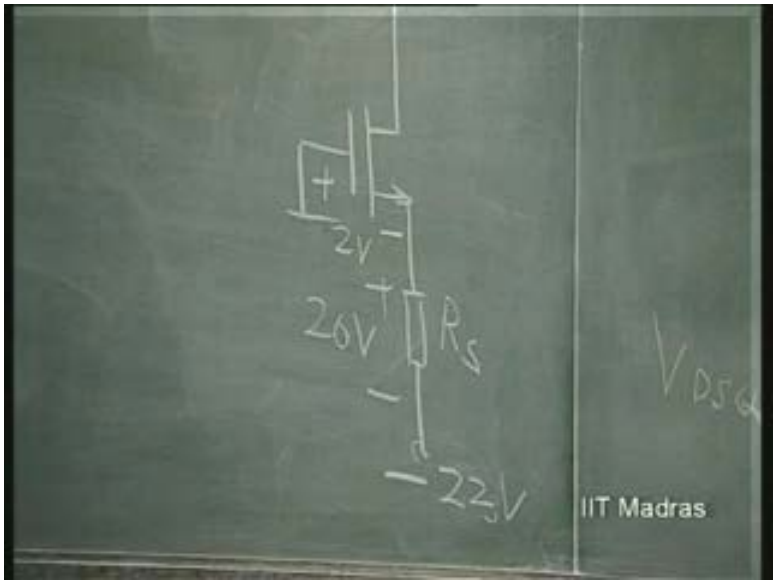

Is this clear? So, what is the value of R S? 20 Kilo ohms. That fixes up the current independent of this V D G. V D G is going to be 10 volts. So now, R D is going to be selected as 10 K in order to make V D D equal to 20 volts. So, V D D is equal to 20 volts. R D is equal to 10 K because, this 10 volts is already given to this. The other 10 volts can be given to R D so that, this V D D becomes equal to 20 volts.

For the same problem now, the design is changed based on option to use two power supplies. The gain now becomes minus 20 because g m remains the same. I D S Q is the same. So, g m remains the same. So, since R D has been permitted to... we selected as 10 K, the gain is minus 20. The operating point is the same as the previous case. But I am now permitted to use two power supplies. The number of resistors that I need to use gets cut drastically. So therefore, you are permitted to use two supplies straightaway. The resistors, R 1 and R 2 are totally unnecessary.