Electronics for Analog Signal Processing - I
Prof. K. Radhakrishna Rao
Department of Electrical Engineering
Indian Institute of Technology – Madras

Lecture - 28
VARIETIES OF MOSFETS & JFETS

In the last class, we were exposed to the variety of MOSFETs as well as JFETs available to us. And we are now depicting these things symbolically, covering all the possible combinations of, types of, types starting with JFETs, n channel, p channel. These are basically depletion mode devices. And then we have enhancement mode devices, where there is no channel existing. Only after a threshold voltage is applied, the channel can come into existence.

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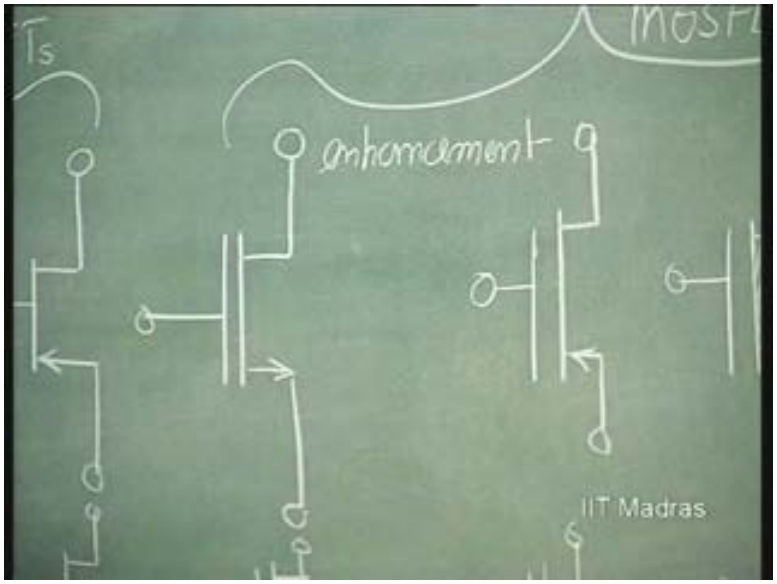

And then, we have in this n channel and p channel.

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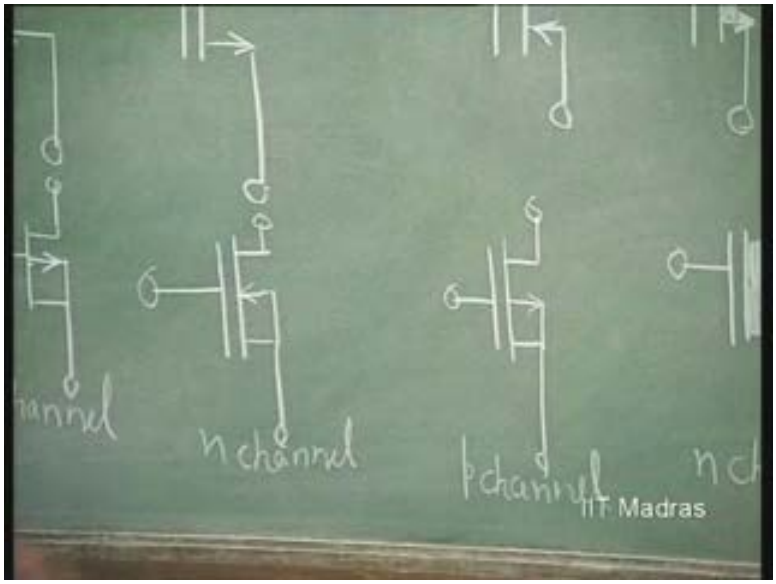

Then, we have the channel already diffused into this. So, these are the depletion mode MOSFETs which can be operated also in enhancement mode; but they are popularly called depletion type of MOSFETs.

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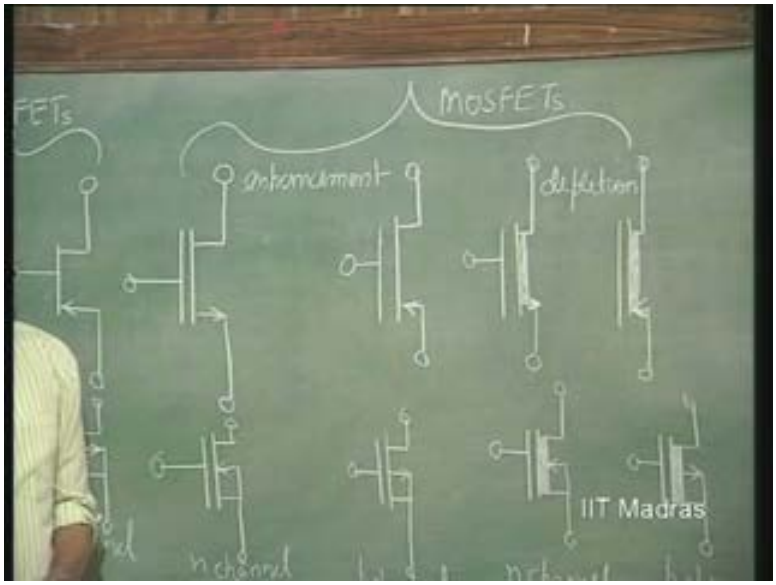

So, let us therefore use these active devices in a variety of applications. First and foremost, I would like to bring out the fact that any of these FETs, one can use as a resistor, voltage dependent resistor. So, this controlled voltage dependent resistor effect of the FET is what we are now going to discuss in detail because, unlike the bipolar junction transistor, this is one active device which can also be used as a passive device. That is a controlled resistor.

So, let us see how this FET, it could be JFET, enhancement type of MOSFET or depletion type of MOSFET. I am just taking one type of FET here. Since the equations look identical, whether it is enhancement or depletion type, we can use the one particular type for illustrating any particular example. Now we know that I D S... this is the drain, this is the source and this is the gate. The I D S versus V D S, if you plot, it is going to be linear as long as ((V D S is ...Refer Slide Time: 4:30)) This we have understood.

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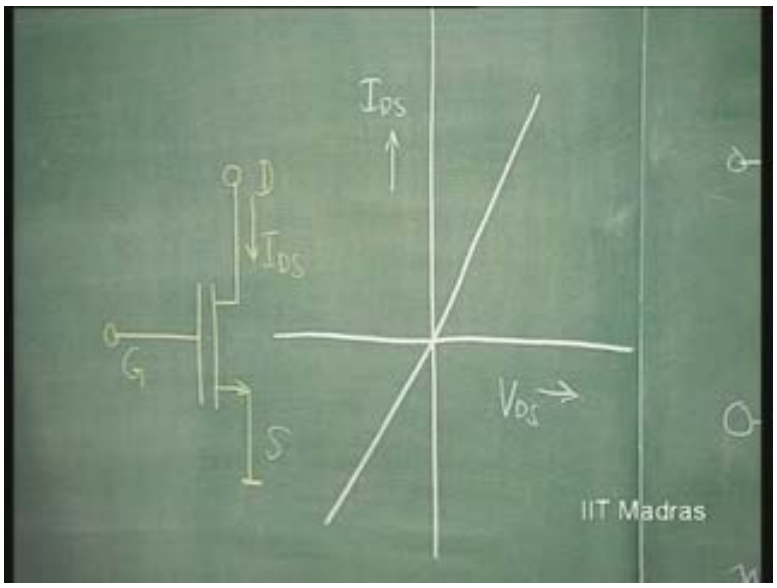

And we have understood also that this equation is simply governed by I D S equals 2 K times V G S minus V T into V D S.

So, please remember this. This linearity comes about because of this relationship. I D S is directly proportional to V D S and the proportionality constant is 2 K into V G S minus V T; which means that, the resistance R ds, which we said is going to be quite useful for us, is nothing but V D S. See the difference. This is supposed to be V D S divided by I D S itself; V by I – ohms law; and that is equal to 1 by 2 K into V G S minus V T.

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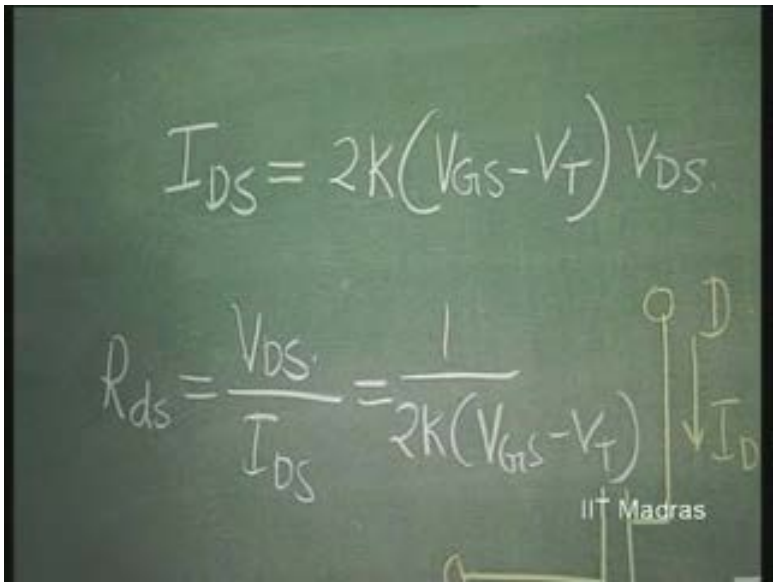

This is valid, when? As long as it does not really go to, what? – this non-linear region. After a certain point, this goes to non-linearity here. So, this resistance, linearity, should not be disturbed by this non-linearity. Similarly, it goes like this here. So, as long as that is not disturbed, as long as the deviation from the linearity is not much; that means, around V D S equal to zero, any of these FETs can be straightaway used as a control resistor. This slope being controlled by this V G S.

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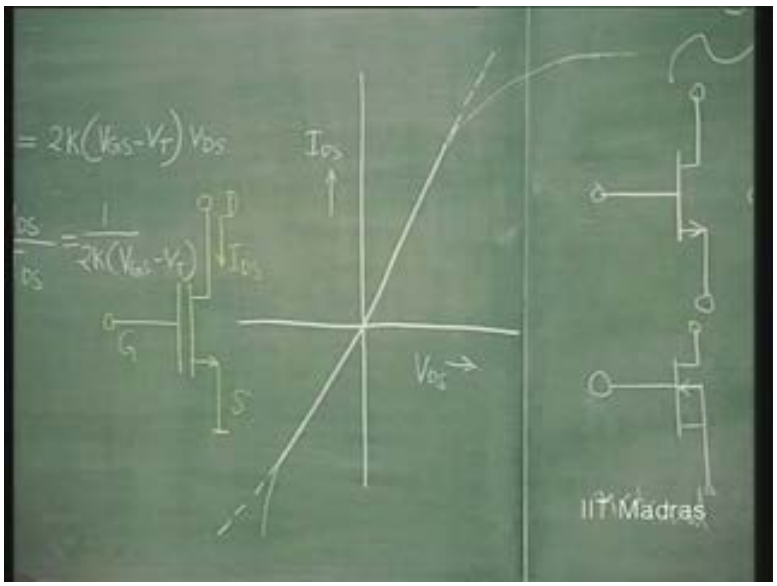

Now, further modification. I D S, actually speaking, equals 2 K into V G S minus V T into V D S and that this non-linearity, we said, is square law, V D S squared by 2. This is approximate; therefore you will say. This is exact.

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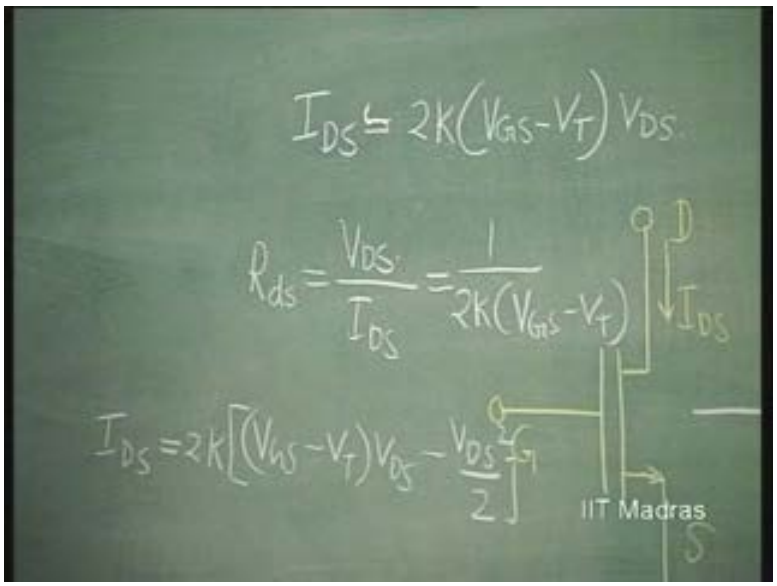

Now, suppose I want to use this as a good linear resistor in this region. This equation is valid for what? V D S less than V G S minus V T; less than or equal to.

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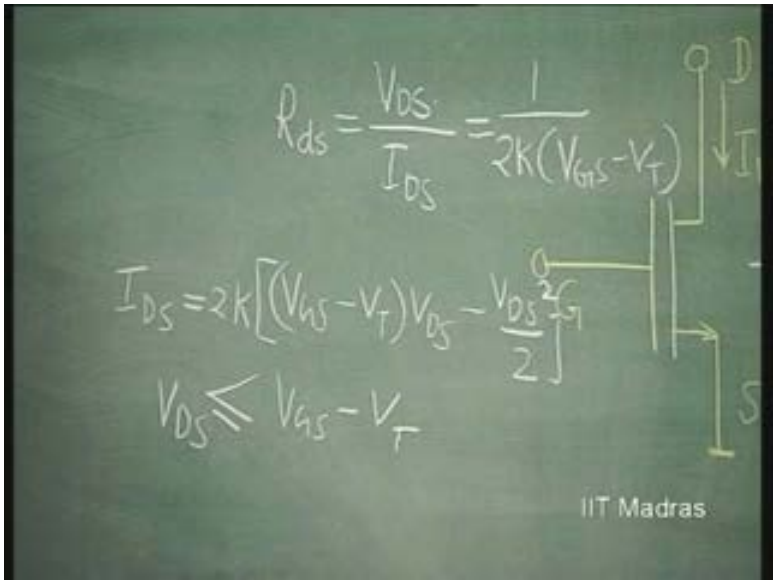

That is called the triode region; or V D S less than or equal to... until pinch off is reached, this is valid. That is, this is valid up to this point; and this voltage corresponds to V D S equals V G S minus V T.

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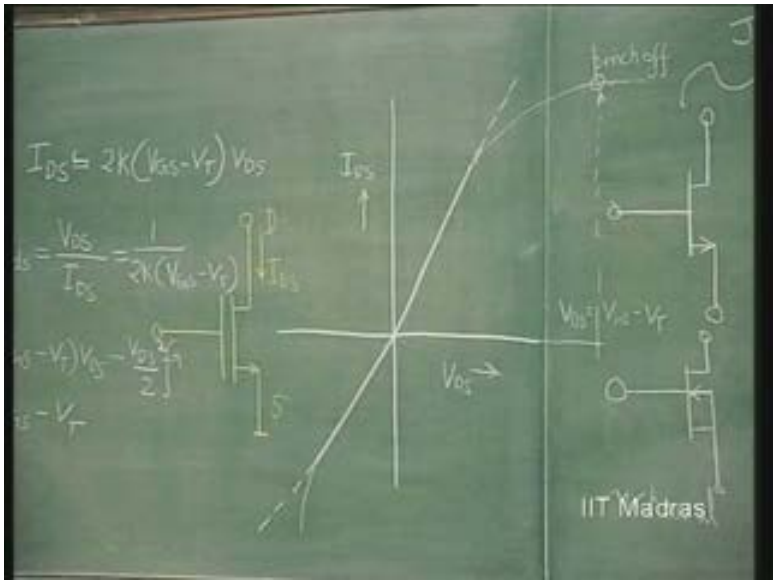

So, this is ... It is valid up to that; this equation is valid. After this point, that is, for V D S greater than V G S minus V T, what is valid? That you can substitute. V D S equal to V

G S minus V T and you will get it as K times V G S minus V T whole square. That is what is correct. Now, in this region, can I therefore compensate for this non-linearity?

So, what we are now, today, going to discuss is to make it more linear by compensating for this non-linearity. So, this can be done using circuit. What is responsible here is this V D S square by 2. This is getting subtracted from this and is getting added here because this V D S is positive here and V D S here is negative. So, and this remains negative throughout. So, the current increases here; the current gets saturated there; because of this non-linearity.

Now, how to get rid of this? Suppose I make V G S equal to... I want to get this rid of this V D S. So, I will... See, if I make V G S equal to V D S by 2 plus something, this V D S we will multiply with V D S by 2 and cancel this. So, I will make V G S equal to V D S by 2 plus, let us say, V C by 2; some control voltage. This is some...

This is an independent voltage. But, I will make V G S equal to... To compensate for non-linearity, make V G S equal to... How we make this to be same? Make V G S equal to V D S by 2 plus V C by 2. V C is the control voltage. Normally, V G S is made equal to V C. Now instead, we make V G S equal to V D S by 2 plus V C by 2.

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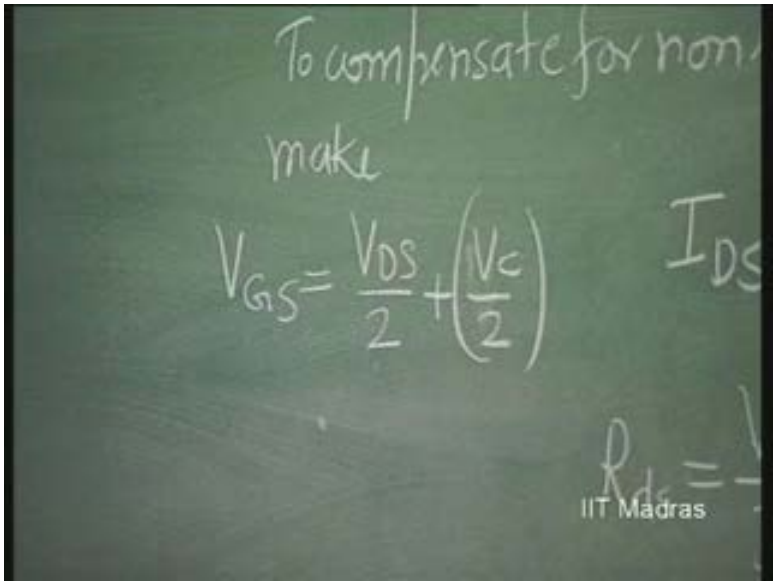

Then, what happens? Substitute V G S here. So, what do you get? This becomes 2 K into... If you do this, 2 K into V G S, V D S plus V C by 2 minus V T into V D S minus V D S square by 2. Now, what happens here? This term cancels with this term, exactly. V D S by 2 into V D S is V D S square by 2 gets cancelled with that; and we are left with 2 K into V C by 2 minus V T into V D S, which is perfectly linear as far as V D S is concerned.

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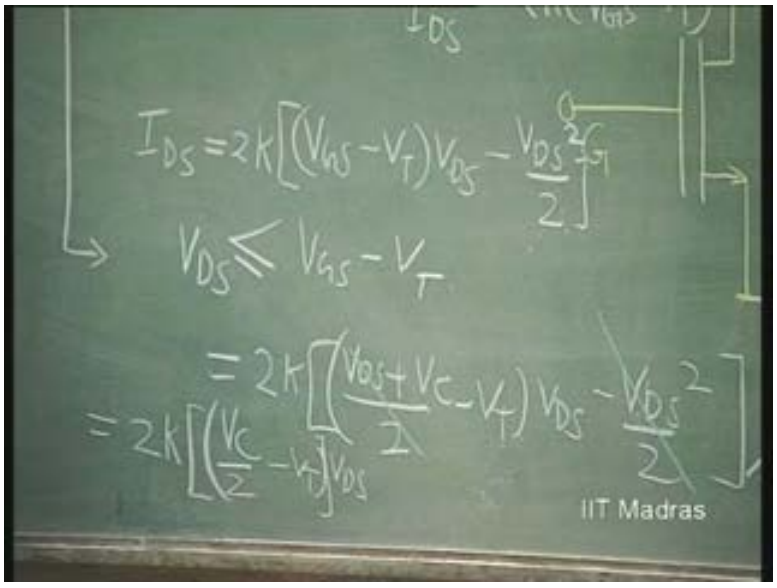

Now, what is the circuit that will give you V G S which is V D S plus V C by 2? A simple resistive attenuator. Let us see how it looks like. So, if I use here, here V C, this is nothing but... What is this? This is V D S. This voltage is V D S. This is V C. So, I put equal resistors R and R. This is anyway gate. This will not... So, if I put equal resistors R and R here, the voltage here at the gate which is V G S, because S is grounded, is going to be V C plus V D S divided by 2. Is this point understood? This voltage is defined as V D S. This is V C. So, at this point, I can get V G S, that is, which is equal to V C plus V D S by 2.

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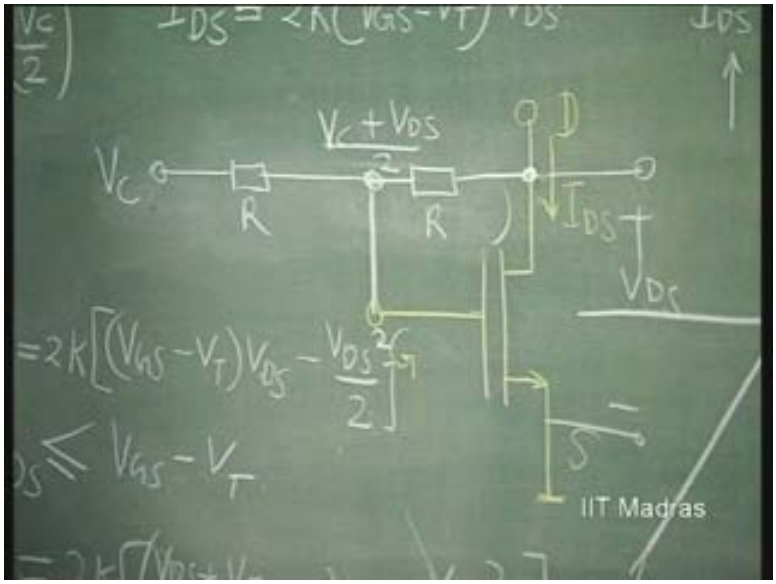

So, a simple circuit like this is going to get rid of this dominant non-linearity. That means now it is enough if V D S is less than or equal to V G S minus V T. As long as that is true, this relationship is valid; whereas in earlier situation, when you have wanted to approximate this, then V D S should have been much less than V G S minus V T. Then only you can make this approximation of neglecting V D S square by 2.

That means you should have worked at a voltage corresponding to a point which is much less than this point; farther into this. Whereas, because of this, now you can go all the way up to pinch off, as long as you are in the triode region. As long as this equation is,

valid, this is perfectly linear. That means these things are becoming perfectly linear here for all the FET characteristics. Is this understood? This is an important concept of linearization, of perfect resistance, which you can use in your practical circuits, wherever you want to control resistance.

Let us see the application of control resistance. So, the same circuit is valid whether it is a JFET or a depletion type of MOSFET. I have illustrated it for what? – enhancement type of MOSFET. The non-linearity occurring in all these things will be exactly same type; which is, V D S square by 2 type.

Now, let us consider the circuits which are possible with these active devices. As we did in the case of bipolar junction transistor, first we will consider the basic inverter. So, I will consider now what you will call as n MOS inverter, just as an example. You could as well say p MOS inverter or CMOS inverter. But n MOS and p MOS inverters are looking almost exactly identical in their characteristics, except for the voltage bias difference.

So now, for the time being, I will put a resistor here, just as we have been putting this voltage as V C C in the case of bipolar, because this is for biasing the collector base junction, we will call this V D D because we are connecting it to the drain. So, this is a single supply in this. Now, consider this circuit, simple circuit. We have this as, let us say, positive; and here we are applying V G S. This is the output voltage which is equal to V D S. This is the input voltage. V i is equal to V G S is the input voltage. V naught equal to V D S is the output voltage. Now, call this resistance as R D.

So, we would like to now know about the, what is called transfer characteristic. What is it? Let us put this as I D S. So basically, we can write down the characteristic in the following manner – that, V D D minus... This is D C I have put. If I consider the instantaneous values, I can consider it as i D S. This is the symbol we have been consistently adopting.

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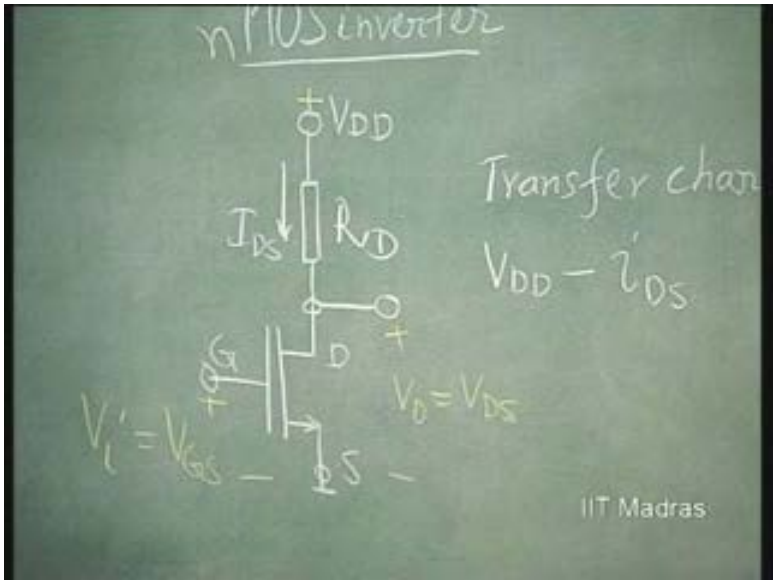

Instantaneous value; it is varying, time varying. It will contain D C as well as A C. i D S into R D equal to V D S. V D D minus the drop here, which is i D S into R D, is the voltage which is V D S, which we will be calling as the output voltage.

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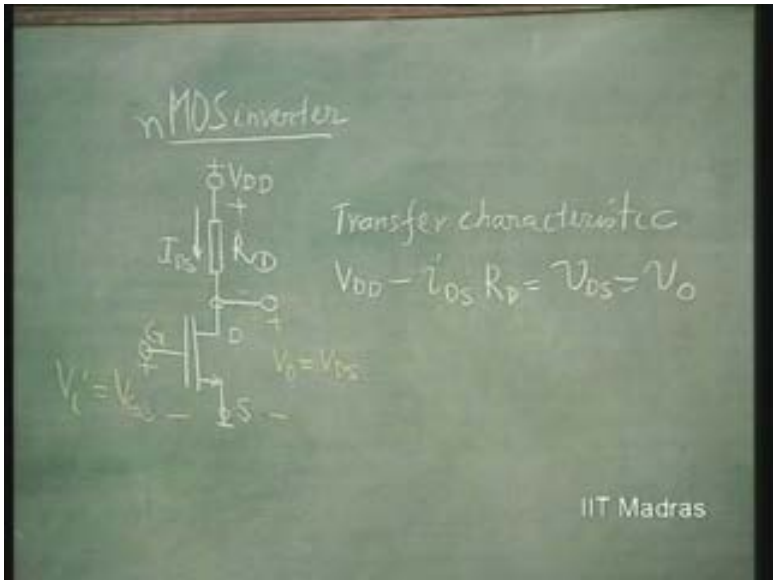

And we have V G S same as equal to V i. That means i D S equals... assuming that the transistor is in the current saturation region, i D S is equal to K times V G S minus V T

whole square. So, K times V G S minus V T whole square; which is equal to K times V i minus V T whole square.

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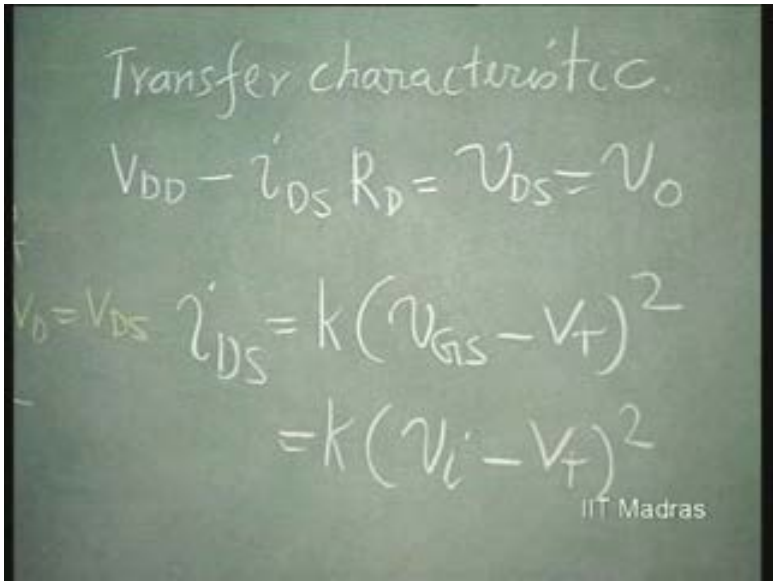

So, we are getting the relationship V naught as equal to V D D, a constant voltage, minus i D S, which is K times V i minus V T whole square into R D. This is what is called as the output versus input characteristic.

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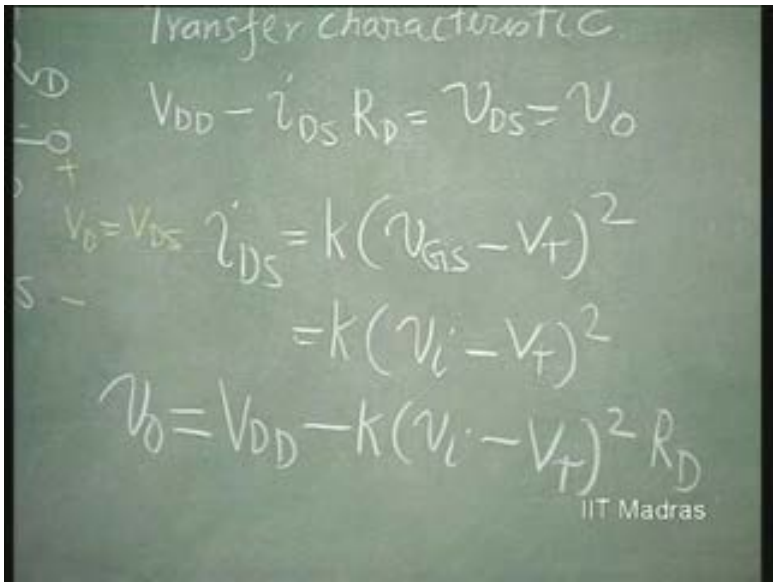

We therefore plot V naught versus V i. Until V i becomes equal to V T, there is no i D S. Until V i becomes equal to V T, there is no i D S. i D S is zero. It is off. The FET is off. Until threshold voltage is reached, current is zero. So, until V i equal to V D S, V T is reached, I D S is equal to zero. The transistor T is off.

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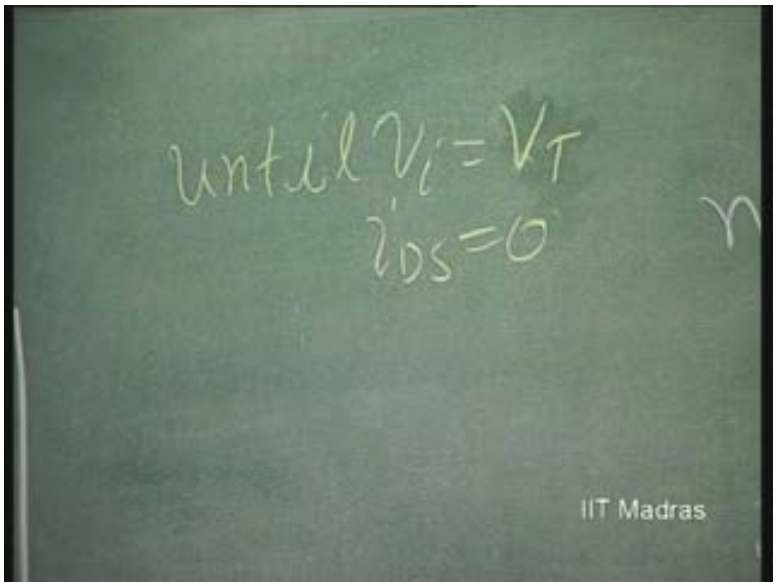

So, output is going to be at V D D. Output is going to be at V D D because i D S is zero. T is off at, let us say, V i equal to V T. The channel has got formulated and the current starts flowing. So, what will happen to the output voltage? It will start decreasing. Now, is the FET in the current saturation region or triode region? In this, here, T is off. The question is, the voltage here, V D S in this case, is equal to V D D itself, because V naught is equal to V D S. So, that is equal to V D D. That is the highest voltage possible.

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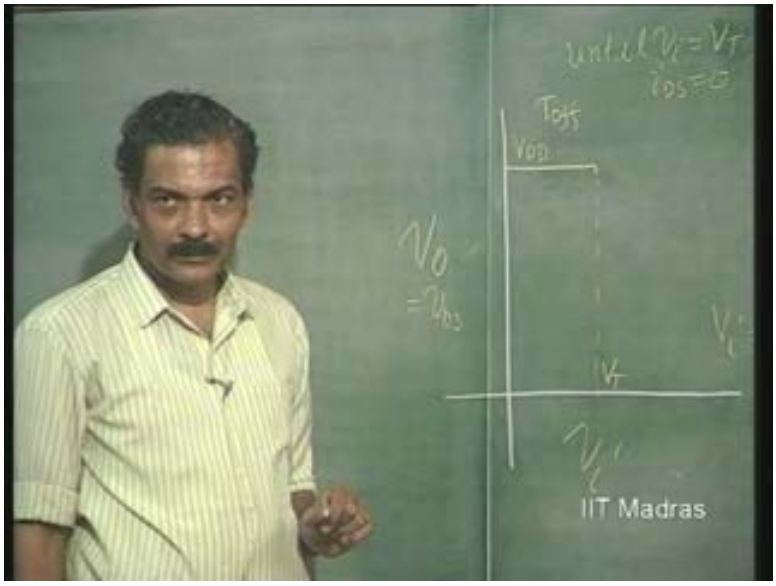

The current is starting from zero. Is the FET in the current saturation region or triode region is my question? Have you understood the question? Where is the transistor located? This voltage is the highest possible. The current, the triode, the transistor enters current saturation region for all voltages V D S, greater than V G S minus V T.

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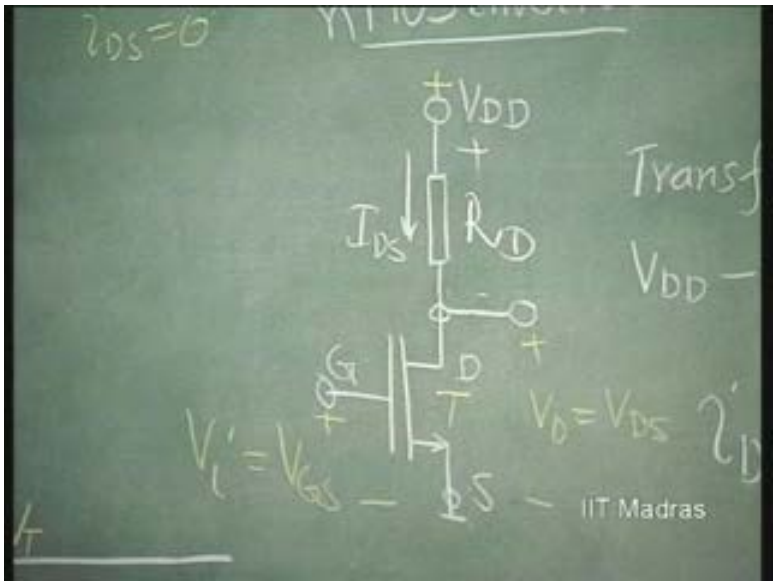

V G S in this case is V i. That means, for all voltages greater than V i minus V T, the transistor is going to be in the current saturation region. Obviously, if at all I want this transistor to be in the current saturation region, this particular point at which I D is zero, and this is the highest, should be the point where the transistor is in current saturation region. So, that is the highest voltage V D S possible, V D D. So, the transistor at this point is in current saturation region.

That means the equation that I have used is straightaway valid. Why? Because, V naught is equal to V D S is equal to V D D; and therefore T is in current saturation region, because V D D is greater than V i minus V T. That is the assumption.

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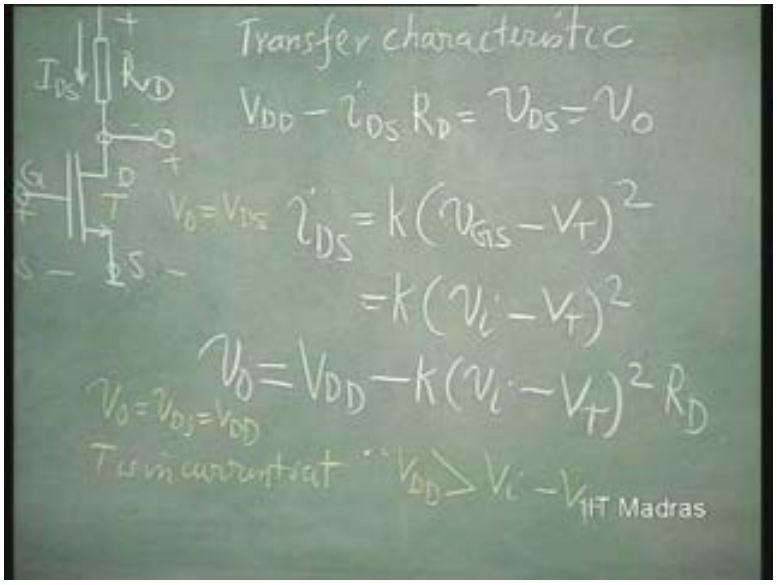

Then, this particular thing therefore is going to, let us say, decrease in a square law. That means something like a, what? Something like... square law means what? This is x square; y is equal to x square. That is a parabola. So, ... And up to what point will it go on like this? Until it enters triode region. Because now, this V D S is going on decreasing. Initially may be, V D D is greater than V i minus V T. Now, V D S is decreasing. Not only that, V i is increasing. V i is increasing; V D S is decreasing.

So, there must be some point at which... What is that? What is that point at which V i minus V T becomes equal to what? V D S; or, V naught. V G S minus V T equal to V D S is the point at which it enters triode region. V G S is equal to V i. V D S equal to V naught. So, corresponding to a point V i minus V T equal to V naught, it will enter triode region.

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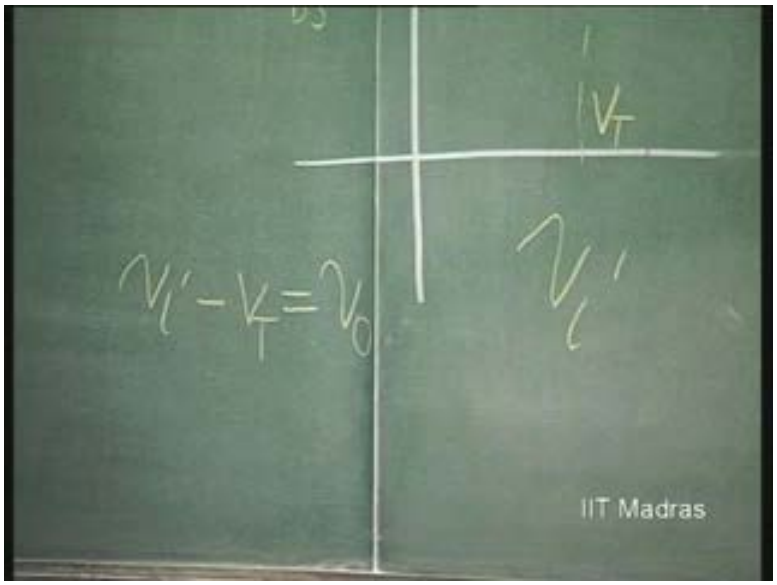

How do we know this? Because, this is one curve, this is another curve. What is that? V i minus V T equal to V naught is a straight line. V i minus V T equal to V naught is a straight line. With... put V naught equal to zero, there will be V i equal to V T. That means at V i equal to V T, there is going to be an intercept here. V i equal to V T – this point. This is the point already; and I draw a line like this with 45 degrees; because, if this scale is same as this scale, that will be a slope of 45 degrees and that corresponds to V i equal to V i minus V T equal to V naught, this line.

And this line will intersect this line. What is that line? This one – V naught equal to V D D minus K into V i minus V T whole square.

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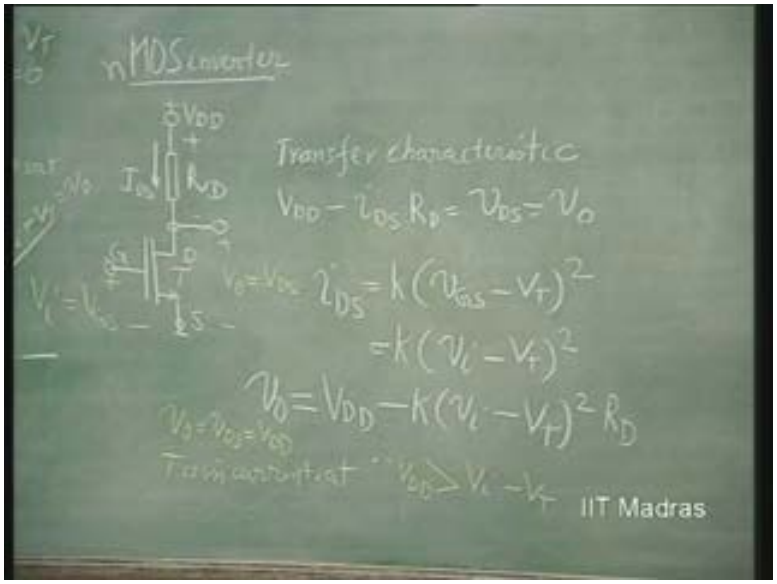

That will intersect at a certain point.

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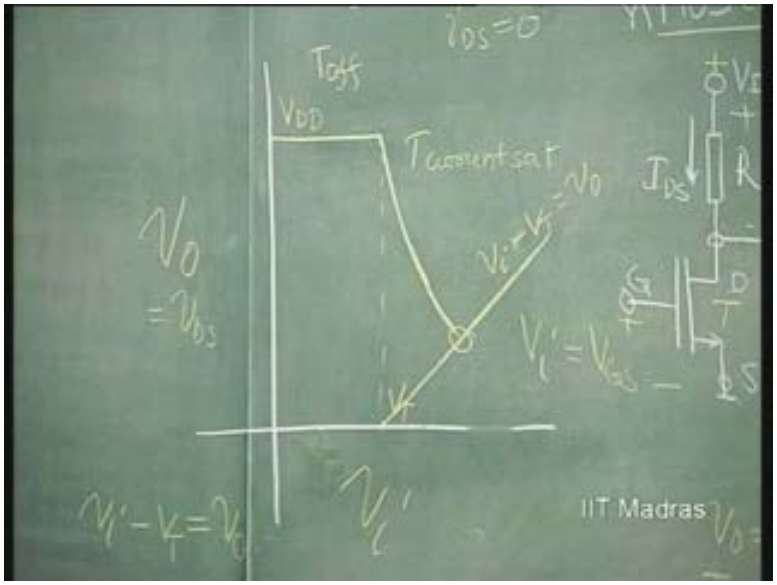

Thereafter, what happens? The FET is no longer in current saturation region and it has entered the what? – triode region. That means the equation that is valid now corresponds to V naught equals V D D minus... What is that equation that is valid? 2 K into V G S is V i minus V T into V D S, which is V naught, minus V naught square by 2. Is this clear?

This is the equation that is valid. That is, 2 K, this into R D. I D S is going to be now 2 K into V G S minus V T, which is V i minus V T, into V D S, which is V naught, minus V D S square by 2, which is V naught square by 2, into R D.

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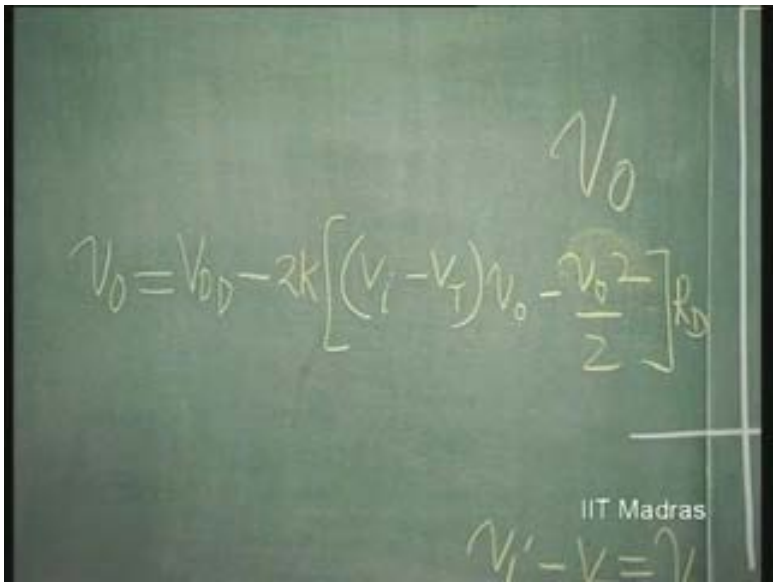

So, this is the equation that is valid in this region. So basically, the active region, the so called active region, where the FET is acting as an amplifier, is this region. Here, the transistor is entering the triode region. Here, the transistor is off. So, T is in the triode region. Here, the transistor is in the current saturation region.

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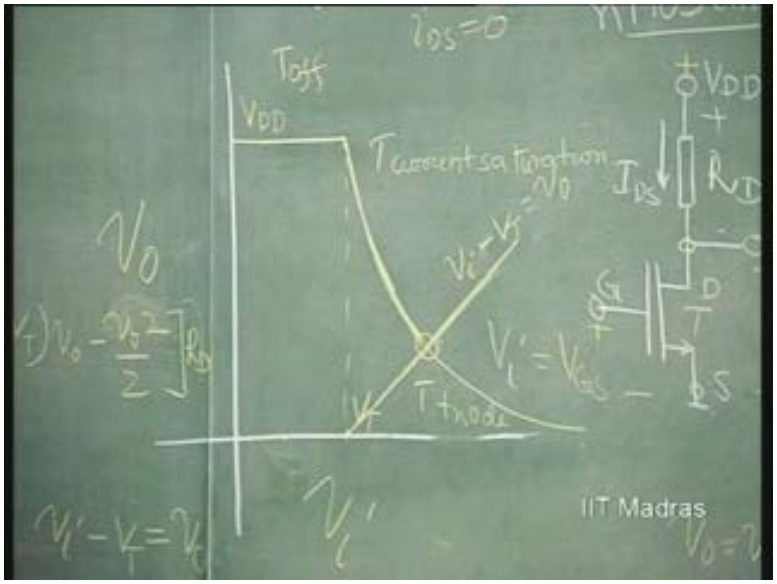

So, this is the complete characteristic of an n MOS inverter. This also can be used as a digital gate. You have high as the input. Output is going to be... That is, you have high as the input; output is going to be low. V i is equal to, let us say, this is the point, V D D. Output is going to be low. If the input is low, output is going to be high. So, this is a digital inverter, the famous n MOS inverter, which has been liberally used in all your what? – VLSI circuits because of its simplicity.

Now, only thing is, there is no such resistance that is used in these inverters in VLSI circuits, because the resistance takes up lot of what? – space. We know that MOSFET itself can be used as a resistance; just now we understood. So, why not put MOSFET itself as a resistor instead of using a physical resistor there? Therefore, in digital inverters, all the resistors get replaced by MOS resistors; MOSFETs acting as resistors.

So, we will discuss that circuit later but this circuit can also be used as an amplifier in this region, if you are operating... If you select your operating point anywhere in this region, this is going to be used as what is called as common source amplifier. So, n MOS inverter or common source amplifier.

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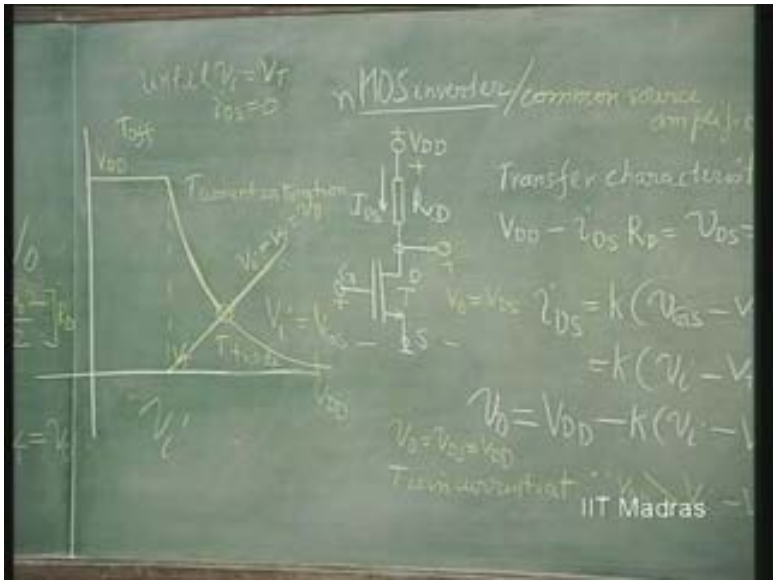

Or, we can operate this anywhere in the region. Let us say, somewhere here. How do I operate it? I will make this as V G S Q – quiescent. This V i is same as V G S. So, I will make this as V G S quiescent. I will apply a D C voltage and then, the signal will vary the V G S around this quiescent in such a manner, the current is going to vary. If this current varies, I D S varies, then, the output voltage is going to vary. Therefore, the slope of this characteristic here on this point, which is, Delta V naught divided by Delta V i. Delta V naught divided by Delta V i is called the gain of the amplifier.

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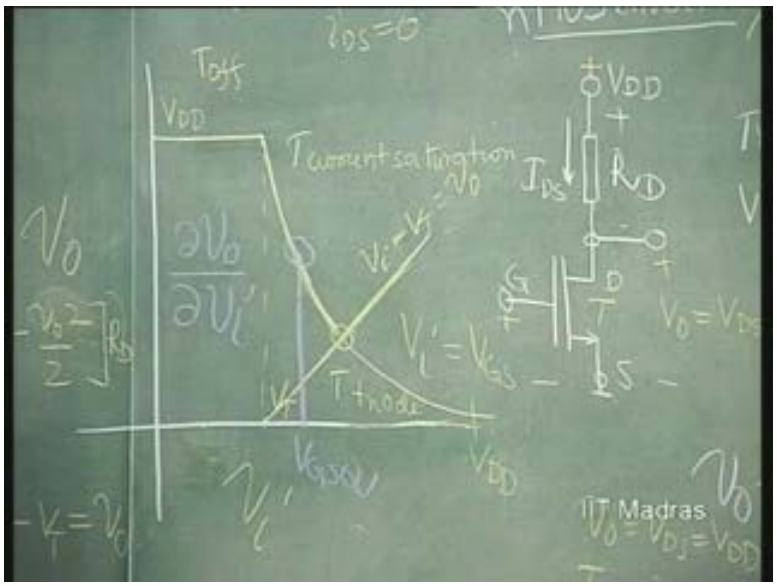

If you take this slope, it is negative here. The slope is negative indicating that this common source amplifier is inverting, giving a phase shift of 180 degree; and the magnitude of this slope will give you the amplification factor. What is it?

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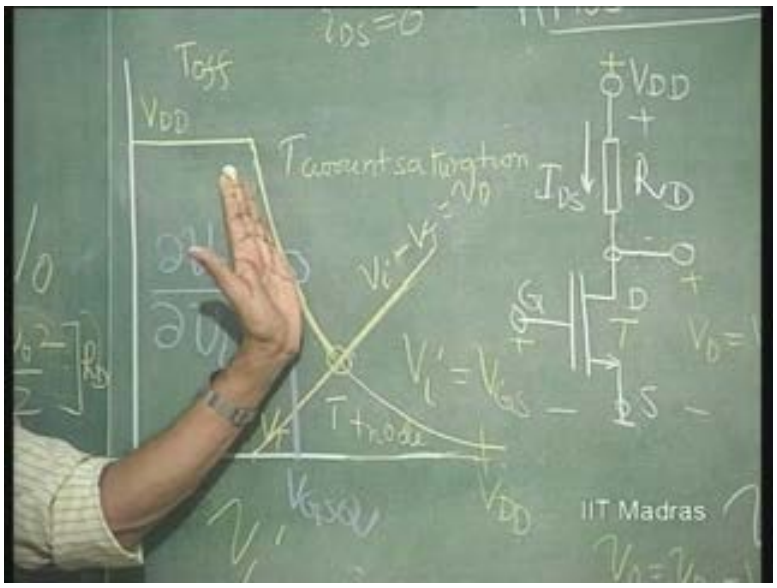

Therefore, that can be obtained by differentiating this equation. So, please differentiate this equation.

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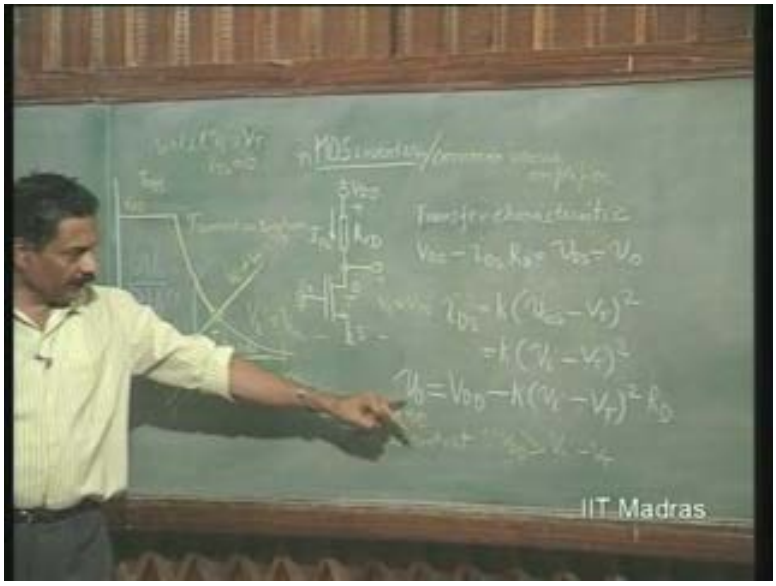

Not this, because this is not the active region.

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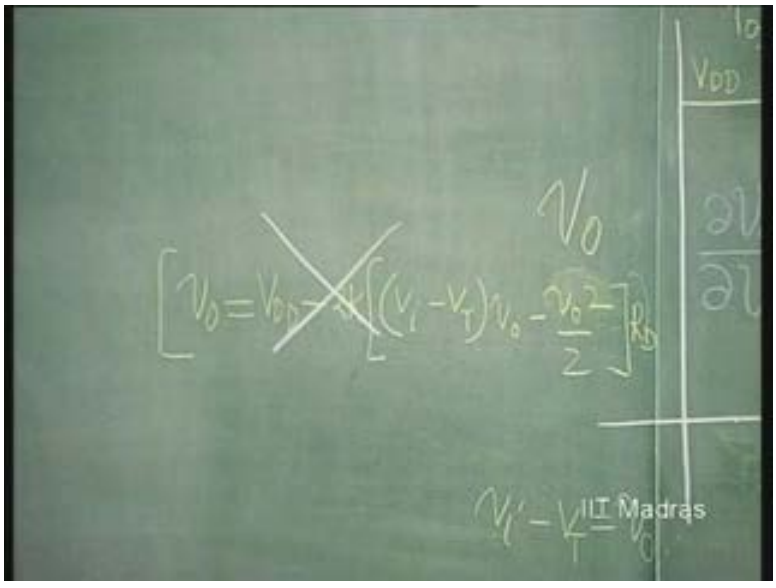

So, the amplifier is set to enter the saturation region here. The amplifier is set to enter the saturation region where the FET is entering the triode region. The amplifier again goes to the limit here where the FET is in off state. These are the two boundaries within which you have to operate the FET in order to keep it as an active device.

So, let us now obtain Delta V naught by Delta V i for this. It is nothing but... Please differentiate that. What do you get? Nothing here. So, minus, minus 2 K into V i minus V T into R D. So, this is nothing but the gain of this. This is also written as minus, what is this factor? So, this is nothing but... After all, this is the I D S. This factor is nothing but I D S. So, because, this is really speaking, V D D minus I D S R d. So, if I differentiate this, actually speaking, you should get minus R D into Delta i D S by Delta V i. Because, R D is a constant.

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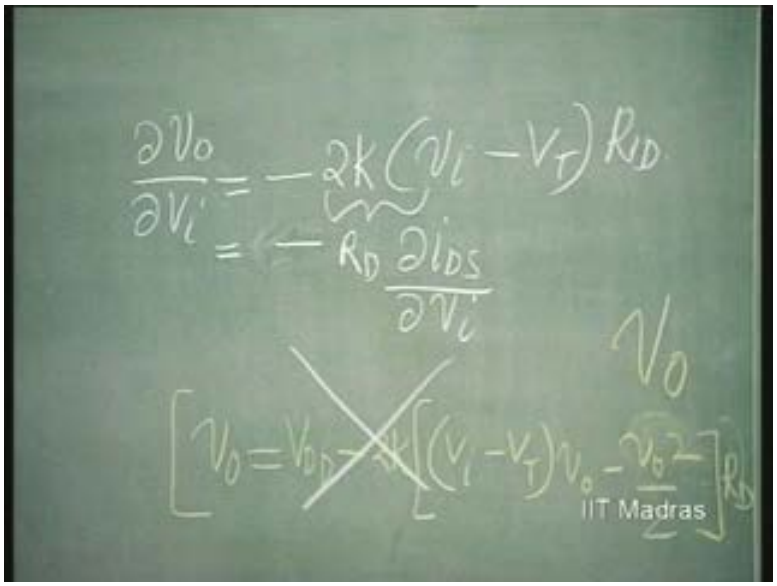

Only thing I can differentiate here with respect to V i is I D S. So, Delta i D S by Delta V i. What is Delta V i? The same as Delta V G S. V i is same as V G S. So, this Delta I D S by Delta V G S is called... output current variation for an input voltage variation; it is called transconductance. Its magnitude is conductance. It is from input to output that the change has occurred; for an input voltage variation, what the current variation at the

output is. So, this is called the transconductance. So, the gain therefore, this is also indicated by g m. So, this factor is called transconductance.

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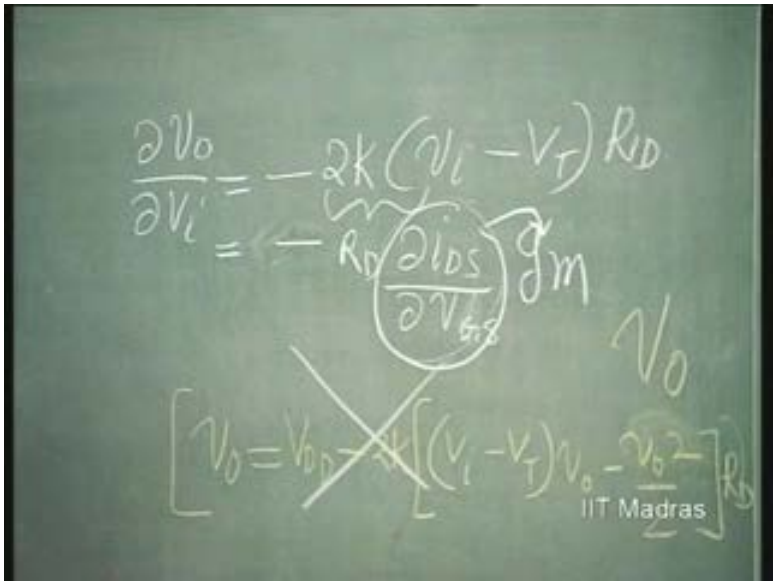

So, this is equal to minus R D into g m. So, please remember that the same expression has been obtained in the case of bipolar junction transistor. There also, the gain was minus g m into R C. In the case of FET also the gain is minus g m into R D. And therefore, these are all exactly identical in their definitions.

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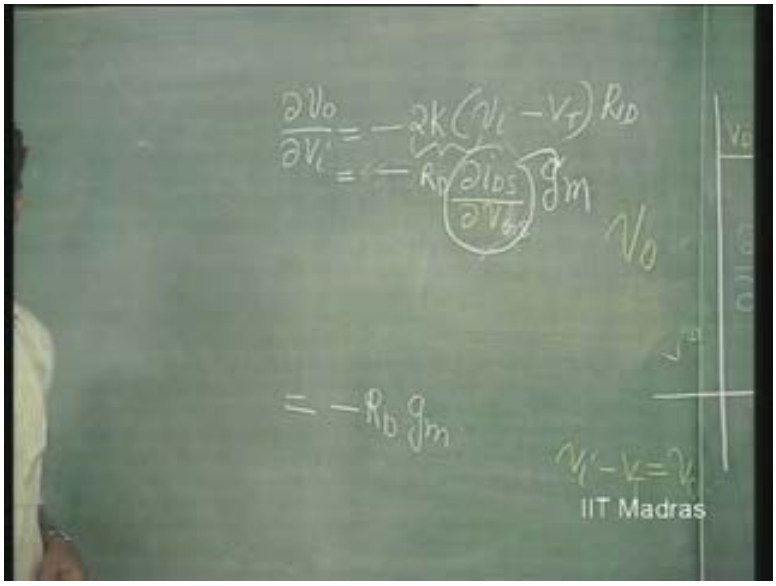

So, you should therefore know, how one should obtain g m. The value of g m is nothing but minus, not minus, 2 K into what? V G S minus V T. What is V G S minus V T? This can be written as 2 K. V G S minus V T is root of I D S, because,... divided by K. So, this is 2 K into root of I D S by K. So, this is nothing but 2 root of K into... Is this clear? Because this I D S is nothing but K times V G S minus V T. This has to be evaluated at a certain operating point at V G S Q. That is the slope. So, I D S is equal to K times V G S Q minus V T whole square. So, V G S Q minus V T is nothing but root of I D S by K. So, you substitute this. This is the value of ...

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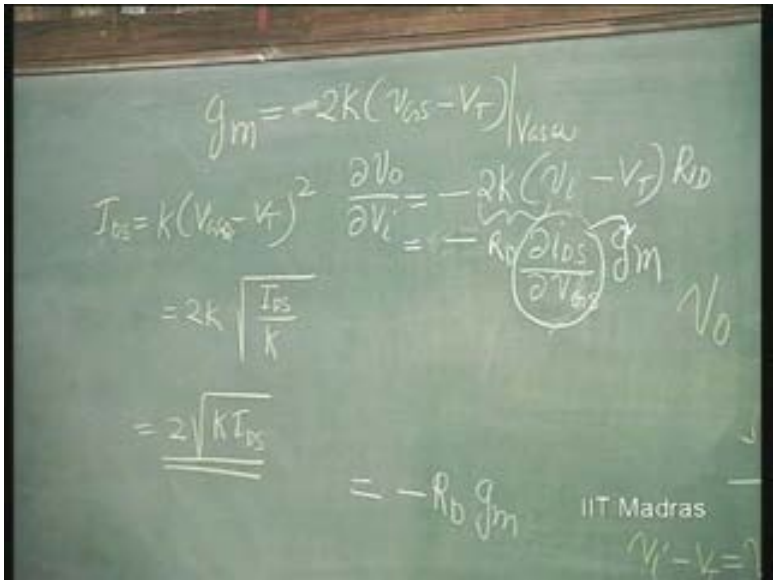

Therefore, if you know the value of K and operating current, 2 root K into I D S will give you the value of g m for FETs of similar dimension compared to the BJT. The value of g m is typically one order of magnitude less than that of corresponding bipolar junction transistor. For example, a bipolar junction transistor at 1 milliampere; if it has 40 millisiemens as g m, then, corresponding g m for the FET is going to be about 4 millisiemens.

So, this is why, if it is an amplifier that you are designing, it is advantageous to go for bipolar junction transistors rather than field effect transistors because, for the same dimension, it is going to offer an order of magnitude, better g m, transconductance; and therefore, it is better to go for bipolar junction transistor.

So, let us now consider what is meant by distortion, which we had already discussed in the case of bipolar junction transistor amplifiers. If you consider that V i is V p sine omega t, this is sine wave, we will now have V naught equal to V D D minus K times V p... Now, we should say V i, if we make V p sine omega t, we have a problem. We should have this superimposed over V G S Q so that there is a quiescent; so that this voltage can go to positive and negative around this point. You can increase above V G S Q or

decrease. So, we have V i is equal to V G S Q plus V p sine omega t. And therefore, V D D minus K times V p sine omega t plus V G S Q, D C voltage biased, minus V T whole square. So, do what you get here? V D D minus...

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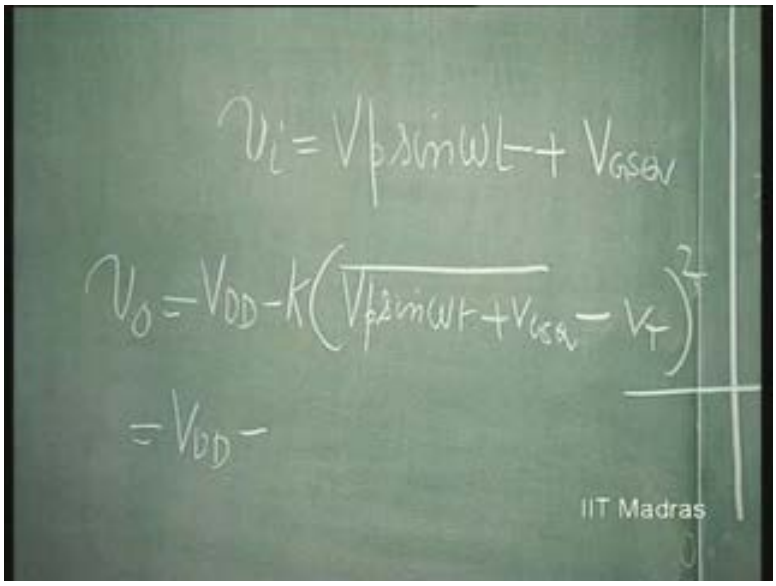

We will now couple this on like this. This is nothing but V G S, time varying V G S; but this is V G S Q, D C, minus this is another D C. So, V G S Q minus V T is a D C. V G S Q has to be necessarily greater than V T in order to locate it in the active region. So, this is a positive quantity. V G S Q minus V T is a positive quantity for this n channel device. So, this therefore can be put as a constant. So, we have this K times, square this, V T square sine square omega T, plus V G S Q minus V T whole square, plus what? - 2 V p sine omega t into V G S Q minus V T.

So, this whole thing into R D.

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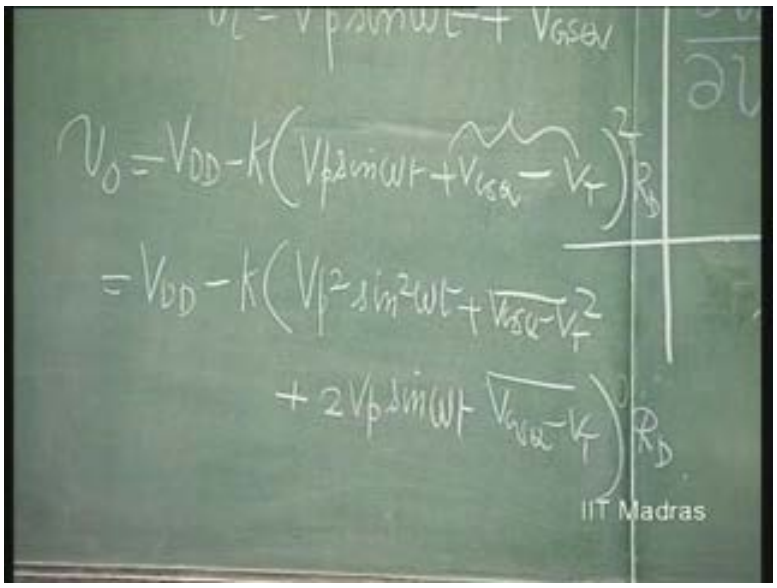

So, that is the output voltage. Now, let us see. V naught is therefore going to be equal to V D D; it is a D C; minus K times V G S Q minus V T whole square. What is this? This whole thing; because, this V D D minus K times V G S Q minus V T whole squared, which is nothing but, I D S Q; this into R D. So, strictly speaking, this whole thing is nothing but, what is called as, V D S Q, quiescent operating point of the FET.

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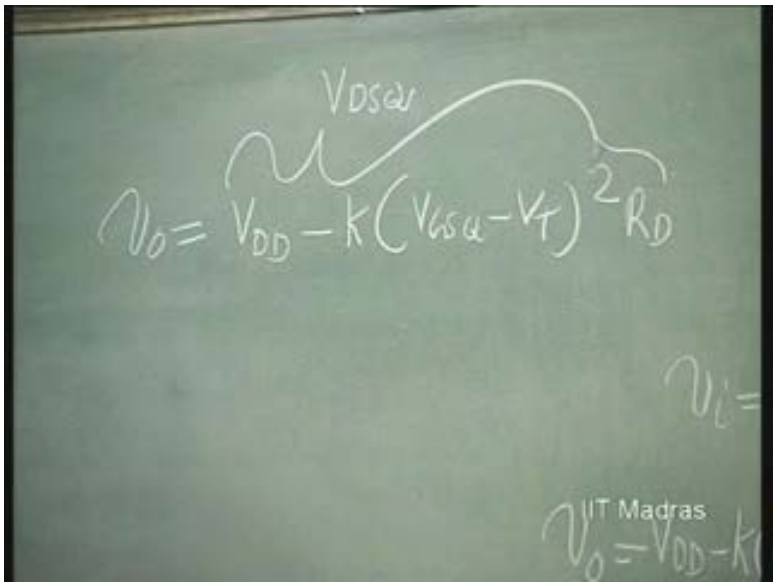

V D D minus K times V G S Q minus V T whole square into R D, is nothing but I D S Q into R D, which is V D S Q, D C voltage. So, that minus... let us take the useful component here; K times R D times 2 V p sine omega t, which is the linear term; because we had applied only sine omega t. We would like this to be amplified and appear as a sine omega t term.

So, this is the wanted component sine omega t into what V G S Q minus V T; so, that into R D – we have already taken into account – minus, unwanted component. This is what is causing distortion. This is called the non-linear term in our FET amplifier. So, we have this as K times V p square into R D sine squared omega t. So, this is the non-linear term; this is the linear term.

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We have noticed this. This is nothing but 2 K into V G S Q minus V T. What is that? 2 K into V G S Q minus V T is nothing but g m. We looked at it. So, this is nothing but 2 K into V G S Q minus V T, which is nothing but what we have already defined as g m. So, we will replace this. So, we have already defined – g m into R D is the gain; that into original input signal which is V p sine omega t with a minus sign indicating that is an inversion.

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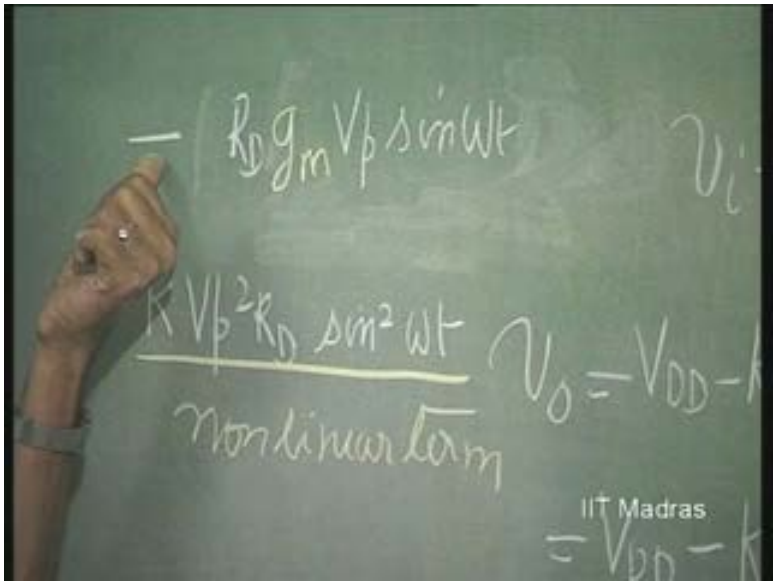

Next, we have K, minus K times V p square R D sine square omega t. Sine square omega t can be expanded as what? 1 minus what? – cos 2 omega t by 2. So, you can see that this non-linear term is contributing to a second harmonic distortion.

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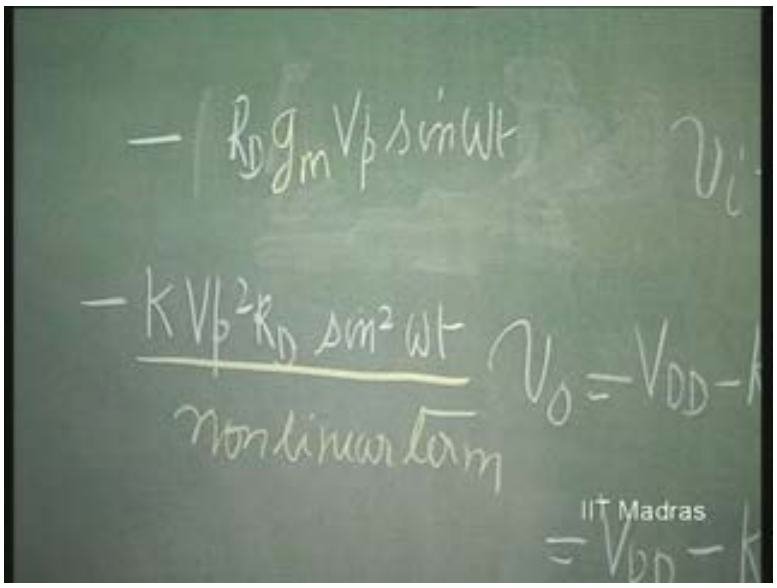

So predominantly, in a field effect transistor circuit, you do not have other higher harmonics; but they are predominantly second harmonic components which are present,

causing distortion. And the extent of second harmonic, you can learn, by how? By seeing that there is a D C term caused by the same thing. The amplitude of the second harmonic is the same as the D C term which comes over and above the quiescent voltage. Let us say, before you apply the input signal, there is a quiescent voltage which is called V D S Q. Measure this using a D C meter. Then, apply a sine wave and measure the shift in the D C output. That shift in the D C output will give you the amplitude of second harmonic.

This is the technique I advise you to use even for measuring the distortion in the case of a bipolar junction transistor amplifier. So, you can quickly measure the extent of this experimentally by finding out the shift in D C, which is minus K V p square R D by 2. So, this is something that you can, in an experiment, do very easily and find out what the second harmonic distortion is. If you are told that keep the amplifier second harmonic distortion less than 1 percent, then, this divided by this has to be kept less than what? – 1 percent. This divided by this should be 1 over 100, point zero 1.

So, this is something that you can always do in design. Suppose you are asked to design a FET amplifier for an output distortion less than 1 percent. Then, you can also find out what should be the value of V p; what should be the limiting value of V p to retain the distortion at less than 1 percent, because this is V p square, and if you divide it by this, one V p will still be there. The distortion obviously depends upon V p.

So, it will tell you the magnitude of V p that should be constrained in order to keep the distortion at a value less than 1 percent. So, this part of the design is important in restricting the design, this thing, what is that? – inputs, to specific values. So, what is it? We can just see, K V p square into R D by 2 divided by R D g m into V p. So actually, g m itself is defined as 2 K into V G S Q minus V T.

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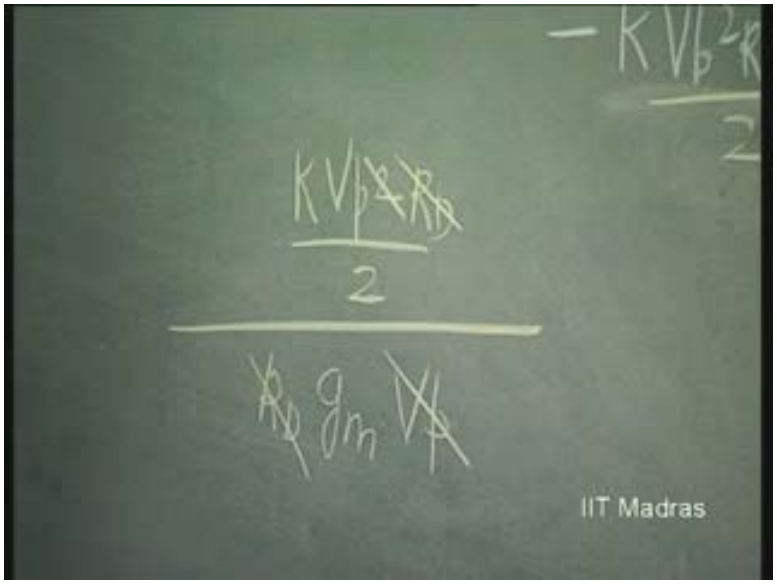

So, you can therefore get the extent of distortion using this. We measure the input signal in terms of V T. In the case of bipolar junction transistor, here, you are going to do it using this K, the parameter associated with... So please see; this g m is, really speaking, equal to what? 2 K into V G S Q minus V T. So, K gets cancelled with this. So, distortion is really V p divided by 4 times V G S Q minus V T.

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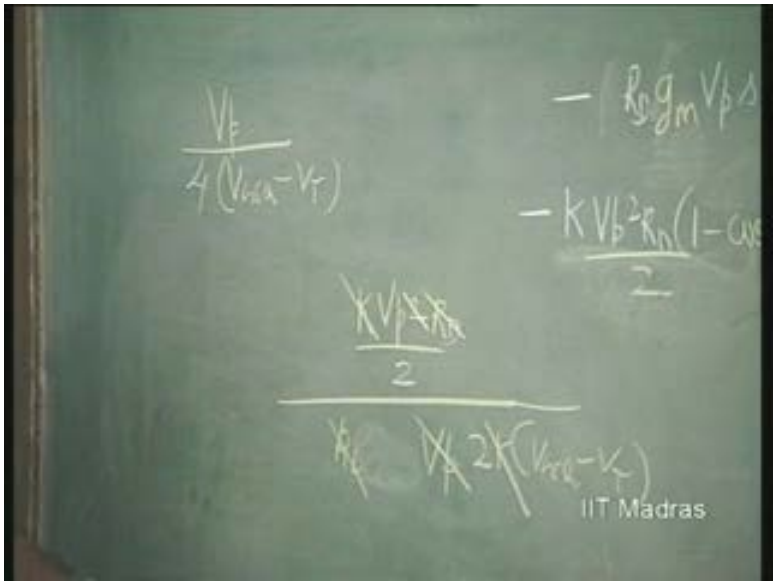

If this is therefore to be kept at much less than 1 percent, that means 1 over 100, then, you can find out what V p should be. V p should be much less than 4 times V G S Q minus V T divided by 100.

So, let us take, V T is 1 volt, you take. V G S Q is, let us say, 2 volts. So, 2 minus 1 volt, 1 volt by 25; 1 by 25 volts, which is 1000 by 25. Or, it should be kept at less than, much less than, 40 millivolts; or, much less than 40 millivolts means, typically of the order of 4 millivolts or so.

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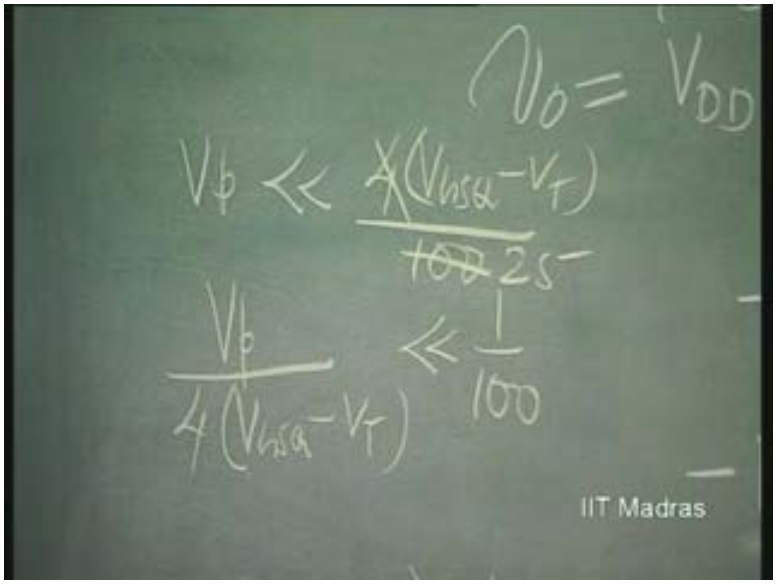

So, this is a classic example as to how you should restrict the distortion.

So, we will consider the other amplifiers in the next class.