Electronics for Analog Signal Processing - I
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Lecture – 27
Construction of a MOSFET

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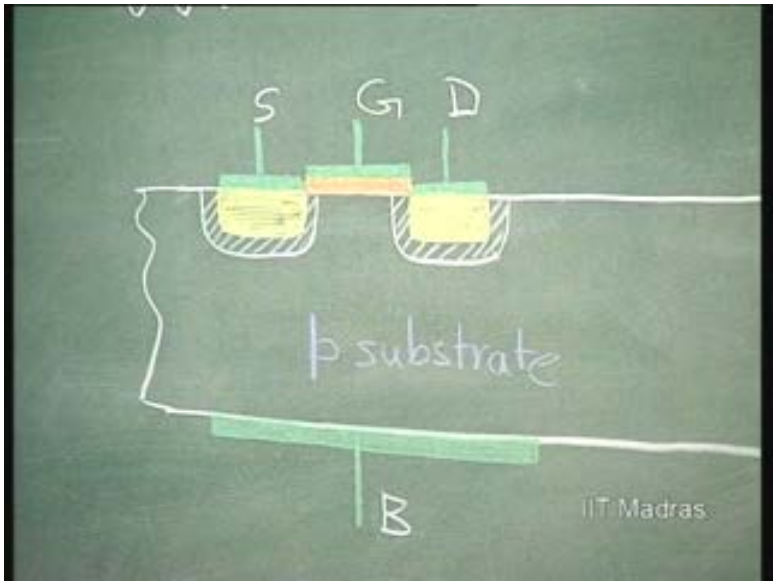

In the last class, we saw something about MOSFET and its characteristics. We started with a wafer; this kind of thing is called a wafer, may be hundreds of microns thick it is. We start with, let us say, p type wafer, p type substrate we call. Whatever is used for the fabrication of ICs, the base is, the base material; that is called substrate. So, p type substrate, we start with, let us say.

Then, we diffuse, we diffuse n type impurity into these; so, these are n regions. These are n regions, n regions. One is source; another is drain. These are isolated because, normally, if it is p type substrate, this is connected to the most negative potential of the circuit. In any IC, if it is starting with p type substrate, the substrate has to be connected to the most negative potential because, all the devices are isolated by a junction, which is substrate and the particular material, where these devices are fabricated.

So, we have a junction here. So, this is always connected to the most negative potential so that when the signal is supplied, under no circumstances will it go ever to positive bias situation. So, the isolation is maintained. So, in this case of a MOSFET, also, the substrate, if it is p substrate, it should be connected to the most negative potential. If it is m substrate you are starting with, it has to be connected to the most positive potential in the circuit, in an IC. So, this is the basis of any design.

So, please remember it because in all these ICs, we have a substrate; and depending upon the type of substrate, we are connecting it either to the most positive potential or most negative potential. If it is n type substrate you are starting with, then it is connected to the most positive potential; if it is p type substrate, it is connected to the most negative potential.

Now, that is, in this particular case, also called body. That is why we call it as B. This is body, this is source, this is gate and this is drain. As I told you, for biasing this to make these devices come into the active region, we need supply voltages; and we would like to make use of minimum number of supply voltages. So, body and substrate, the source, has to be reverse biased. The best way of reverse biasing, of course, is connect zero bias. It does not need any source. Any other biasing will require a voltage source.

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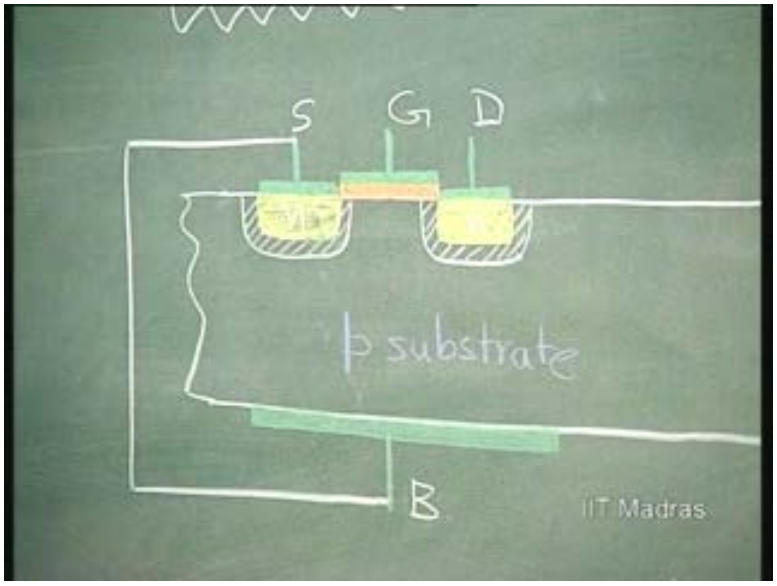

So here, the bulk or the body or the substrate is connected to the source. Now, if you do not want to do it, then, you have to take care that there is a D C potential applied here so that this is negative with respect to the source. That is all that you have. Now, if that is done, we have now three terminals for the MOSFET.

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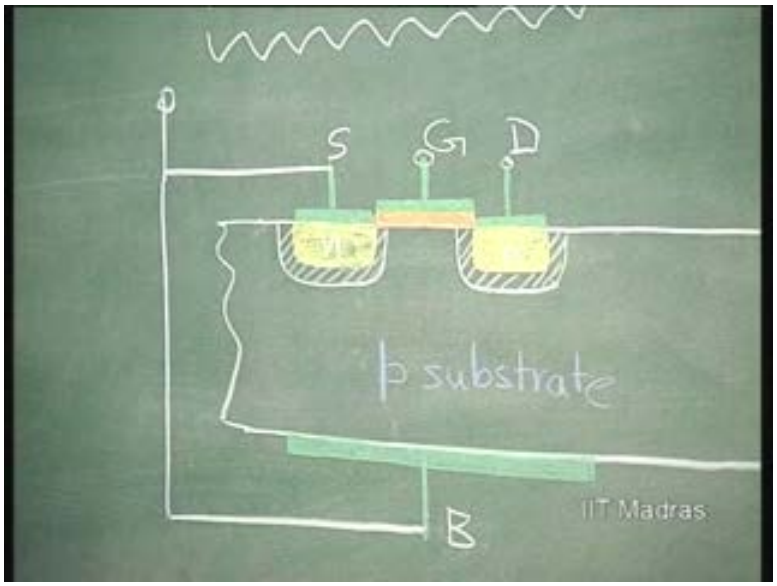

That is why, you have the symbol here. Let us try to understand the symbol for the MOSFET.

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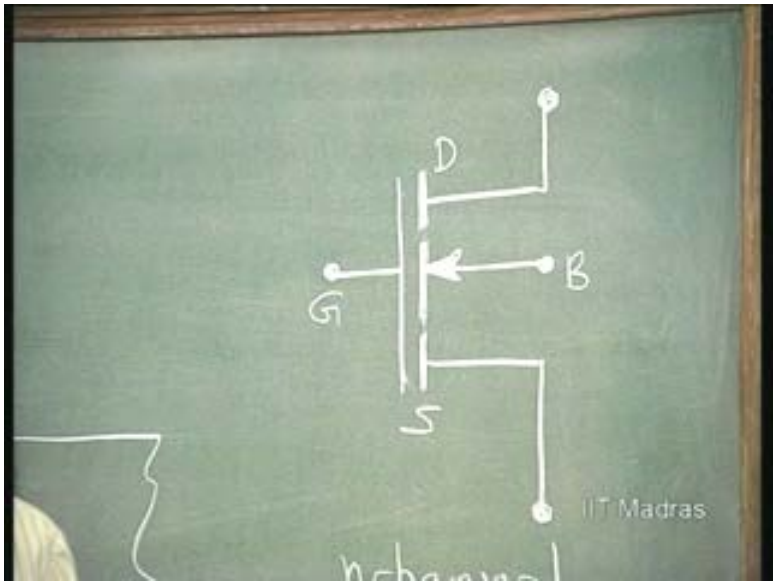

Gate is insulated from the parent material where the channel exits. So, that is the gap. Then we have the source and drain; isolated from this, is this channel. This channel can exist only if I apply a voltage. So, this break indicates that this is an enhancement type. Otherwise, source is not connected to drain normally. So, the break indicates that unless I apply a voltage, the channel cannot be formed. So, this is the symbol.

Now, as far as this arrow is concerned... let us also understand why this arrow has come about. This arrow, as I told you, any symbol in electronics indicates always the actual direction of flow of current; but current need not flow; this actual direction of flow of current, when that particular junction near that is forward biased. But the junction normally may not be forward biased at all. In this case, let us say, this is the bulk or the body or the substrate. So, look at the substrate, it is p; and when this is going to form a channel, it will become n. So, p to n, always, arrow is indicating the actual direction of flow of current, p to n. Whether it is a diode or a transistor, always from p to n, the arrow

is marked. Is this understood? Whether it is a bipolar transistor or a MOSFET or a diode, from p to n always, the direction is, of the arrow is, marked.

So, that will sort of make you remember, how to remember the symbol for each of these. Now, this is a pretty complicated symbol for drawing by a draftsman. It requires patience to break this and all. We do not want to waste time, precious time, in drawing a fairly complex circuit, may be an integrated circuit, VLSI and things like that. So, we do not want to waste our time in taking care to see that it is an enhancement type, therefore, there is a break and all this. For that, a simple symbol is going to be resorted to.

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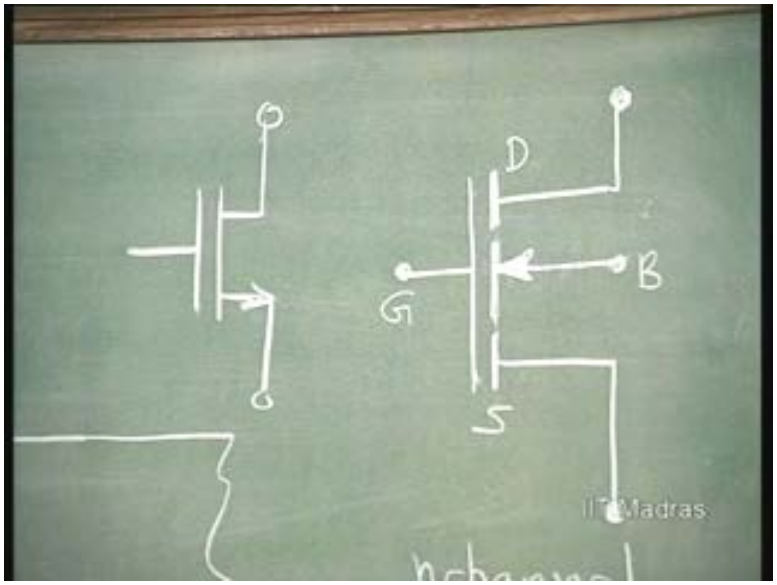

This is the simple symbol adopted for a MOSFET which is n channel enhancement type. Why? Now, if this is connected to positive potential, this also is going to be connected to positive potential for making equal. The current direction will be always this way; and the current direction is always marked at the source end or emitter end.

So, the current direction is indicated here, this way. So, this is the source end. So, indicate the current direction at the source end.

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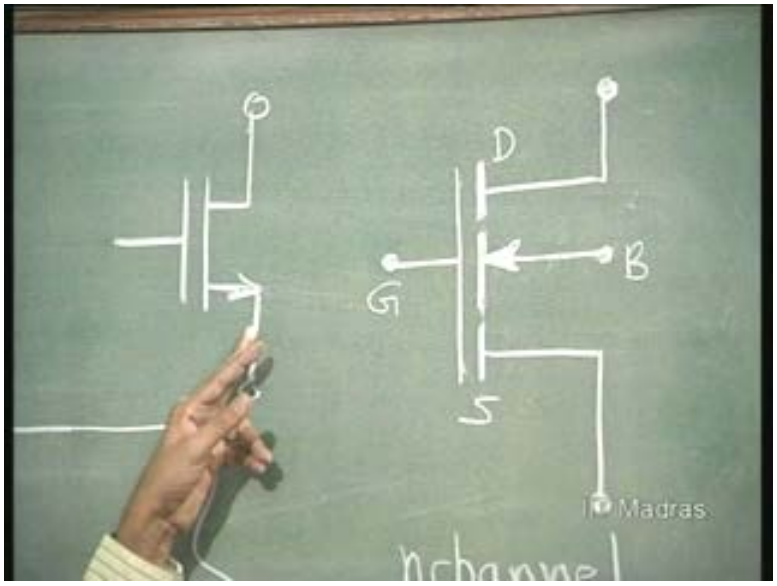

So, all this business about substrate is forgotten there; it is assumed that the substrate is connected to the source and you are shorting this. ((... Refer Slide Time: 9:00)) In fact, this is the simplified symbol for a MOSFET which is now universally adopted. Now obviously, the biasing for making it work is positive with respect to source. We apply a positive voltage here as well as to the drain. Then only, MOSFET action occurs.

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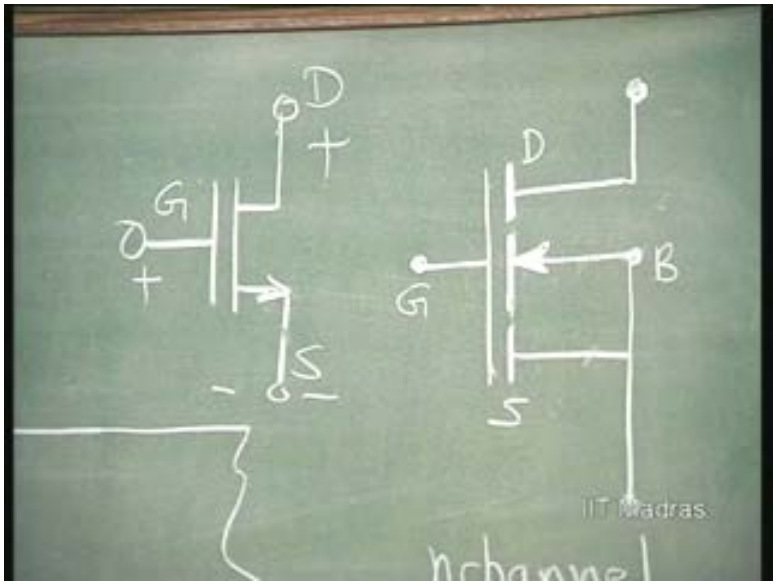

Let us, sort of, briefly review what we understood in the last class, quickly. I told you, there is no connection between source and drain. That means the resistance between the source and drain is infinity, as such. So, that is, a enhancement type of MOSFET is normally, normally open kind of thing. Then, in this sort of, not switch is, if you are using that as a control switch, it is normally open switch; control switch.

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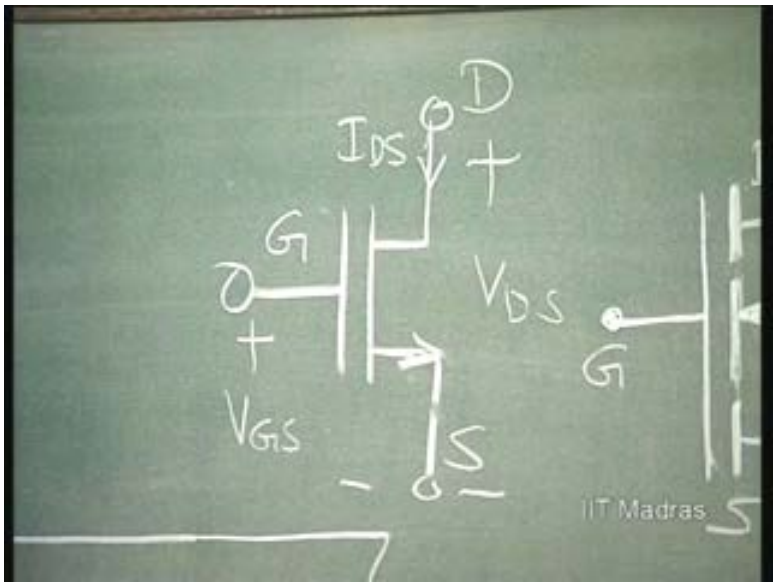

So, if I plot I DS versus V D S... I D S is the current here, versus V D S, voltage V D S, let us see how it looks like. Obviously the resistance is infinity. That means there is no current, whatever be the voltage V D S. So, this is the characteristic curve for V G S equal to zero. So, for V G S equal to zero, this is the curve; no current.

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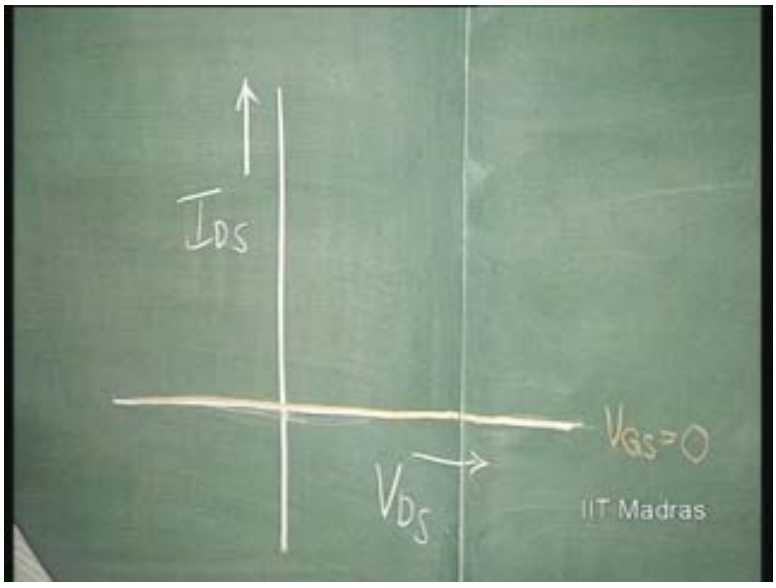

Now, that is because, there is a junction formation here; and even if I apply more V D S, V G S equal to zero, even if I apply more V D S, the depletion layer width keeps on increasing and there is no question of any current. This reverse bias here keeps on increasing and this... Now, when V G S becomes equal to V T, we have defined this as a threshold voltage, which is an important voltage.

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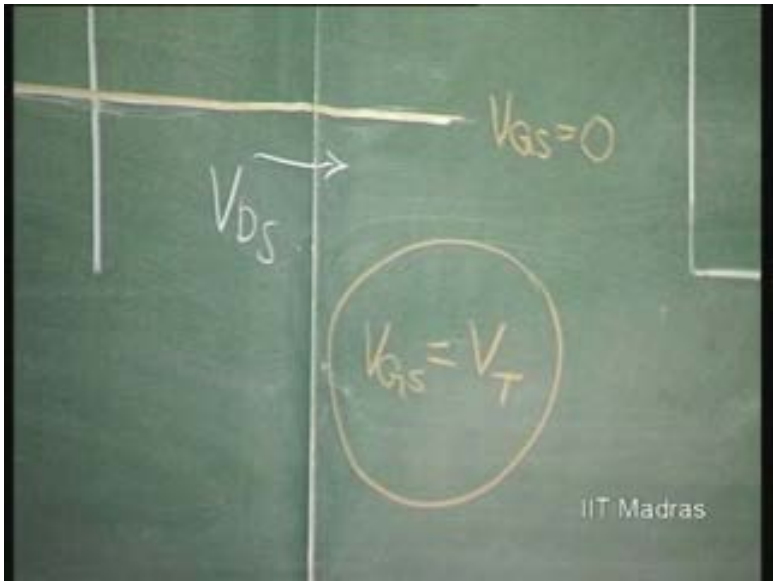

What is that voltage? It is that voltage at which there is... When you apply a certain voltage with respect to the source or the bulk, body, there is a what? – channel form. That is, as I told you, as I apply a positive voltage, the p substrate contains lot of what? – mobile carriers, which are what? – electrons as well as holes. Electrons are the minority carriers; holes are the majority carriers. Electrons tend to come towards the surface; so, and the holes are repelled.

If I apply a positive voltage here, so, this side becomes less p type. Suppose this is p plus; this becomes just p type. The resistivity of the surface increases. This is what first happens. Then, as further positive voltage is applied, you have most of the, say, minority carriers already coming to the surface. Then, you are starting to uncover the immobile atoms which are charge carriers, carrying what charge?

Now, the impurities here donate a hole; therefore, acquire a negative charge. So, that way, the negative charge is uncovered here. That means this region gradually becomes depleted of carriers. And then slowly, you further increase the positive voltage there; then, the surface becomes what? – flooded with minority carriers which are electrons and the type becomes n type. Then you say that there is inversion.

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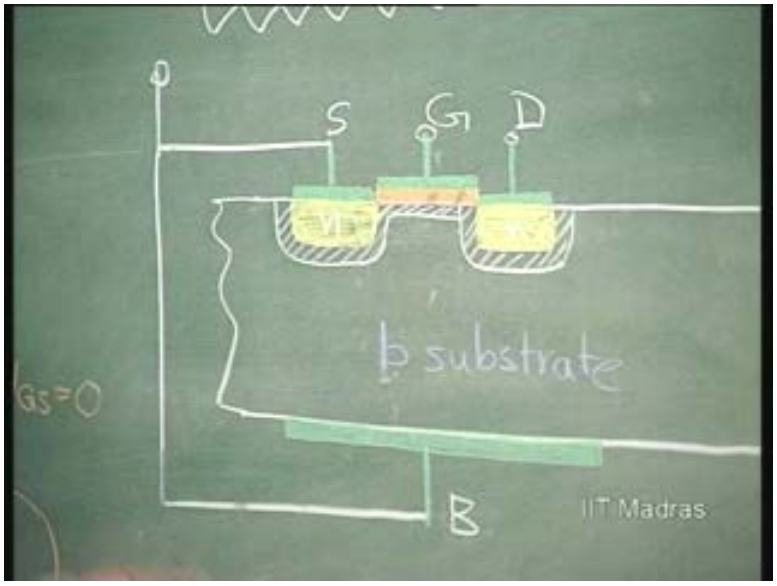

So now, once inversion occurs, a channel is said to be formed and this depletion layer is pushed down. So, this is how the channel gets formed; and the voltage that you apply to the gate to make a substantial amount of current flow, start flowing, is called the threshold voltage.

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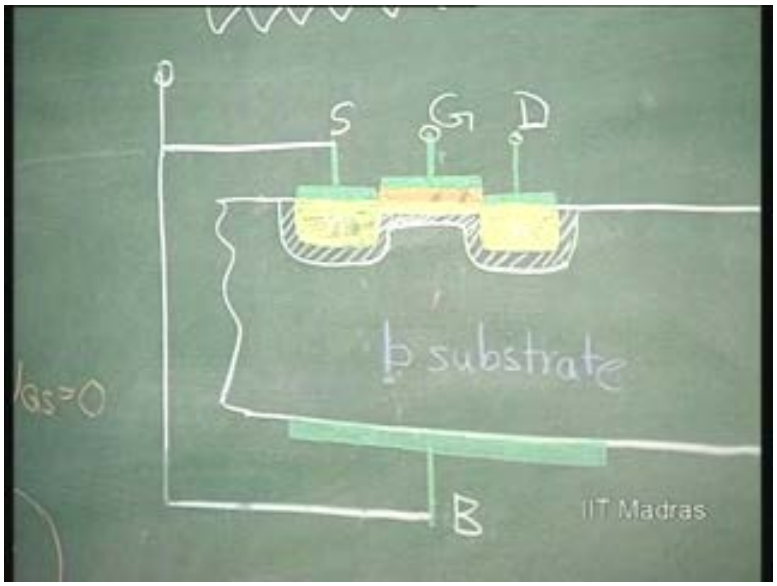

So, when you apply the threshold voltage, the channel is just formed. Let us say, very thin layer. That means the resistance is still very high. Current is going to flow, but very very small. So, current has started flowing. So, for V G S equal to, zero to V G S equal to V T, we have still current flowing here, but very low. That means resistance can be still considered very very high.

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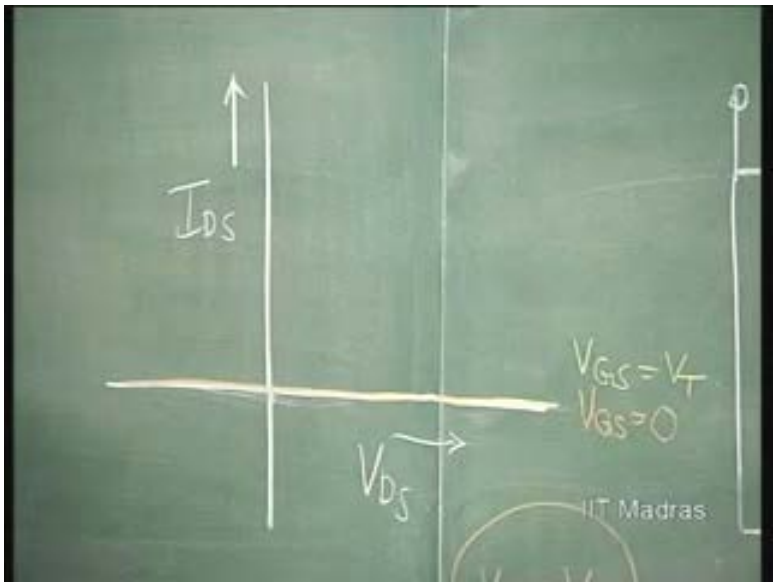

Now, I apply further gate voltage with respect to source, which is greater than V T; that means, additional voltage that I have applied is V G S minus V T, extra, let us say, this is what you have applied. Corresponding to this, the width of this is going to increase. If V G S minus V T is, let us say, 1 volt, there will be certain channel width. If it is 2 volts, the channel width will be more. If it is 3 volts, it will be still enhanced. This is why it is called enhancement type of MOSFET. The channel width can be enhanced by applying suitable voltage to the gate. So, once you enhance the gate, that is, the channel width, let us see what happens.

As long as V D S is still zero, it looks just like a ordinary resistor; the width is uniform throughout. V D S is zero. So, V G S and V G D remain the same; and therefore, the width here is uniform. So, you can treat it as a plain, good old, resistor, of a certain width

in this direction, certain depth here, certain length. So, the width is in this direction. Length, channel length is in this direction, width is in this direction; and there is a certain depth determined by what voltage you are applying, in excess of V T, to the gate.

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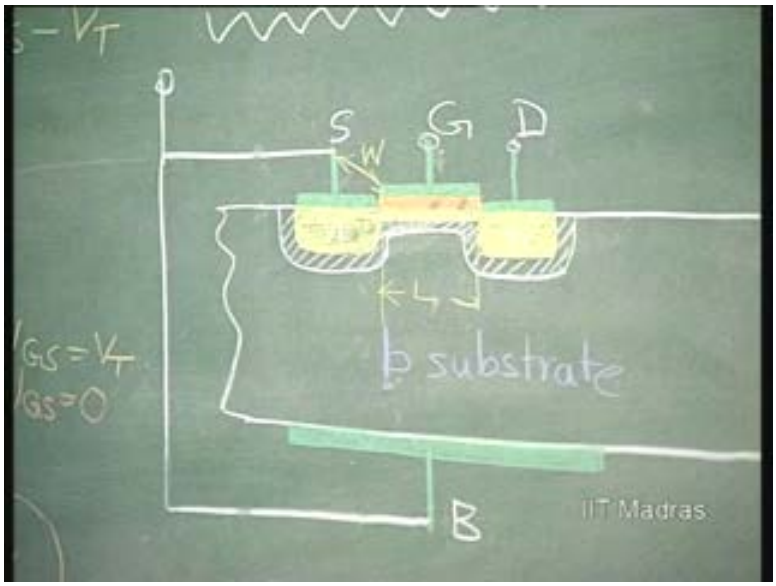

Now, this is crucial in determining the depth here. So, depending upon this, if this magnitude is higher, this depth would be higher. Therefore, what can we conclude about the resistance now? – that the resistance keeps on decreasing, as I try higher and higher value of V G S. The resistance keeps on decreasing. That means, this is really equivalent to, this channel is really equivalent to a resistance. As long as V D S is kept close to zero, this uniformity of this resistance depth can be stuck to. So, I can therefore say that for a certain value of V G S minus V T, this is it, and for a certain other value of V G S minus V T, this is the characteristic.

V G S minus V T, going on increasing. So, this kind of characteristics is what? That is why this MOSFET can be used as a voltage dependent resistor or voltage variable resistor. It is called voltage dependent resistor or voltage variable resistor.

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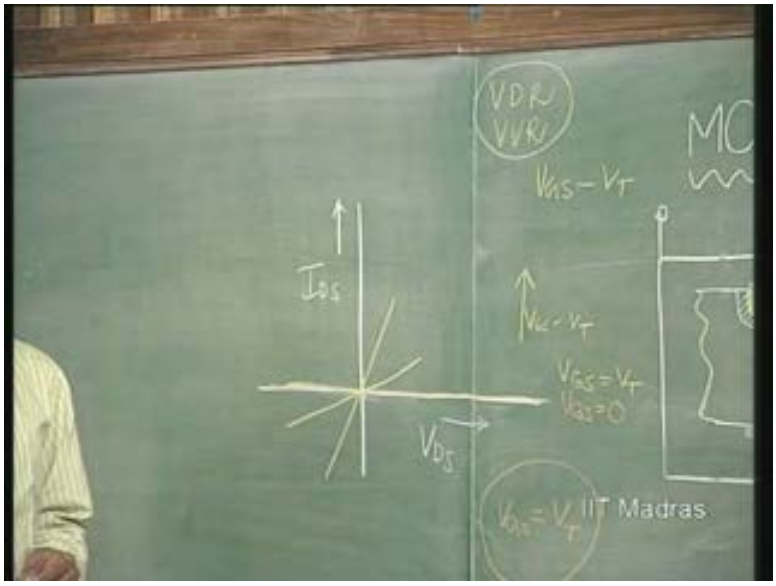

Now obviously, let us look at this channel here. What happens when I connect a voltage like this, V G S, we have discussed. Now, what happens when this voltage is increased?

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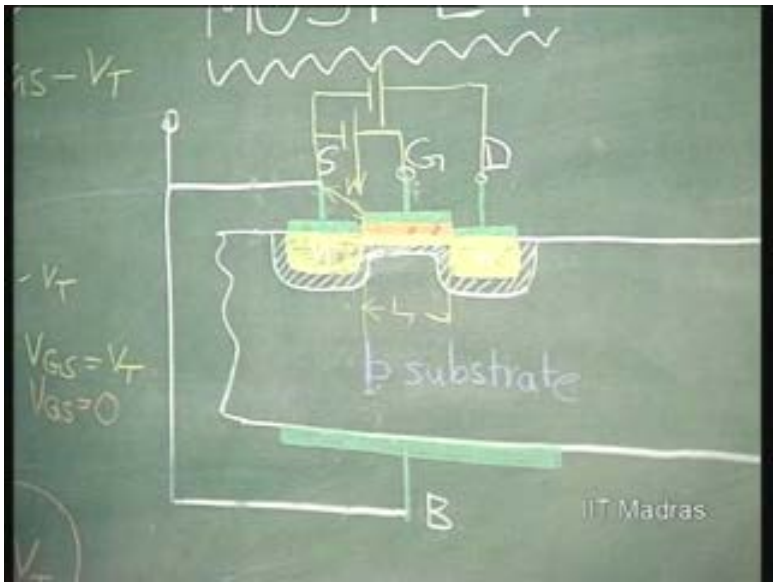

This is V G S and I have been able to open up a channel whose width corresponds to V G S minus V T. Now, the voltage between G and D was same as G and S, when this was

shorted. But now, I am applying a voltage; if you see from G, this is V G S, V G S minus this voltage is what we supply to D. This is opposing this.

So, what should happen to the channel width? It should decrease. At the drain end, it will start decreasing as I start increasing my value of V D S. So, because this V D S is opposing V G S in forming the net V D G, the channel width will decrease. What is the value of V D S that I should apply to close the channel? That is same as V G S minus V T in the opposite direction. That point at which the channel gets closed at the drain end is called the pinch off point. The channel is pinched off. So, what happens to the channel?

Let us depict it in a sort of neat manner. Originally, let us say that it was like this. This is the channel. As I apply higher and higher... this is for a certain value of V G S minus V T; let us say, V G S 1 minus V T, we will call it. This is the channel width. This width depends upon this value. Now, as I apply more and more value of V D S, this remains the same; nothing has changed here.

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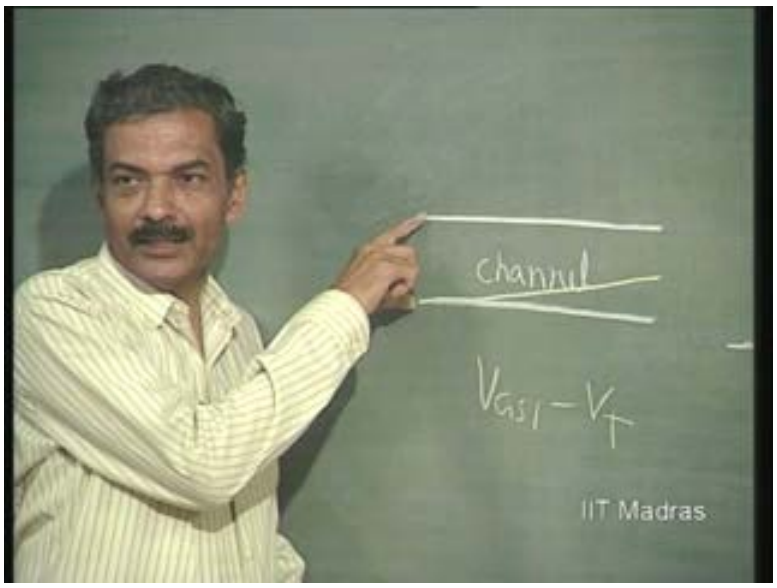

This width corresponds to simply V G S minus V T; whereas, V D G is changing because V D S is increasing. Therefore, this width here, on this side, will decrease. This is what

happens. This is for a certain value of V D S. So, this resistance, strictly speaking, is non-linear because we are plotting I D S versus V D S. The width or the depth of the resistance itself depends upon V D S. So, this is a non-linear resistance.

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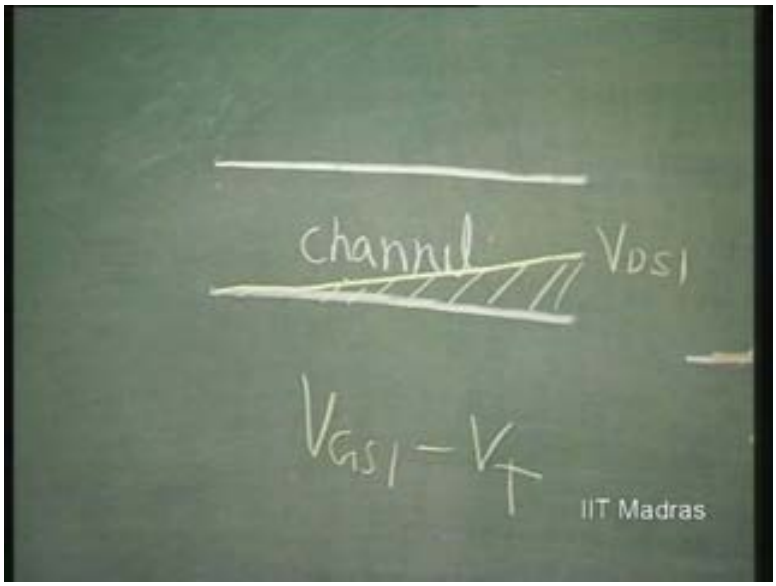

What happens to the resistance, we can understand; because the width uniformly, that is, the depth uniformly decreases. So effectively, the incremental current for an incremental voltage should keep on decreasing. An incremental current, because now it is a non-linear resistance I am talking about; so, an incremental current for an incremental voltage, incremental voltage remaining the same, will keep on decreasing.

That means, for the next portion of the incremental voltage, the incremental current is going to be less. This same voltage if you maintain, this current is going to be lesser than this current and the next current is going to be still less. Ultimately, at the pinch off point, ... What is the pinch off point? V D S equal to V G S 1 minus V T. At this point, V D S equal to V G S 1 minus V T, there is this channel getting completely closed.

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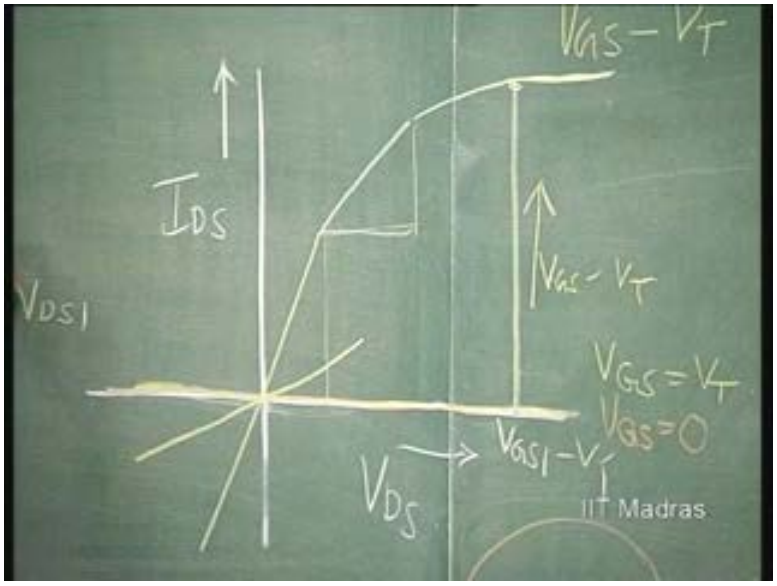

So, we can say that this is the position for V D S equal to V G S 1 minus V T.

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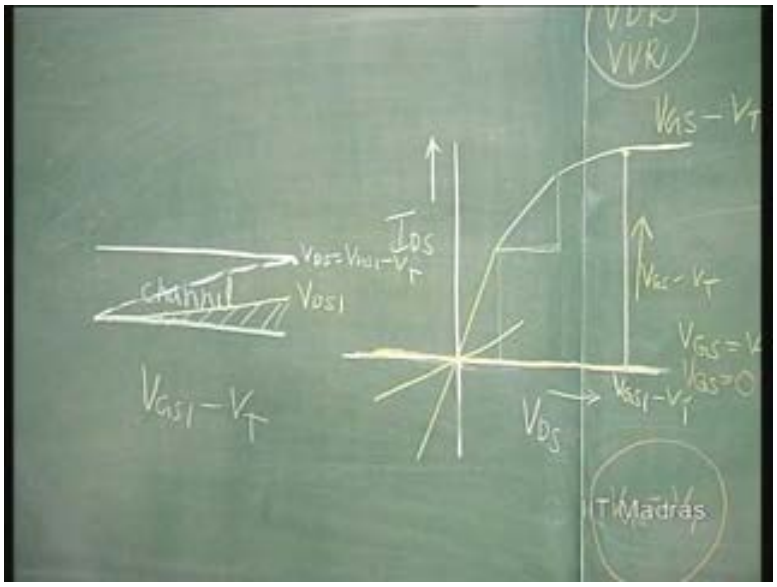

So, current is said to reach its saturation value at this point. For a lower value of V G S minus V T, obviously, the saturation occur at the lower value of V D S. And for V G S equal to V T, saturation occurs at this point itself; and the current is zero.

So, these are all the points at which pinch off occurs. This terminology should be very easily remembered because, that actually depicts what happens at the channel, pinch off.

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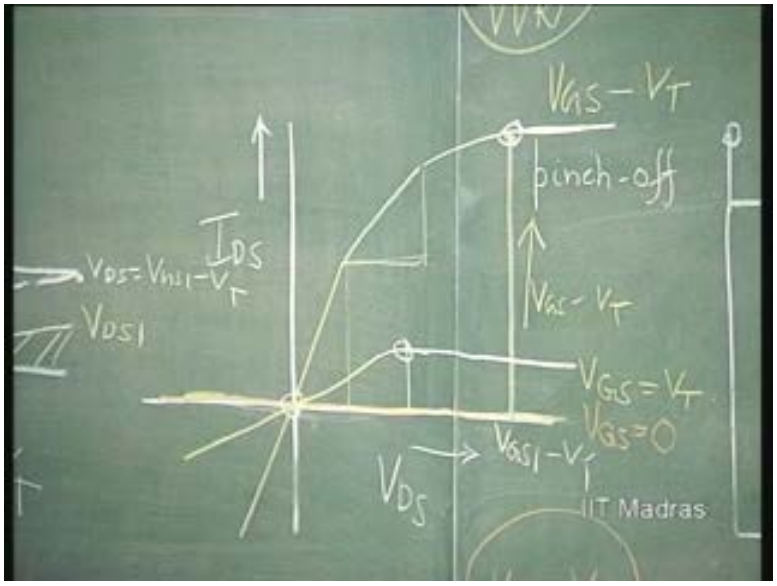

So, this characteristic is understood as FET characteristic and the transistor, FET transistor, field effect transistor, is operated in the current saturation region. This is called current saturation region. This region, we know this region is called triode region. This region, this is called triode region; and this region where the current goes to saturation is called current saturation region.

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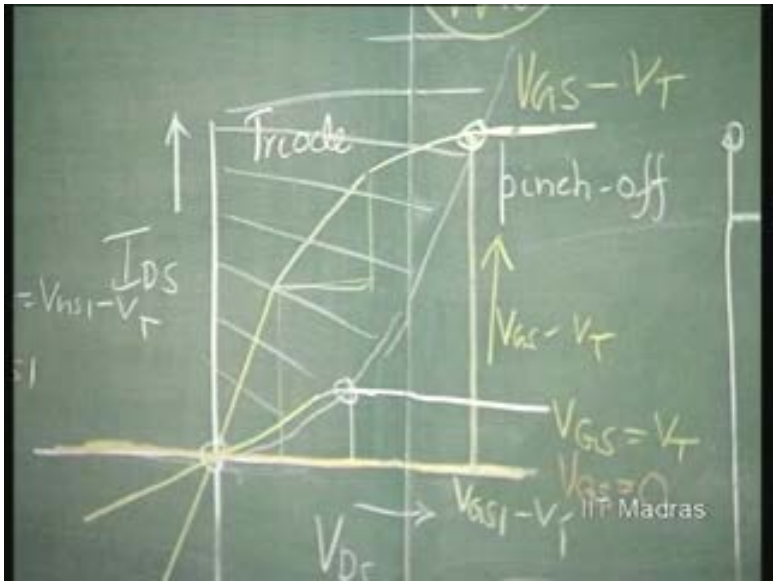

Let us therefore now mathematically indicate what this is. I D S was equal to some proportionality constant; we will put it as 2 K. We will see why that 2 K is put; some proportionality constant. K dash you can call it. The K dash is 2 K; into V D S, sorry, into V G S minus V T. So, it is understood that I D S depends upon V G S minus V T.

Why? Because, the channel width depends upon V G S minus V T. The conductivity increases as V G S minus V T increases; or, resistivity decreases. So, it is dependent upon V G S minus V T. Higher current will be obtained; higher the value of V G S minus V T. So, the proportionality constant depends upon V G S minus V T and it is a resistor; so it is directly proportional to V D S. So, I D S by V D S is equal to 2 K into V G S minus V T. So, this is called defect resistance, R d s.

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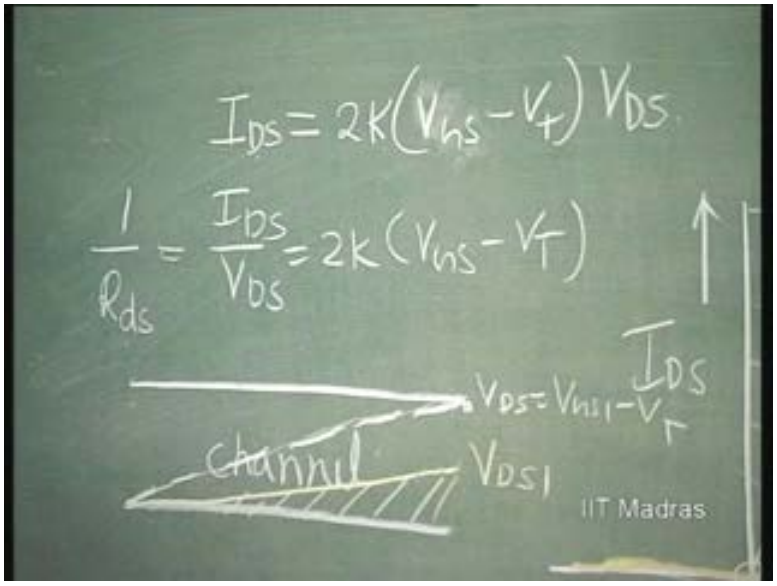

In the triode region, R... actually in the region where it is linear, where the non-linearity has not yet come to picture. Now, in this region therefore is perfectly linear. But thereafter, we have non-linearity setting in. What is that non-linearity? It is called square law non-linearity. That means, some current is going to be reduced; and the reduction is dependent upon square of V D S.

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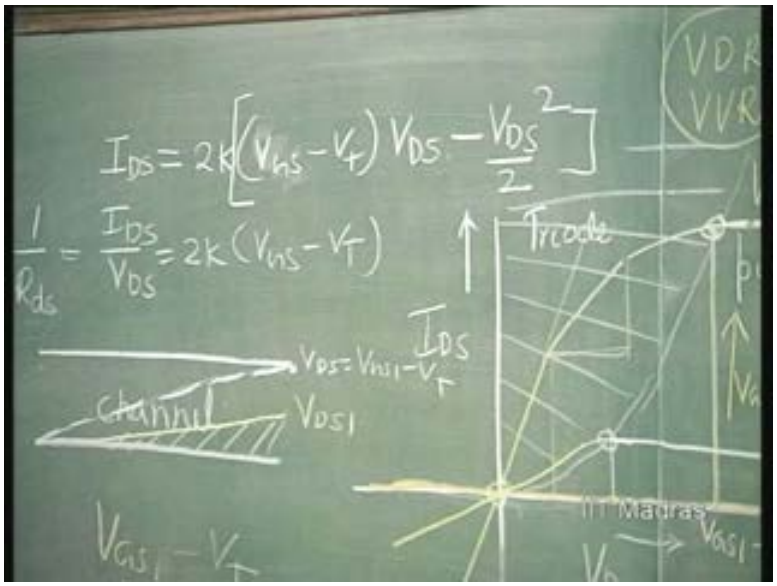

So actually, if you see here, since it is square, so, it is going to be here, adding on to the current; because, V D S changes polarity. V D S square does not change polarity. So here, it is getting reduced; here it is getting added, because V D S square polarity remains the same; V D S polarity has changed here. So, this is the non-linearity that comes into picture. Therefore, this region – it is not suitable; it never goes to saturation. The current never goes to saturation. It is increasing. So, in this region, it is not suitable for FET action, third quadrant. It is suitable for FET action only in the first quadrant.

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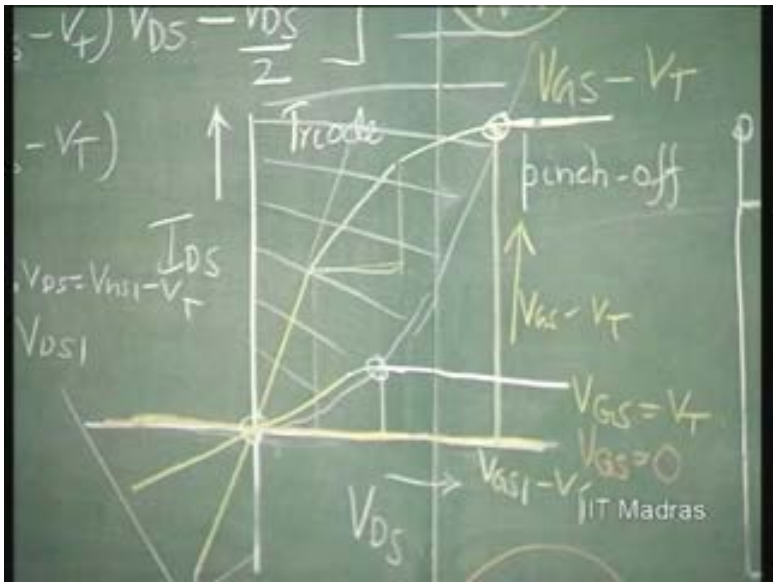

So, that is the non-linearity and therefore it no longer is a linear resistor as depicted here; this formula is not valid because it is non-linear. And, this keeps on happening until we reach the value of V D S, which corresponds to V G S minus V T.

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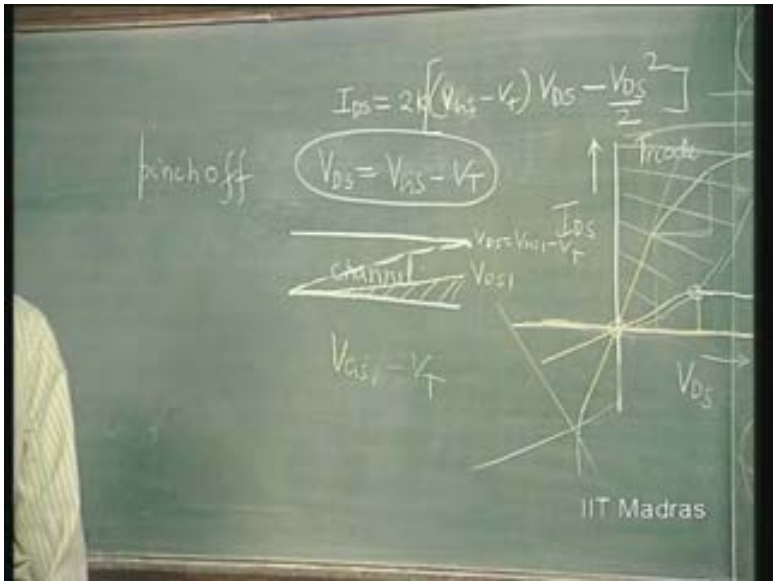

That region is the region of what? – pinch off, where the channel is closed completely; where the current just starts getting saturated. So, you can substitute the value of V D S in this expression. That should give us the value of current saturation. So substitute this – V D S is equal to V G S minus V T. Thereafter, it is independent of V D S; current has reached saturation. What it means is it is remaining same whatever be the value of V D S. So, substitute the value of V D S there, and you get I D S equals K into V G S minus V T whole square.

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So, please remember now, these simple equations which will depict the entire region of operation of the field effect transistor. Simple equations. This is what is called square law equation. K is dependent upon w by l ratio. You know: w is the width of the channel and l is the length of the channel; and the resistance of the channel obviously depends upon w by l. It is directly proportional to w; it is inversely proportional to length.

So, the K is a factor which is dependent upon w by l ratio. Obviously, it depends upon the mobility of the carrier, etc. If it is n channel, it will depend upon the mobility of electrons; if it is p channel, it will depend upon the mobility of holes. More than that, we are not interested in learning, as far as this equation is concerned. So, it is enough if you understand the regions of importance. Once again, this is the triode region, where it is linear and then there is a square law getting subtracted; and at this point, it is pinch off; and beyond pinch off, it is current saturation; it is equal to this.

Now, this is similar to transistor current going to saturation here; but only one difference – that it is not true that this current is really independent of V D S. Just as we had, early effect discussed in the BJT, where this current was still dependent upon V C B, here, we have this current not really independent of this V G S minus V T square into 1 plus, let us say, Lambda times V D S.

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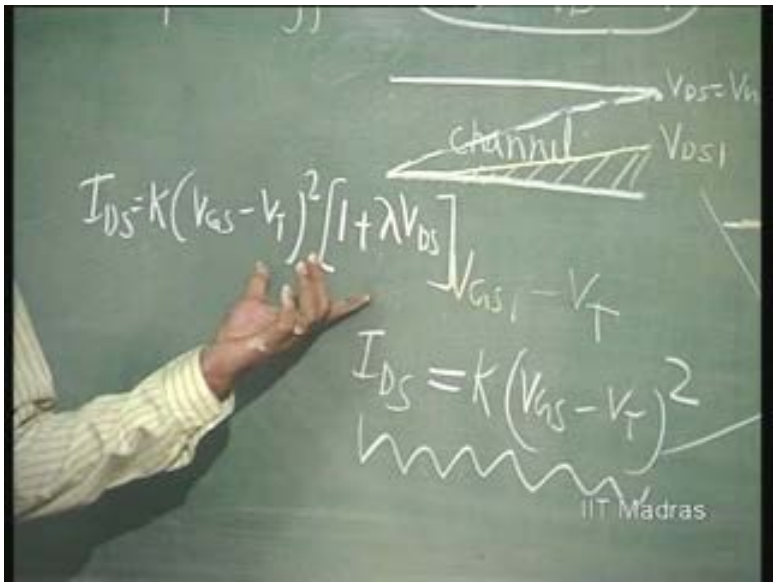

The dimension of Lambda is 1 over voltage; 1 over some voltage. So, this is what really happens in the case of a practical field effect transistor. It is not all that independent. There is certain amount of dependence. It is not going to remain constant at this value of K times V G S minus V T whole square. It is slowly increasing. What again this means is that this dependence is going to sort of, if you extend it, it will get... the intercept will be somewhere on this axis. So, that is what is1over Lambda. If you find out the intercept along this line, it will be corresponding to 1 over Lambda.

So, this characteristic is exactly identical as far as the p channel enhancement type MOSFET is concerned. Let us understand the difference. In the p channel MOSFET, we have to have either n type of substrate. And then, this will be free and this biasing will be negative with respect to source; and this biasing will be again negative here. And

therefore, the threshold voltage itself is going to be negative. The point at which the channel gets on is itself negative. So, except that, the other discussions remain the same. The symbol, obviously this arrow, is going to be in the opposite direction.

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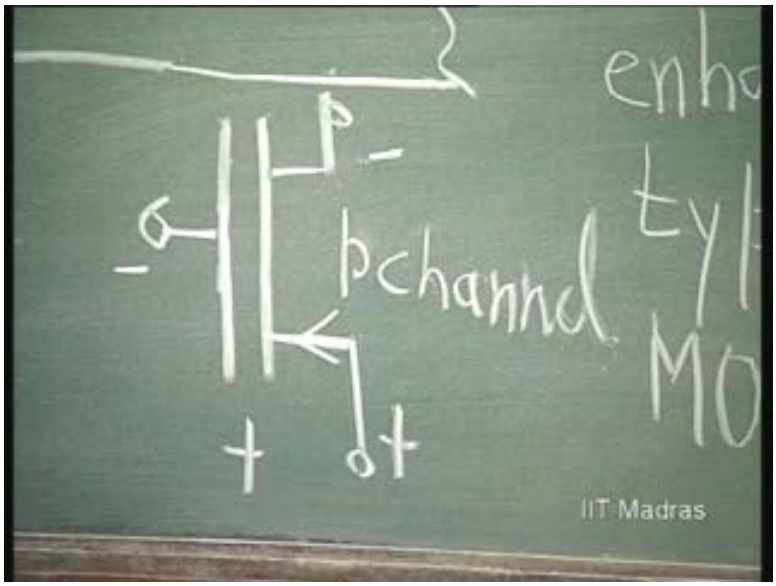

So, negative, negative. So, this is for p channel enhancement type of MOSFET. Of course we can have both n channel and p channel co-existing in an integrated circuit. Let us see. Let us start with p type substrate. Then, these will be n type of source and drain. Then, we have an n channel; and I would like to have, let us say, a p channel FET also in this. Then, I will have an island of this diffused region to formulate a p channel FET in which I will now diffuse into this what? - p type impurities, source and drain.

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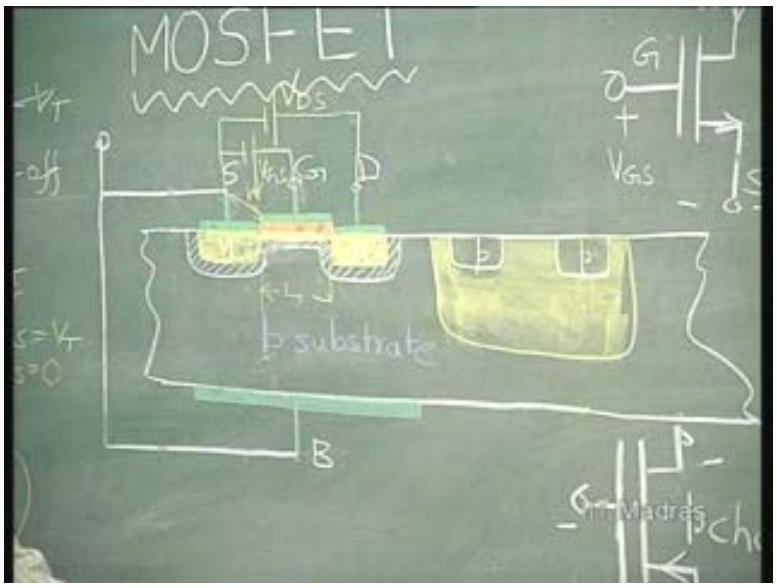

And then, we will have again, similar gate like this. This is silicon oxide, which is also there here as the gate oxide; and then over this, we will have the contact source and the drain contact; and we have the gate contact on this. So now, so we have this n type material here; p type diffusion occurring in this n type material; and we have source, gate and drain. So, in the same wafer, I have what? – n channel MOSFET as well as p channel MOSFET.

This is called CMOS, complementary MOS. This technology of fabrication of this kind of thing is called CMOS technology.

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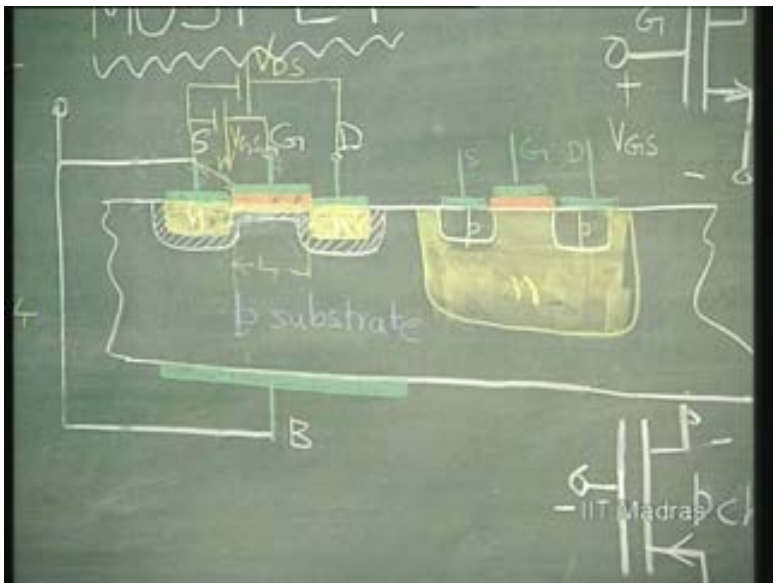

You can have the technology where you do not have this p channel at all. We have only n channel MOSFETs throughout. So, you can have n channel VLSIs or p channel VLSIs or CMOS VLSIs. These are the three different technologies which are available for fabrication of very large scale integrated circuit. Advantage, of course, in the previous one of n channel or p channel is that, the number of steps are less. Here, the number of steps of fabrication are more.

The more the number of steps, the less reliable the system becomes. The more the number of times the human beings start interfering, the less reliable the system becomes. This is always the general truth in any system. So therefore, the reliability depends upon the number of steps. The yield also depends upon the number of steps that you adopt for fabrication. So, most of the VLSI circuits can be either n channel alone being used, NMOS technology or PMOS technology or CMOS technology.

To the same category of field effect transistors belongs another type called junction field effect transistor; Junction Field Effect Transistor, popularly known as JFET. Let us see how it looks like. We have, let us say, the same type of substrate, p type substrate, in which now, we have n type of diffusion done. And then, later on, p type of diffusion done again. And, the second p type diffusion corresponds to the gate. So, the metal contact is placed over the gate. Here we have source, and here we have drain. This is the n channel; this is the n channel. All this is already linked; source and the drain are already connected. So this type of FET is called depletion type of FET because there is already a channel; you can close it only by depleting carriers from this or actually extending the depletion region further into the channel.

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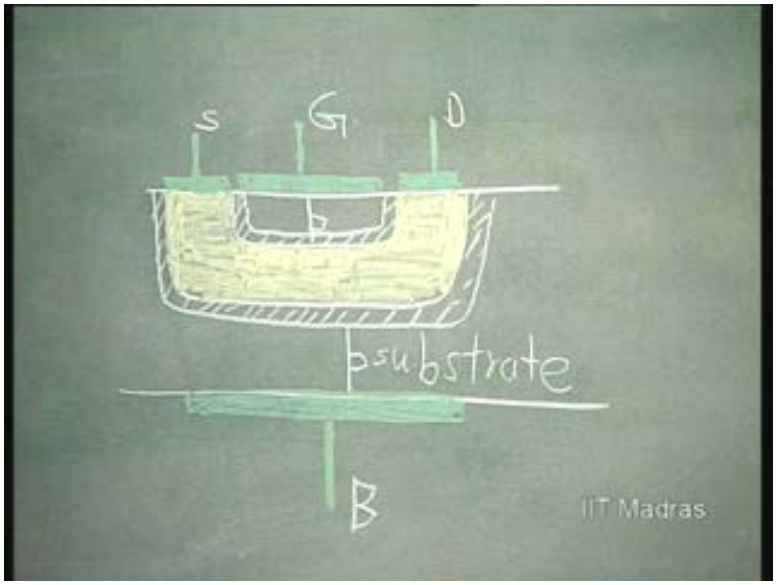

So, the source and drain is already connected unlike the other FET which is called enhancement type of MOSFET where source and drain were not connected. They could be connected by only by applying a voltage. Here, it is already existing. This is a resistance, a plane resistance. Between source and drain, there is a certain amount of resistance depending upon the doping of this n channel.

Now, how do we really sort of make this a field effect transistor? Obviously, by pinching off. So, please remember; this pinching off is the characteristic of a field effect transistor to work in the active region.

So now, let us say, here for V G S equal to zero, the channel width, that is, the depth is going to be this much. Let us assume that this is the channel length and there is a certain width here. The depth here is going to be fixed by the extent of reverse bias applied between gate and this source. If V G S is zero, that is going to be a normal depth. That means this particular thing is going to be applied on resistor for V G S equal to zero. Then, once I start applying I DS, V D S, what should I do? In order to close this channel width here, I have to extend this depletion layer width here.

So, please remember. This is n and let us say, this is... we are starting with... how do we reverse bias this junction. This is a junction here, which is important, which should be always kept reverse biased so that, the gate does not start conducting. Gate is p type and source is n type. So, if I apply a positive voltage here with respect to this, this will start conducting. That means this ((... Refer Slide Time: 43:50) should be biased in the opposite direction, so that, initially there is no gate current at all.

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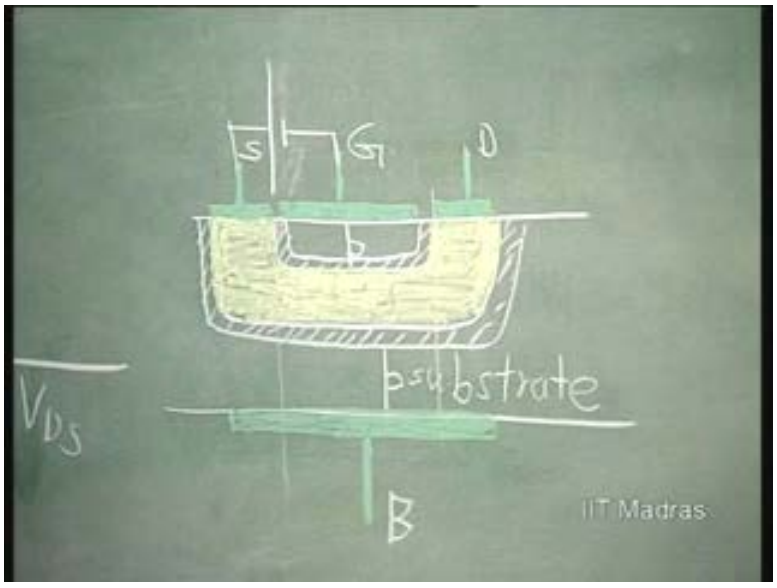

So, please remember: for the same n channel MOSFET, we have to bias it with positive voltage. That is because we wanted to cause a channel to exist. Here, the channel is already existing. So, in this particular case, as far as gate is concerned, it must be always reverse biased with respect to this source so that the gate current is not drawn. There, there was no problem; gate was insulated from the channel by a silicon oxide layer. We could bias it, positively or negatively, strictly speaking. No current was going to flow.

Only thing is, in order to cause MOSFET action, we had to bias it with positive voltage in the case of n channel. So, this is the kind of voltage. If I apply more voltage, this depletion layer width will increase and the channel width will decrease. That means, the more reverse bias voltage... that means, this is made more negative, then, we have this going like this.

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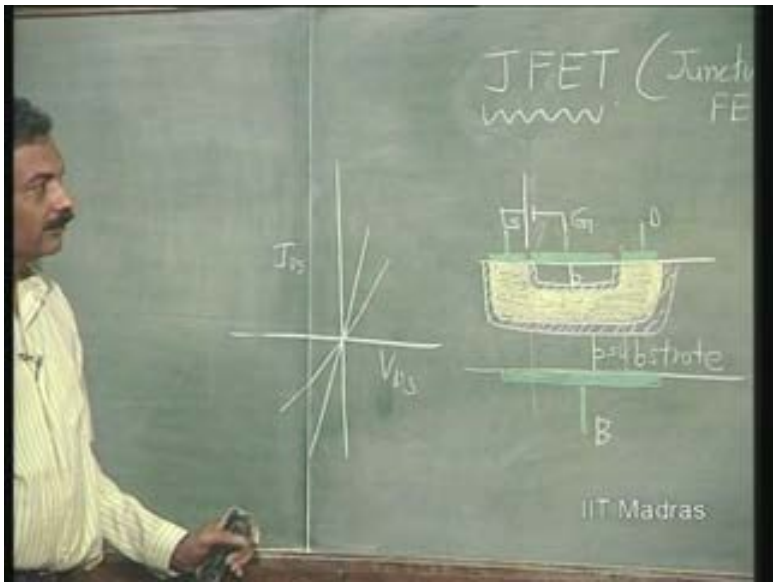

So, this depletion layer width is going to increase and channel width is going to decrease; which means, there is a specific voltage at which the depletion layer width will cover the entire channel and that is called the what? We have already defined. Whenever the depletion layer width covers the entire channel, that voltage is called the pinch off voltage. So here, the only voltage that is important is the pinch off voltage. So, since the

channel already exists, the voltage that you applied to the gate for closing the channel is called the pinch off voltage. That means, at this particular point, you are applying a V G S which corresponds to a magnitude equal to the pinch off voltage. This corresponds to that. That is, therefore, there is no connection between source and drain and the current is zero.

So, this is, let us say, V G S equal to zero; and V G S more negative; and ultimately, magnitude of V G S being equal to some value, called pinch off voltage. It is a negative value.

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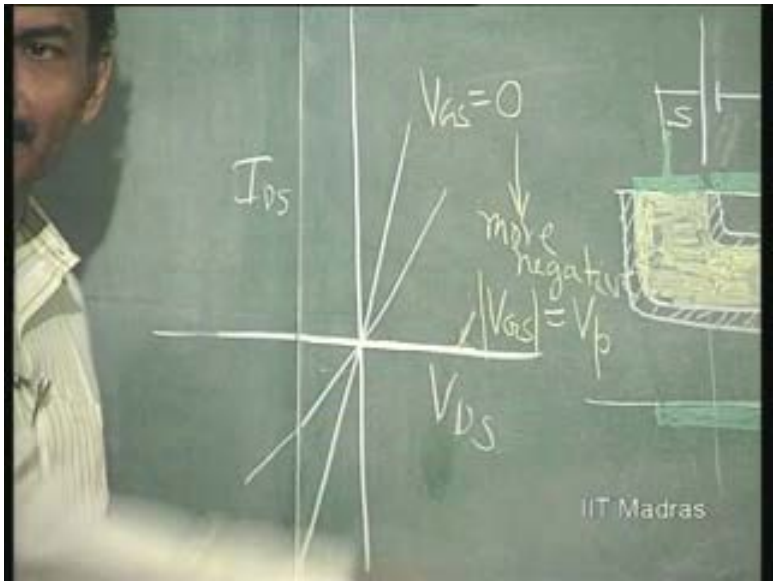

Next, if that is the case, for a given value of V G S here, it is having a certain channel width. And channel width is going to decrease as V G S magnitude is increased. But now, when I apply a value of V D S, now you see, why did I apply this polarity; because, for a given value of V G S, this way, I would like to close the channel at the drain end that is possible only if these things add. So, this voltage will add on to this voltage and therefore effective reverse bias voltage at the drain is increased in magnitude.

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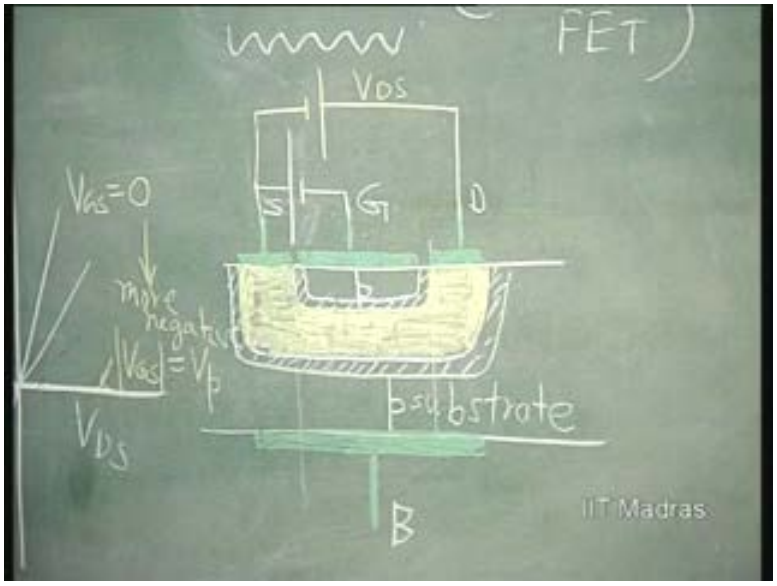

For a given value of voltage V G S, let us say, equal to minus 1 volt, minus 1 volt, what is the value of V D S that I have to apply in order to close the channel? Have you understood the problem? V G S equal to minus, we will say, V G S equal to zero volts. What is the voltage V D S that I have to apply in order to close the channel here, in magnitude? Pinch off voltage. That, by definition, is the pinch off voltage. Pinch off voltage, when V G S is zero, V G D is the same as the V S G, V S D. So, the voltage that I have to apply to the drain in order to close the channel when V G S is equal to zero corresponds to pinch off voltage in magnitude.

So, if you say, pinch off voltage magnitude is 3 volts and V G S is minus 1 volt, what is the value of V D S at which pinch off occurs? Minus 2. If V G S is minus 2 volts, what is the value of V D S at which pinch off occurs? Plus 1 volt, right? Because, pinch off voltage essentially remains the same. It is 3 volts, whether it is getting distributed between V G S and V D S is your affair.

So, let us now see. The same thing happens. This is non-linear resistor here; and this will keep on decreasing and at a value which is equal to what? – V D S equal to pinch off. It goes to saturation. The current remains constant. And, let us say, this corresponds to V G

S equal to minus 1 volt. So, at V p, V G S equal to minus V p minus 1 volt, this will go to saturation. Let us say, V G S equal to minus V p; then, V D S equal to zero ((... Refer Slide Time: 51:00)). Pinch off occurs. So, this is the kind of pinch off characteristic...

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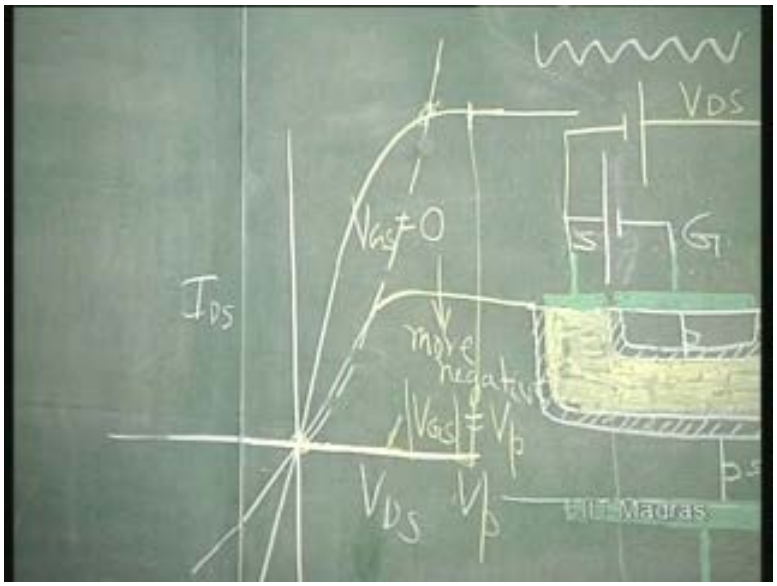

So, characteristic is exactly similar to that of MOSFET characteristic; but this mode of operation is called depletion mode. This mode of operation is called depletion mode.

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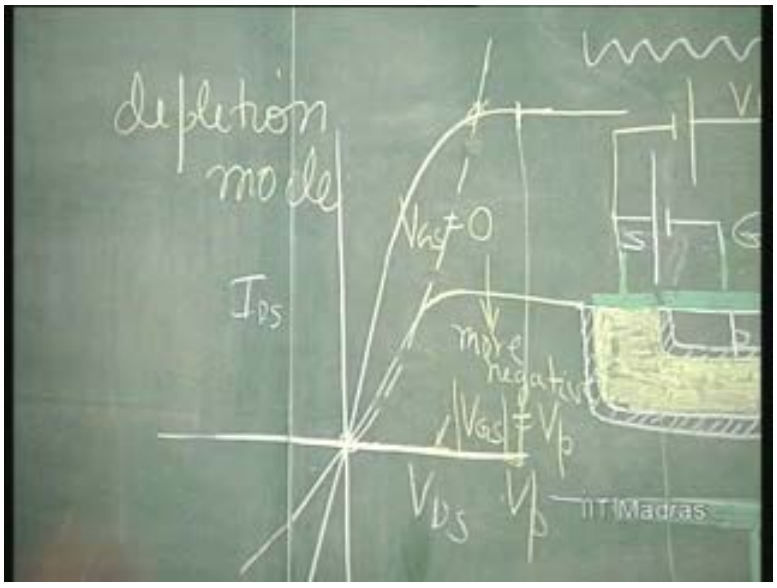

We can actually build a MOSFET also equivalent to this by having a channel; so you can also have a channel.

You can have n, n, and the gate oxide and diffuse impurity here, diffuse impurity here and actually have a channel like this; and then have a gate oxide here and then the source terminal. This type of MOSFET is called depletion mode MOSFET, even though it can work both in the depletion mode and enhancement mode; because, it is a MOSFET; we can apply positive gate voltage and negative gate voltage. Nothing is going to happen. It will not draw any current.

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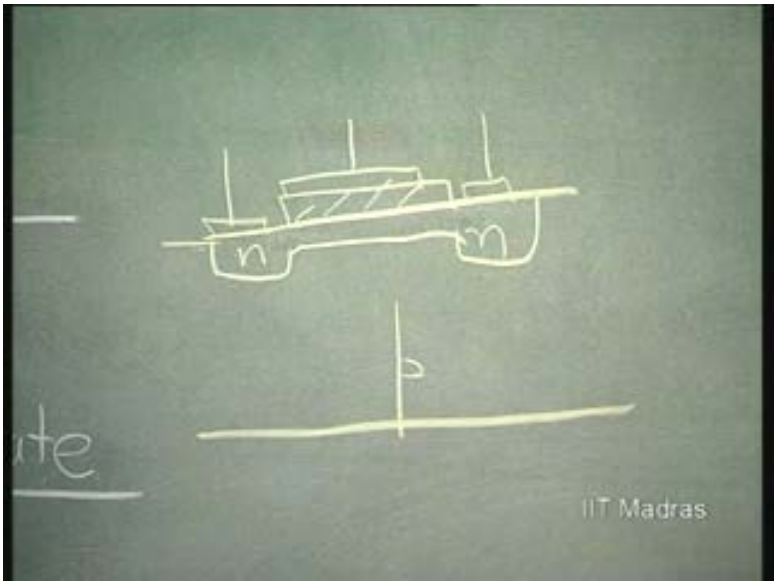

So, as far as the depletion mode MOSFET is concerned, you can have a channel already existing. That means the symbol is very clear. The channel is already there. So, it is not broken and this is the substrate. So, this is the complete symbol. But again, it is too cumbersome for us to draw. So, like the other case, the symbol... but then, you indicate saying that this is already having a diffused channel; the shaded portion indicate a diffused channel already existing. This is called a depletion type of MOSFET.

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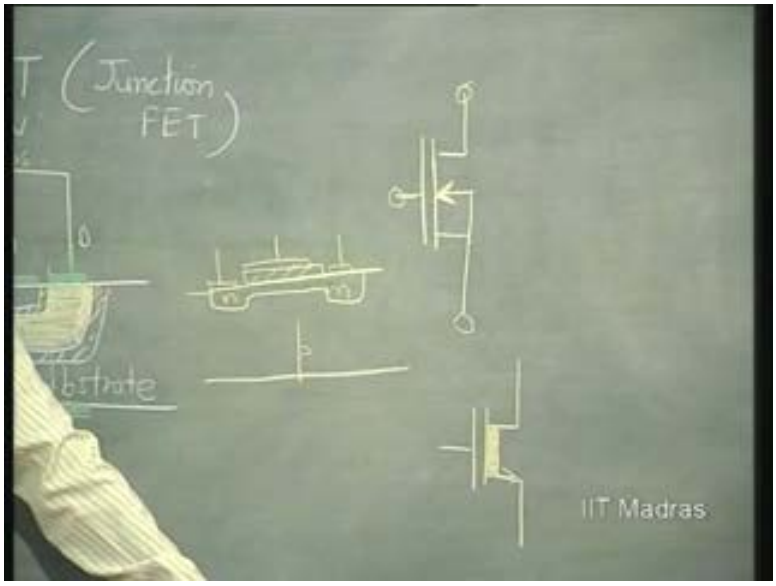

So, depletion type of MOSFET and JFET have similar characteristics; but depletion type of MOSFET can also be worked in the enhancement mode of operation. So basically, the equation is also the same square law.

But instead of having K and all that, you have this as I D S s constant 1 minus V G S by V p whole square. It is the same square law. Mathematically, there is no rela... difference between the equation that is given for enhancement type of MOSFET and this. Only the constant of proportionality, I am defining it differently. What is that constant? That constant corresponds to the current saturation for V G S equal to zero; because, there is a characteristic that corresponds to V G S equal to zero here.

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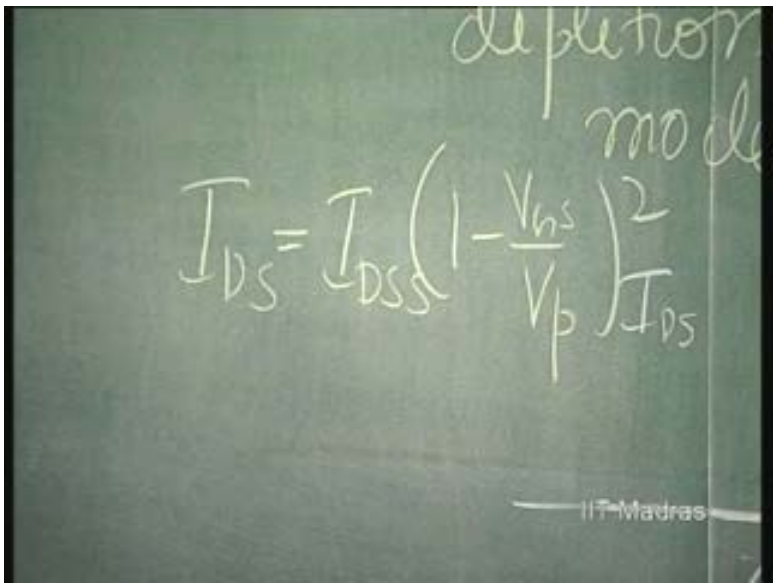

Whereas, in the case of enhancement type MOSFET, there is no such characteristic called V G S equal to zero; because, current is not yet flowing. Only, when voltage exceeds, the threshold voltage current starts flowing. So, in this case, the same equation is rewritten as I D S. For example, this can be I D S S by V p into V p minus V G S whole square. Since it is square, this is V p square. I D S S by V p square into V G S minus V p the whole square. This is similar to K into V G S minus V T the whole square.

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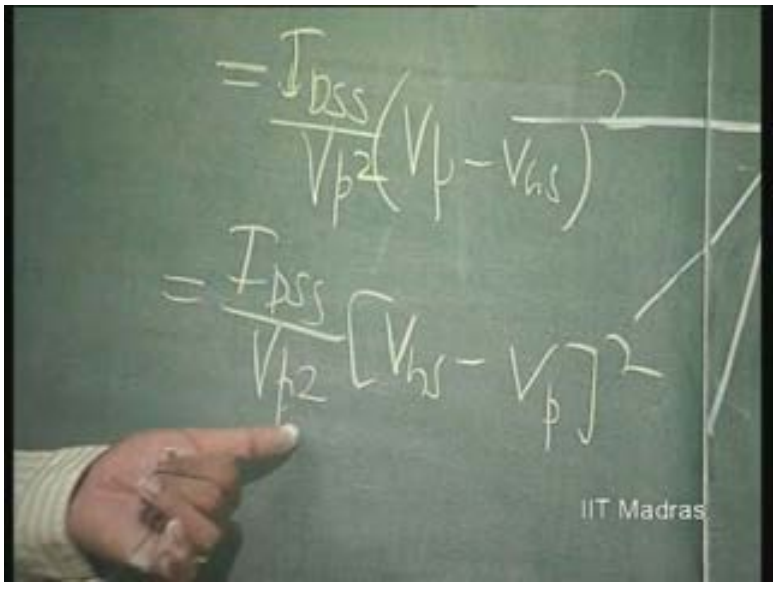

Only thing is K is defined differently in the case of depletion type of MOSFET or JFET. So, it is always defined this way; saturation, with respect to saturation current at V G S equal to zero. So, characteristic also is mathematically the same as that of enhancement type of MOSFET, mathematically.

So, with this, we will stop discussion about the FET characteristics. In the next class, we will discuss about the FET circuits.