Digital Circuits and Systems
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Lecture – 33
Design using Programmable Logic Devices (contd...)

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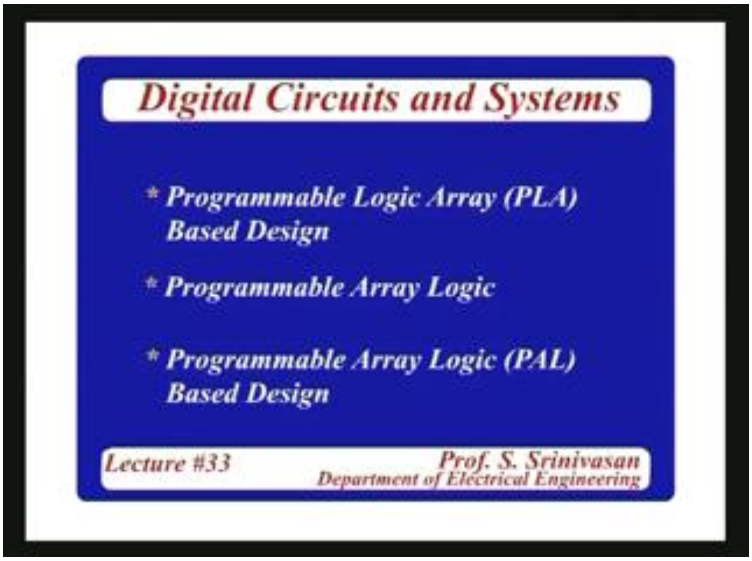

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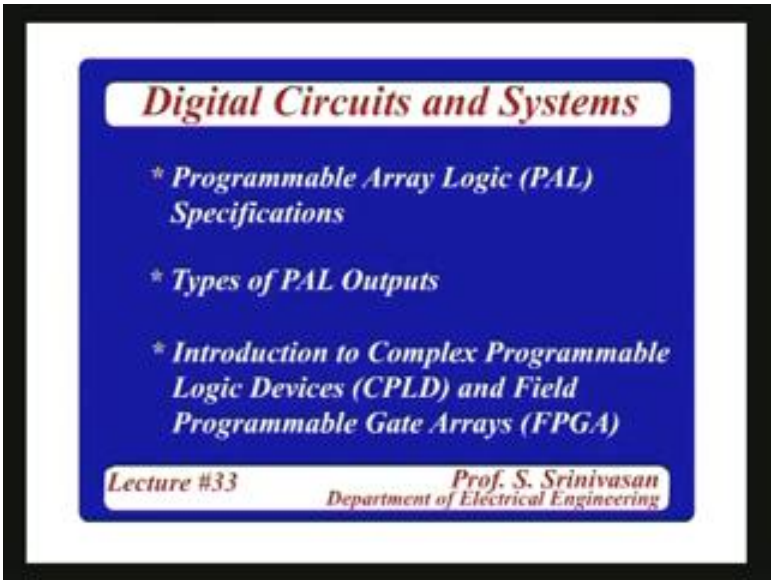

We have been talking about the three different types of Programmable Logic Devices, prom programmable ready only memory where you generate all the min terms and

combine them in or gates to get the different functions fixed AND array and programmable OR array. Then we thought of Programmable Logic Array where the number of AND gates are reduced to generate not all min terms of given input variables only generate a few products terms from which we can get the output functions. so there is a programmable AND and programmable OR then we looked at the third possibility the programmable array logic PAL wherein that flexibility of generating small number of product terms was kept but the outputs the OR gate array was fixed. That means each output had an OR gate in which only few of the product terms are connected pre-connected and it cannot change those connections.

That means there is the programmable AND and fixed OR. if you can really do a good job of optimization Programmable Logic Array then it is good but in view of the practical difficulties it is not very popular so programmable array logic in which you will need to only minimize the Karnaugh Maps and then use appropriate size of the programmable logic with proper number of input functions with gates became very popular and that was what we saw in the last two lectures these three devices and then simple examples.

Today I asked you to do the example of the binary to 7-segment decoder using PROM, you can also do it for PLA Programmable Logic Array. If we can do that of course we need to specify the size of the Programmable Logic Array where you will have to select the common terms. So,, only if you know the number of product terms available or given to you only then we can optimize it based on that. but just make a general design with as few terms as possible having as many common terms as possible, repeat the same exercise of BCD to 7-segment display decoder using Programmable Logic Arrays assuming that you are required to optimize or make as many common terms as possible within the different segments then come up with this size you come up with a requirement. It may not be available in the market that you want, it may be an odd number, the number of AND gates and odd number of outputs but outputs are fixed of course, 7 outputs and 4 inputs. The number of product terms is minimized taking into account the common expressions and then we can repeat the same example with programmable array logic.

Of course here again four inputs seven outputs but you should know how many inputs are required for each of those output OR gates that I can't say now without minimizing it so you individually minimize each of those and segment them, logic a b c d e f come up with a list of product terms AND terms for each one of them and come up with a requirement saying I can do this if you can give me seven OR gates one of them with so many inputs, one of them with so many inputs and so on. So give me a listing of how many inputs should each of those OR gates require so that will complete exercise of all these three of course I gave you a simple example in the class I am asking you to do a slightly more extensive example with more inputs, more outputs and more number of terms so that you have an idea of the design. You can call it home work, do it.

Now let us move and as I said programmable logic array is very popular device today in the design of digital system using programmable device as against the design using gates or medium integrated circuits, now there, there are varieties of devices available of

course one is the manufacturer's. Two types of varieties are there, one is that different manufacturers make them, that is only a product then second variation is the type of device which means how many inputs and how many outputs we need for a system but how many product terms can it generate and what is the composition of the inputs of each of those OR gates. So you will have to give the specifications. For example, pal specification.

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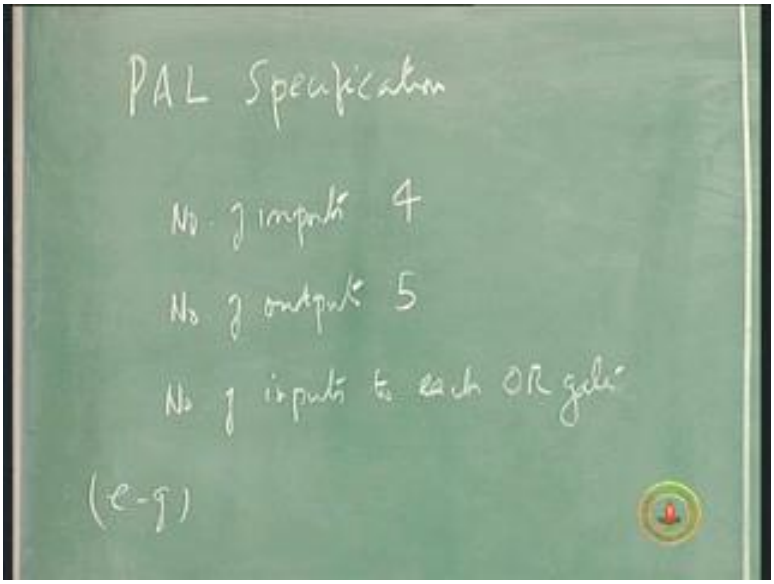

Number of inputs available, number of outputs and then number of inputs to each OR gate. As an example if I have the number of inputs four and number of outputs as 5 I don't know, these are arbitrary things, there are standard devices. It is not enough if I say 4 and 5, I will have to say for each of these five outputs how many product terms can be connected to the OR gate which leads to each of those outputs. I will have to say in addition number of inputs to each OR gates that means I have to say for example (2, 3, 3, 3, 2) that is like this (Refer Slide Time: 9:10).

In case I have 5 OR gates then the first OR gate will have, it is like this, second one is this, 3 3 2, so total number of product terms that is 4 will be 13 in this case. There is no use giving this unless you know this structure.

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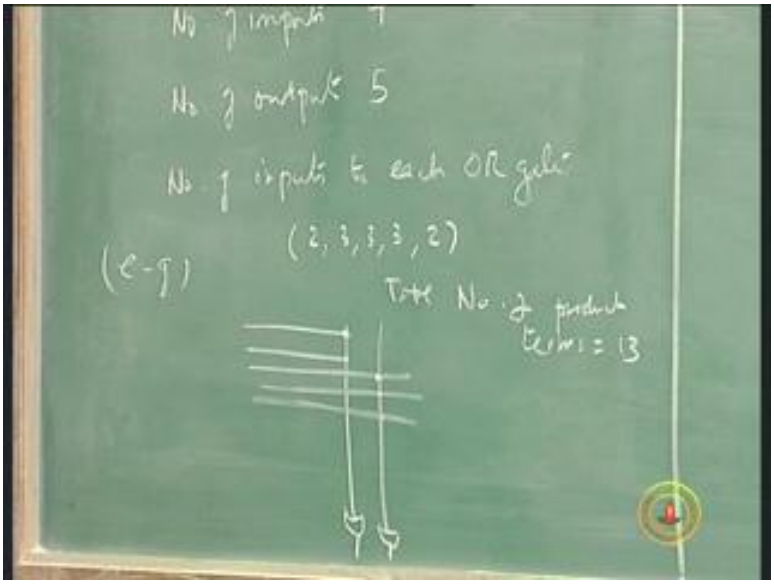

There is no use telling you that I have four inputs and five outputs and thirteen product terms so you just minimize it and use it to get the implementation. The next question you will ask me is how are these thirteen product terms connected to different OR gates. There is no way you can change those connections whereas in a PLA this is enough, this, this and this is enough (Refer Slide Time: 10:20) so I can reuse them in different OR. Therefore, for ROM I just need the input and output alone the number of inputs and outputs for PROM, in a Programmable Logic Array PLA I need to know inputs, outputs and number of product terms because each of those product terms are given as inputs to each of those OR gates so I need not tell you how many of those product terms are connected to each of those OR gates.

In the third variety namely the programmable array logic I need to tell you not only the number of inputs number of outputs but I should tell you how these product terms are distributed as inputs to the OR gates. Of course the total number is not of consequence to us. We need not count the total but if we want we can count the value.

That means for the selection of devices for your application first of all we have to choose the manufacturer, choice for our reason, for the price, reliability, types of devices you are looking for is available with that manufacturer then I will not go to it because that is the commercial aspect then you will have to look for this value. That means there is variety in the manufacturer, there is variety in types of devices so these are standard. I am going to talk about another variety today.

This PIL is a very popular device and lot of people are putting lots of things and are making it more and more attractive for people to use so they are coming up with features which are useful to the designer so that those devices will be chosen as against to the preference for a competitor's device that is the reason.

Types of outputs:
What you mean by that? Each of these product terms F_1 F_2 as I said are till now combinational logic, I have been saying combinational logic design using Programmable Logic Devices so we will have an output function in terms of P_0 P_1 P_2 etc. Now simply like this (Refer Slide Time: 12:36) each of these AND gates, each of these inputs a b c and then counterparts also, suppose you say make it simple and say A and B as inputs then you have A A bar B B bar are available so all my product terms can be functions of A A bar B B bar and that is what I mean when I say two inputs. Now I am assuming that have the first product term which combines this in someway this is symbolic I have put an AND there I don't show all the inputs, I will just show the AND gate which just can take any of those inputs, we can take as many as these inputs as required to make a product term so this (Refer Slide Time: 13:23) is my P_0, P_1 this is how you find it in the data sheet, if you look at the data sheet your Programmable Logic Array there will be a block diagram, you can see in books also the digital logic book Programmable Logic Devices chapter if you look at they will give you a symbolic description of some of the commercially available devices and how do they represent it? This will tell you that there are two inputs possible and four product terms possible each of these product terms can be functions of A A bar B B bar.

Then of course there will be a third one which will tell you this, this is my F_1, this is a pictorial or schematic representation of PAL. Now what you mean by type of outputs? You have combinational input and combinational output but normally you assume the positive logic positive logic normally we assume we have a variable A and B and they take certain values output is true and in the other case the output is false so we assume that high is 1, 0 is low voltage high is 1 voltage, 1 is high voltage and 0 is no voltage, and as i already told this is active high logic a logic in which 0 is represented by lower of the two voltages. Logic will have only two levels 0 and 5, 0 and 2.3, 0 and 15 if you want to really have it, o and 1.2 volts whatever low voltage is 0 and high voltage is 1 so this is active high logic.

On the other hand I may want to have a situation where I want active low that means I may have a NOR gate at the output so first in the types of output is active high and second is active low. What is meant by active low is F_1 F_2 are represented as nor outputs rather than OR outputs. The reason is as you know like in DeMorgan's theorem and all that you have seen it the simplification of logic sometimes it is attractive to give solutions in terms of the complimented functions that is a simpler function compared to the true function which is more involved or may be the output of this needs to be lower in order to drive the device I am going to drive this f one f two I am going to use these outputs to drive devices which will work if the voltage is low and stop when it is high, is it possible? Yes it is possible, it is a possibility. So in this case I want to synthesize circuits whose outputs are low rather than being high for a given combination of inputs.

So I want that combination and I have it. So all we have to do is look for the device. That means you have to go through the data book in conventional terms or modern terms that is go to the website or product manufacturer give the requirement and they will give you the devices. it is not only enough if you say I want four inputs five outputs and I want this

type of combinations to the outputs AND gates and also I should say active high or active low, then there is a NOR which is already here, exclusive or EXOR.

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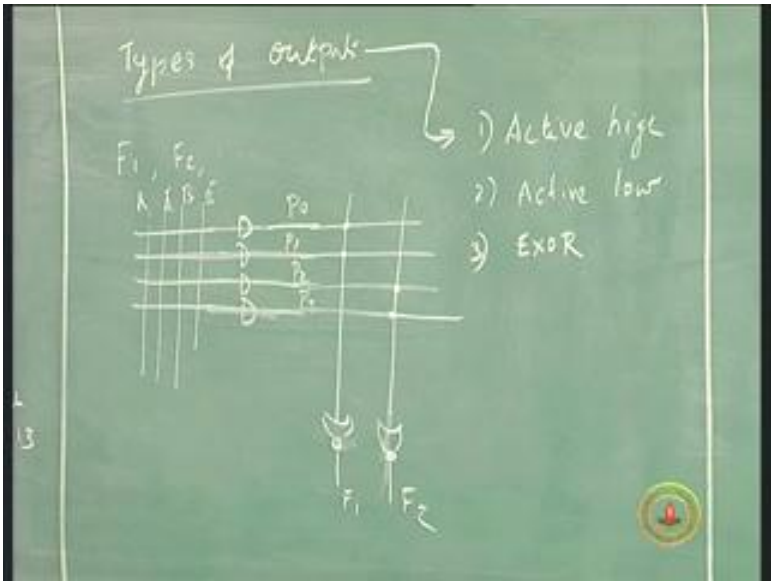

What you mean by EXOR output is I can have groups of, normally this is what it is (Refer Slide Time: 17:50) I can combine these two so if this is P_1 P_2, P_3 P_4 this is P_1 or P_2, P_3 or P_4 and this is P_1 P_2 exclusive or EXOR P_3.

So, if you want a function in this from which can be also single, I am just giving you this, you can also put P_1 P_2 and exclusive or EXOR. Supposing you want an adder, full adder or a parity generator, code generator and so on, remember we did some of those things earlier but it is not necessary that only one of those terms should be to the EXOR, the EXOR will have two inputs but each of those inputs need not be a single AND product, it can be OR combination of several AND terms both are possible.

Likewise I can have an EXNOR output, all I need to do is to change the output gate to our requirement. The point is these are available. The idea is to go for as few ICs as possible, we don't have to do logic outside this, it is necessary of course to do it but you need to devise a chip which will do everything so you program it for your application. These are small applications, mechanical applications, non electrical applications. The signal is coming convert it into electrical signal do some processing and put it back as a mechanical signal. They do not want to have huge electronics there but just a little device which will just program.

Many of these gadgets which appear are very big but non-electrical gadgets like a mixie at home or a washing machine you will find that it will not work but then the moment the service fellow comes and replaces the chip it works, he just changes one chip and then it works because that one chip does all the functions. So in such a case don't say okay I only have active high then you need to put an inverter if you want to, so my device only

takes active low for functioning, you are giving active high so you say go to an inviter. You say it is fine you can give an inverter but for that you need voltage so there are so many things, second you have the socket and so on and so forth. Hence, that is the reason.

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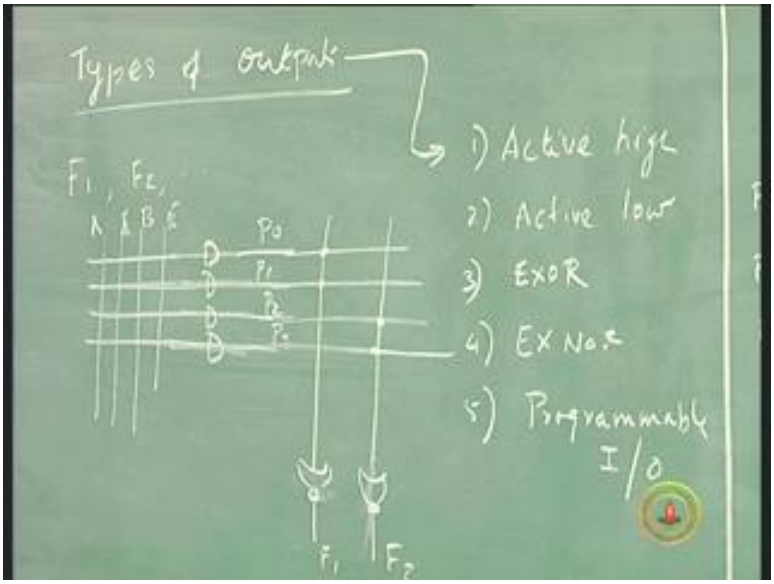

The idea is as I told you is to give flexibility for the designer with options which are normally found in electronic service, it is not a big deal to do all this but what is slightly different is, somewhat a big deal is we can have what is known as programmable I/O. what is a programmable IO? Supposing I want in this case four inputs five outputs a very small device where you generally won't have any problem, in fact you will have problems finding four inputs five outputs, you will find the reverse 8 inputs and 8 outputs which is the smallest you can get possibly, on the other hand suppose I want twelve inputs four outputs and this fellow says I have 8 inputs and 8 outputs totally 16, I want a total 16 but I can't use it because you have 8 inputs and I need twelve inputs then I have to go for a 16 input device because twelve may not be available because 16 outputs[……22:09] because the device size becomes much larger.

I don't know how many of you have walked into the electronics lab so far, the lab where you go to check your mail in the group floor of ESB the same lab is used as a digital lab next semester but I don't know any of you showed curiosity to see what are the other things available in the lab, you just try go to the computer check your mail and come back, browse the internet, all you need is a little curiosity, two minutes extra, there are lots of people sitting there like lab technicians, lab assistants, then lab supervisors who can help you, they want somebody who is interested because they have the lab class only in the afternoon and they would be very happy when a student goes to them asks I want to know about the IC then they will be very very happy.

Why don‘t you try doing it when you go to the digital lab next time. you need not go anywhere else, you go to the same lab for mail checking anyway there if you look at the ICs there are different sizes, usually there are twenty pins 8 inputs 8 outputs 16 power supply ground and may be there is a clock required and something, there are some standard packages, these are called standard packages, there are designations, type numbers for each of those packages I may not know all of them but even then there is no point in presenting them here 20 pin package, 16 pin package but then there is nothing like a twenty pin package, nothing like a twenty four pin package, there is nothing like a thirty pin package so if you leave the bus an 8 pin package might be there, 8 is there, 16 is there, 20 may be there but when you leave the bus it may go for 40 pins.

My problem gets more and more complicated now. I wanted twelve inputs, four outputs I have only 8 and 8 in a twenty pin package, I have 16 pins input and 8 pin output or even 16 and 16, 16 inputs and 16 outputs and forty pin package which will double the size length-wise because pins, it is mechanical I can put million gates in a small IC small area because we are talking of dimensions of nanometers today microns and submicrons the dimension but inside you can do anything etching and all that electronic beam lithography so that they can make a line which is as thin as the size of the electron or molecule, [molecular p……25:10] laser etching and things like that but then I put one million gate functions then I want to seal it and give it to a customer then it should have a mechanical recognition it cannot be brittle, it has to be put on a base which will stay and then I have to make connections because when I have thousand gates naturally there will be large number of inputs and large number of outputs so I will have to provide for all those inputs and outputs that means I need a base with different pins for inputs and outputs and the size they cannot be micron dimensions how do you physically connect it to another device or a computer so I need to have a minimum size so when the size becomes larger all our concepts of size saving and everything has to be re–thought. So we want a chip in which I would trade off, I want twelve inputs and four outputs, you are having 8 inputs and 8 outputs so if I can trade off four of those outputs for inputs it will be nice I can do with a twenty pin IC and then be very happy about it that is the concept of the programmable I/O.

So certain pins are designated as I/Os and it can be used as input and outputs based on your requirement. whatever you want is available in the electronic market that is the beauty of today’s technology, it is not individual making but the technology has given it over these fifty years of semiconductor technology has given you all that you want and much more than what you can use.

So what is the concept of this programmable I/O. I said I want only four of the 8 outputs available but all those four outputs should be used as inputs.

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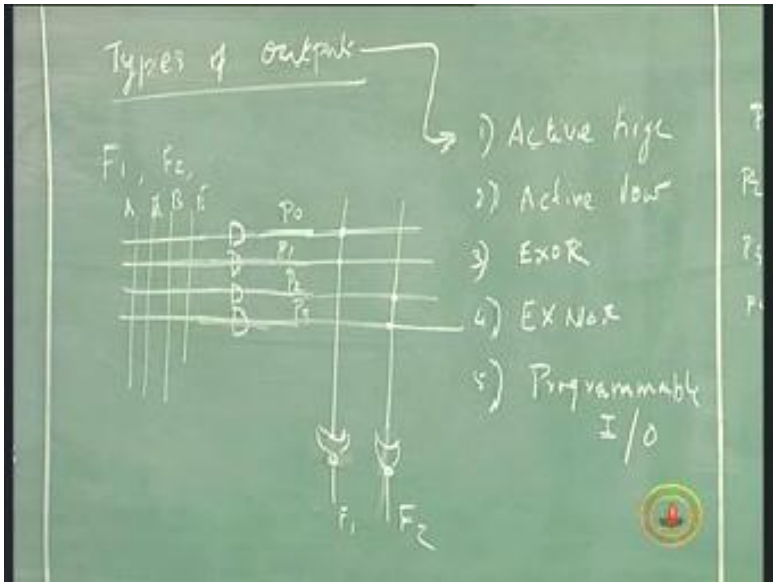

So this is a pin which is normally an output pin, this my device PAL (Refer Slide Time: 27:27) individual output is coming normally in an output but I want this to be chosen as inputs because I already have four of those outputs this is the fifth one and I don't want to use the inputs. So what I need to do is put a simple buffer here and inverter in whatever size you want, you talked about the tri-state remember? enabling a gate and disabling a gate we talked about it, there is a state called high impedance state so I am going to put an enable here (Refer Slide Time: 28:08) so I can physically disconnected this, electrically disconnect this, make it physically present, I can electrically disconnect this from here because when this is zero output goes through and then output, when EN is 1 when enable is 1 this is disabled which means there is no connection between output and input electrically. That means as if this is a mechanical projection available to me which has no connection to the rest of the circuitry, all I need to do is use this as inputs, this is the same pin the one output pin, this output pin (Refer Slide Time: 28:57) will be used as an input now why I am putting this is when I have an input like A supposing this is A B C and let us say this is D inputs I need both D and D bar in my logic, when I have input D a new variable I need to have both versions of them, so my input is not complete unless I give the complement also, combine them, I can't go for an inverter inside, inside it is all AND gates and OR gates so there is an inverter along with that.

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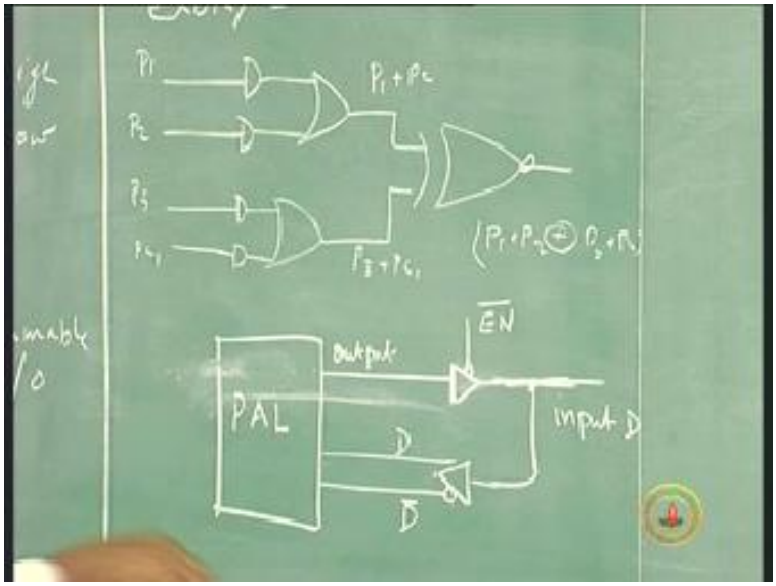

So this is the programmable connection (Refer Slide Time: 29:56) if EN is 0 this is used as an output pin, if EN is 1 this is used as an input pin and a new input can be connected and its complement is also available for implementing your logic using that extra input. This concept is called programmable I/O.

Of course this PIL is only my artificial but the PIL is really the whole thing, this is the rest of the circuitry because this will come from a combination of AND gates and this will go as inputs and so on. so the total thing is a PIL, what we had originally normally I would had this output available to you but now I have an extra logic here which can keep it as an output if you want when you are making EN equal to zero, if you don't want this to be the output then I will make EN is 1 and this is connected actually this AND gate is not available as output this OR gate or whatever, this is an OR function which is not available so I take this and use this as an input with this one complement and all that and I also use in my synthesis, this is my programmable I/O. You cannot have both of course, some of them have to be programmable. If you want to use a device of this choice but you choose one with that feature.

Once you have 16 8 and 8 I cannot have 16 inputs and 8 outputs, that's not possible, a total of 16 but in manufacturer's data sheet they will mislead you because there is something like selling, everybody wants to sell their products so they will say 16 inputs and 8 outputs, you have to be careful in reading those data sheets, what they mean is up to 16 like this price reduction 50 percent off. When you go to a shop you will see a small thing up to fifty percent and then they will say five rupees off.

You went there because there was a big 50 percent off and you didn't see that up to. Similarly, they will tell you 16 inputs 8 outputs I am not joking it's true, you go through the data sheet of any standard manufacturer, for a particular device you will say 16 inputs

and 8 outputs, you go there they will say up to 16 inputs up to 8 outputs but not at the same time, it is sales gimmicks, the academician do not know all those.

The last output is called registered output. Registered output is what is a combinational logic used in the sequence of circuit as a driving logic as a steering logic and what does it steer, the input of the flip flop, it is used as an input of the flip flop to share the circuit from state to state. So, if you can also put that flip-flop as a part of the PIL I can finish my sequence circuit design in one single chip. suppose I have a single chip solution for some of the problems we did earlier sequence detector and all that we had combinational logic we had flip-flops outside, those flip-flop outside need not be put now because these are small ICs this is one large IC or medium scale IC and you want to have extra small scale ICs put together and again those extra logic putting them together, wiring and so on. So, if I can push those flip-flops also inside the PIL then that is called a registered output.

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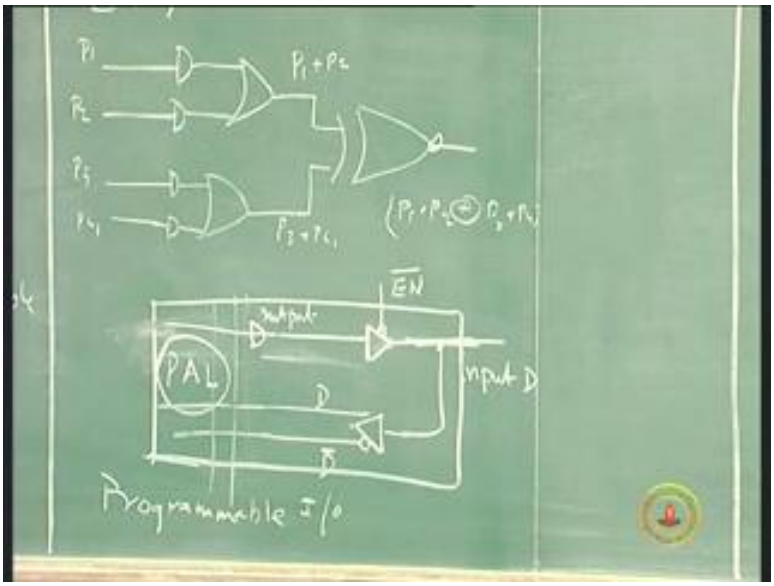

The reason is we have these outputs, this is my output O1, I want this to be my input for the flip-flop, and the flip-flop will be the state variable which will be fed back, this is the standard sequence circuit block diagram. We have the steering inputs, steering logic, output of the steering logic will be the next stage information which goes to the flip-flop […….35:06] after one clock cycle. so that I can do within the chip itself. So if this is my D flip-flop as an example this is my output function Q bar and this has to be used as a saving input for the next, state variable is also used as inputs, the present state variables are inputs to the next state so I want the output of this also fed back or available as inputs.

Remember that this variable is available here as O_1, this is O1 bar so when you invert it you make sure that this is O_1 bar, this is O_1, this is O_1 bar (Refer Slide Time: 35:55).

The old thing is within the IC. This flip-flop is inside the PAL, an OR gate output of the PAL or combinational output active low or active high does not matter drives the flip-flop to the next state and the next state information is fed back, so all that is part of this. That means it is a single IC Programmable Logic Array IC with sufficient number of registers, sufficient number of flip-flops inside it. So when I choose my outputs I need to choose a variety of combination of outputs. I want some to be combinational outputs for direct outputs and some of them as registered outputs, these are called registered outputs, some of them are registered outputs. The number of registered outputs I need is equal to the number of state variables I want to use in my design.

Supposing I have, a 16 or 8, this is a good example. Suppose I have an IC called 16 or 8, 16 inputs and 8 outputs what he means is up to 16 inputs and 8 outputs so 8 of them are inputs and in the other 8 4 can be registered and four combinational because you have to go into details of how many connections for each of these OR gates etc. this is also possible. You can select an IC with four registers, four non–registers as outputs then 8 inputs can be combined, so up to four state variable you can have 16 states, the sequential circuit up to 16 states can be implemented using a single IC. If I want more of course 8 registers also I can have.

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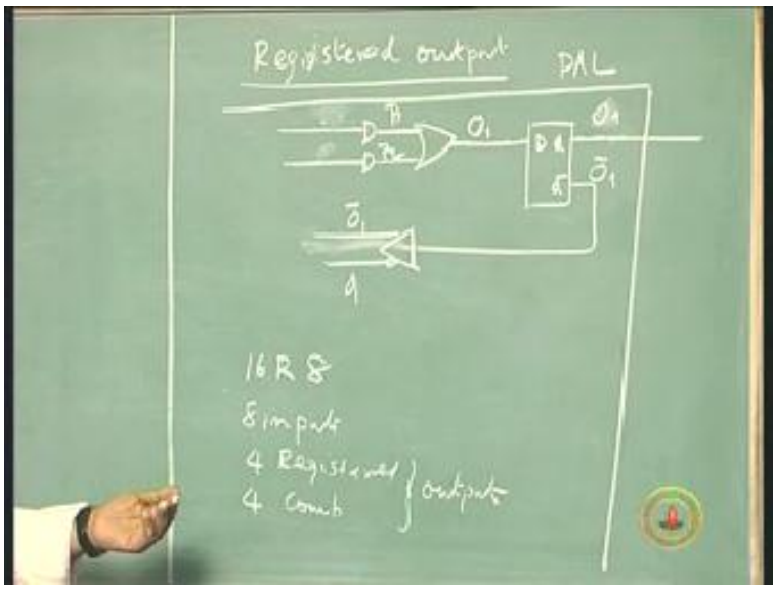

Therefore, in most of the textbooks there will be a 16 or 8 diagrams. Please look at this 16 or 8 block diagram even in your textbooks, some of the standard textbooks or most of them will have this, Mano has it. So if you look at 16 or 8 diagram it becomes clear about the registered outputs or you can look at 16 or four also, four registered outputs. Since it is up to 16 outputs and four registered outputs the other four can be non-registered outputs. You can have 16 or four if want to and then you can have all the other features.

When you have this programmable feature (Refer Slide Time: 39:00) or this feature we need extra inputs, you need a clock signal, enable signal so all of them have to be given

so decide on the number of pins required number of inputs number of outputs, ground and power supply, clock required and enable required and all those things. This has to be the clock remember (Refer Slide Time: 39:23) so clock is one of signals so I need to connect also. So my pin outs I have to account for the clock signal how to feed the clock into the pin, to an output pin external pin so external pin has to take a clock and through external pin only I can enable signal and then I need inputs then I will take outputs.

Now you know a variety of this so you can do almost any design up to what you have seen small designs, pure combinational or pure sequential like registers or combination of registers, combination of sequential or combination of ANDs sequential everything can be done so PAL as I said is a versatile programmable family and people have used it in large, the designs now are a very popular alternative and you will have to go to the website of any standard manufacturer like there used to be one MMI [40:38ma,…….. memory] many industries most of them do it I think analog devices national semiconductors etc. So I would like you to go to one of the websites national semiconductors look at their PAL alternatives or you go to the lab and ask for a data book. The same lab I was referring to has data books, you can go and ask for a data book of the programmable array logic and see for yourself there are varieties of this, each of them will have a block diagram.

So I want to spend the next few minutes on summing up this concept of the programmable device. The design using programmable device is very popular today because of the flexibility of design and we can change the design including the size. But what we have seen in the class till now are very small devices.

ROM can be of any size but larger size means larger memory, space and power and we don't want to use them. As I said large ROM is inefficient for a design because large ROM means large number of inputs and the min terms are generated so when all the min terms are generated only a few of them are used so this is inefficient hardware utilization so leave that, they do it with the look up table approach but generally the size is small only they use ROM. That means that leaves two other alternatives Programmable Logic Array and programmable Array logic. As i told you the Programmable Logic Array is more popular, we will consider 5 and 8 inputs some 16 or 8, 16 or 4 will be 8 inputs that is 4 registered outputs and 4 non registered outputs.

Now these are all alright for many problems we do in the class and also many of the small systems like elevator control. We go to lift the control is a logic circuit in which there may not be this number of inputs and all those, trafically controlled. When you talk of bigger systems like micro computers, microprocessors other electronics process as we said rocket launch, avionics and even other areas, plants large number of inputs then large number of outputs that means PLD becomes inadequate.

This is the trend now, the PLD Programmable Logic Device based design is the trend but size wise it is growing. There are two options for larger designs, there are many options but two are more popular. One is called cpld, the other is called fpga. cpld is complex

programmable logic device. Nothing is complex about it, each is a PLD, a 8 input 8 output 4 registered PLD I put several of them in one single chip and give it to you, it is a complex PLD that means all you have to do is to do the interconnection properly. The functionary thing is defined, you can program the interconnected structure. So, combination of groups of PLD is the programmability structure has to be designed, interconnection to be programmed.

We do this, these are interconnect through a switched matrix, which one is connected and which ones are left, it is programming the interconnection basically. all PLD, PLD and PLDs all over the place and they are interconnected. The FPG is almost similar again the concept but it is slightly different in a way in a sense it comes with what is known as logic blocks, it is an array of gates, field programmable gate array so gate arrays are units made of gates.

Having the gate you can design a multiplexer, a flip-flop, with the gate we can design exclusive or gate and all those types of things so we have small units of gate arrays which are called CLBs Configurable Logic Block so but hundred gates they will make a unit, so like that there will be several things, it is an array of those 100 gates each, totally there may be 10000 gates, hundred thousands gates, one million gates, two million gates are available today, so two million gate structure is available, one million gate is available let us not worry about that. If 100,000 gates are available it is not that the 100,000 gates is given to you in a big sack use it the way you want, put it in front of you and you don't know how to do it they make life simpler for you by grouping this hundred million gates into smaller groups where each may contain about thirty forty gates or hundred gates maximum so such a group is called a Configurable Logic Block.

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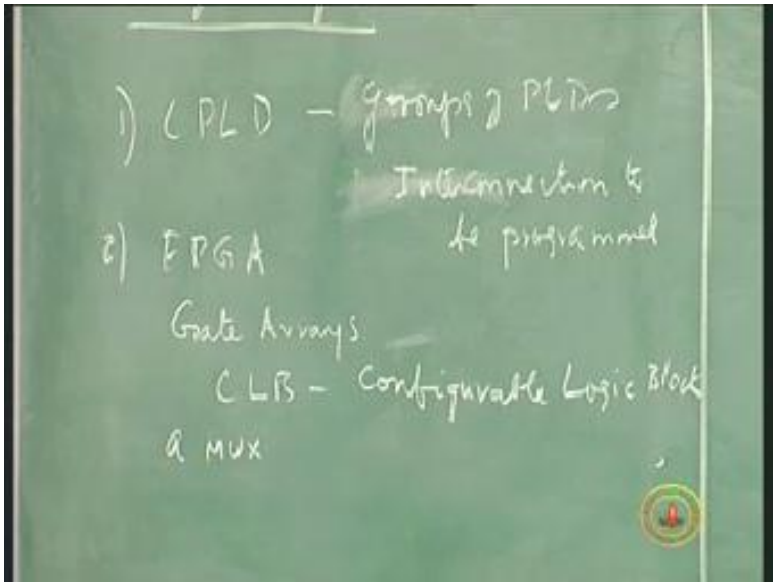

Therefore, the total number of gates available is grouped into smaller groups where each one will have a specific function like a CLB will consist of a mux. What are the various

small things we use for a design, we want a multiplexer, we want a flip-flop, we want a look up table look up table which means memory, you look at the value and then read it when you want it that means memory, a small amount memory, a flip flop, a multiplexer and a few gates so that you make a small design out of this and like that several groups are there and each of them have these standard features, each of them will have a single mux may be 4 2 1 mux, a single flip–flop, a look up table of a small size such as 8 words 16 words and then few exclusive or gates and all that so the logic has to be broken your whole system requirement, you come up with a requirement with a logic which has to be broken down into small small things so your job is to break your design into smaller groups and then do the interconnection efficiently. You have to map your logic on to CLB and also inter connect them, that is the difference between these two. Here there are standard PLDs which we are familiar with, they are available there is a switch matrix you program for switching them properly connecting the properly, program only the interconnection.

Here I have to map my logic, I have to break my logic in efficient blocks which can be fitted into each of these CLBs and then not only you have to efficiently map them but we have to interconnect them efficiently. There is a lot of debate about whether this approach is better or this approach is better, there are some companies which specialize in this called altera, this company is specialized on xylinx, now each convince the other fellow in the market and they want to do both. So now you may have both companies, these are the two well known companies altera and xylinx. But xylinx is famous well known for this, aletra is well known for this (Refer Slide Time: 49:34) but then I think they are also having the other line of products.

But then the problem here is what, problem is how am I going to program, it is overwhelming; I am given hundred thousand gates and a huge system like a control circuit of a Pentium microprocessor. I give you hundred thousand gates and ask you to design a control circuit for a Pentium processor. The problem is that the known hardware is given how I do this. I give flight path of the trajectory, trajectory of space vehicle all the various parameters and then map it on this IC. So there are standard software available. These will be done only by what are known as CAD tools Computer Aided tools, EDA Electronic Design Automation.

You will have to do the electronic design automatically but more efficiently. You need domain knowledge, don't think that it is a C programmer or java programmer cannot do this job, you need to do it because you need to know some of these things so there is a CAD tool available, this is for another day, I am just giving you the details so that you should not be ignorant. So what we have seen is a small mini school the beginning of a whole revolution or a whole range of big area of programmable logic devices in which several alternatives like that in very very large sizes so it is a big industry both hardware and software, tools are available, people constantly work on its improvement, the capability of the tools, rapid efficiency and you can work on design or you can work on design or you can work on even tool development.