VLSI Data Conversion Circuits
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Lecture - 09
Charge Injection

This is V L S I Data Conversion Circuits lecture 9.

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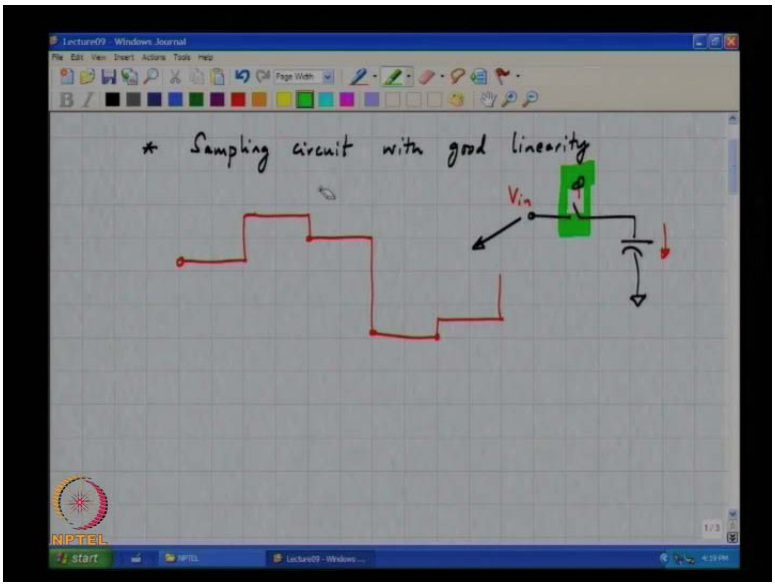

So, far we have seen how to make a sampling circuit with hopefully good linearity, in the sense that we learnt how to make the resistance of the sampling switch independent of the input signal. Of course, we know how to choose the sampling capacitor because we know that the mean square noise that sampled on to the capacitor is k t by c. So, given the resolution of our entire equity conversion system, we can go and figure out how much double noise we can tolerate, which fixes the size of the sampling capacitor.

And then depending on the tracking bandwidth that we need we go and choose the resistance of the switch that we can tolerate, often you do not want to operate on the Harry, Edge of your tracking bandwidth. So, you want to make sure that the resistance of the switch is small enough that the R C time constant is you know exceeds that required simply from tracking considerations by reasonable safety margin.

And let us remind ourselves again why did we go through under what circumstance do we need this switch to be you know a linearized by having a constant V G S. Why did we

need the switch to have a constant resistance as a function of input, pardon.

Student: Sir it is agrumental.

Of course, so in other words if the input was a continuous time sinusoid right and therefore, the voltage across the capacitor is also the same sinusoid assuming that the drop across us which is very small. Then the displacement current flowing through capacitor is C D V D T right and that gets multiplied by the resistance to give you the voltage drop, which is the difference between the input and output just before you turn the switch off correct.

Now, if the resistance varies with input signal, then the displacement current which is the derivative of the input signal gets multiplied by the non-linear resistance and gives you harmonics. On the other hand once you sampled the continuous time input, it is just sampled and held. So, within a clock period the input voltage is not changing, you might ask where do you see those scenarios right.

So, the front end of the A to D converter is the one which typically sees this continuously varying signal. Once the signal has been sampled on a capacitor nobody knows what kind of input it came from correct once it is sampled it is just as good as coming from D C you understand. And we may further want to process this signal in some way, for example, I mean we will; obviously, need to quantize this input voltage, which is been sampled on the capacitor right.

There many ways of quantization one for example, if we were may able to make a very course estimate of the input then we could quantize it in the following way. We have the sampled signal on the capacitor, we subtract the course estimate right and get the difference between our course estimate and the actual input. And now we start working on the on this error or the difference between the actual input and the course estimate.

I mean the motivation for this is that it is not always that one is sampling a continuously varying input signal as we will see going forward there many instances, where a sample and held signal has to be sampled again right; after suitable processing may be subtraction may be amplification may be you know anything else you understand. So, if this input was not continuous time, but was sampled and held to begin with correct. So, the situation is not like what we had earlier, earlier we had a continuous time input.

Now, if you already had sampled the input and you wanted to resample this on to another capacitor you understand, a question I am now posing is what kind of switch would we need to sample a signal like this. In other words would we still need a bootstrapped or a or a gate boosted switch I mean by bootstrapped switch, I mean the switch where the gate potential is V n plus V D D right. I mean has we have seen going through the last class notes it is a quite elaborate affair right.

So, to make to linearize the sampling switch there was a whole bunch of extra paraphernalia needed in order to make that happen. So obviously, you know bootstrapping the gate with the input is you know quite complicated from a circuit point of view all right.

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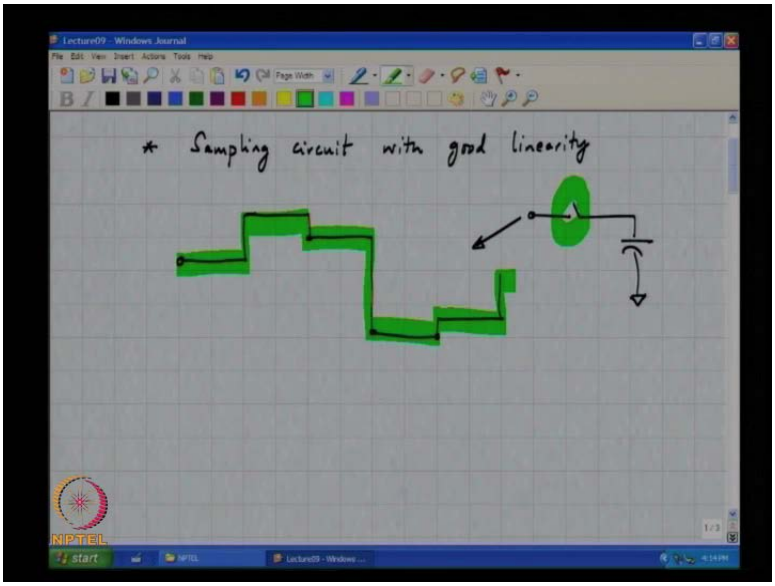

Now, the question I want to ask you is let us assume for the time being that we have a signal which is already been sampled and held and we want to resample it on to another capacitor. A question is what choices do we have for this sampling switch, is it necessary that I use a bootstrapped switch I mean clearly a bootstrapped switch will work, because I mean this is just an any other this just any other input as far as the bootstrapped switches concerned. A question is such a switch with all its extra baggage really necessary or it is not necessary, it is not necessary in this case and why might that be.

Student: Strongest these switch can pass through the each of these levels properly and if the R C time constant this optional when compare to this each of those sampled value the

sampled intervals then it is…

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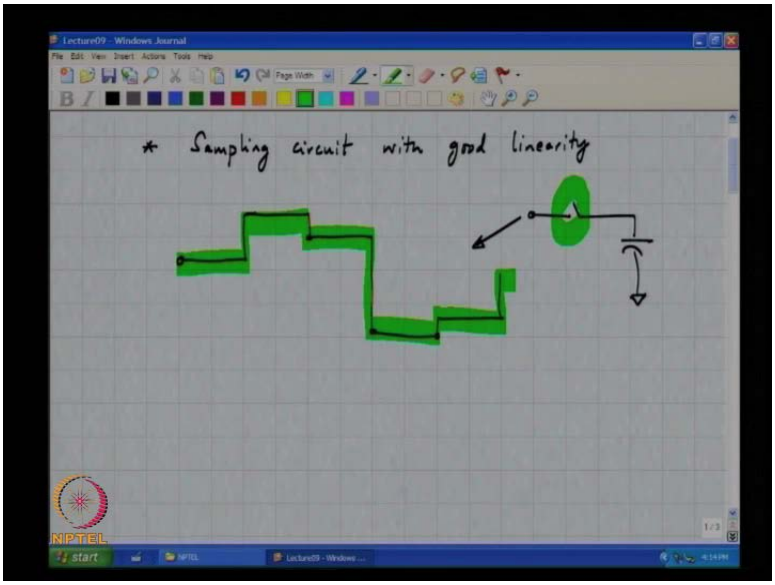

So, there is a crucial difference between this signal and the sinusoid which is continuously varying right and that is within a clock period this input is constant; which means that if the resistance of the switch even if it is non-linear is sufficiently small. What happens at the end of the clock period this voltage will be the same as this voltage, which means the derivative of the voltage is a same as the derivative of the input voltage, which means at the current flowing through the capacitor is what, what is the current flowing through this capacitor if the voltage is of this form.

Student: 0.

It is 0 right, because it is they will be a jump in the current when there is a switch, when the input changes at the end of the clock period. But, that current will quickly decay to 0 correct because the rate of change of this voltage is 0 within a clock period right. So, if the current towards the end of the clock period which is what you are interested in sampling right is 0. Then even with the switch is non-linear the voltage drop across that switches is 0 which means that there is in principle there is no problem with sampling a distorted version of the input.

So, in another words, just before you open the switch and in which switch we are talking about this switch. So, just before I open that switch the voltage here will be virtually the

same as the voltage at the input does make sense. Now, the question is what happens when I indeed turn the switch off all right. So, just before I turn off the switch, the voltage to the left and the voltage to the right of the switch are exactly identical.

And why because the current through the capacitor is 0, which means that there is no voltage drop across this switch, even though the switch can have a resistance which is non-linear nonlinearly dependent on the input is this clear. Of course, when the input changes at the end of the clock period there is a big difference between the voltage to the left to the switch and the right of the switch, because a capacitor will not allow the voltage to change instantaneously.

So, there will be a spike of current that occurs; however, that will only occur around transitions of the input and will quickly died on right as the cycle continuous does make sense. So, it is often you will note that bootstrap switches are gate boosted switches are only employed at the continuous time to discreet time interface. Once you digitized it, once you have sample the input with sufficiently good fidelity after that most of the time simple switches are all that are need is that clear. So, what kind of switch do you think is a good candidate here.

Student: Transmission gate

A transmission gate is in principle good enough because this signals can go all the way from 0 to V D D and a transmission gate allows you to sample the input without any problem does it make sense all right.

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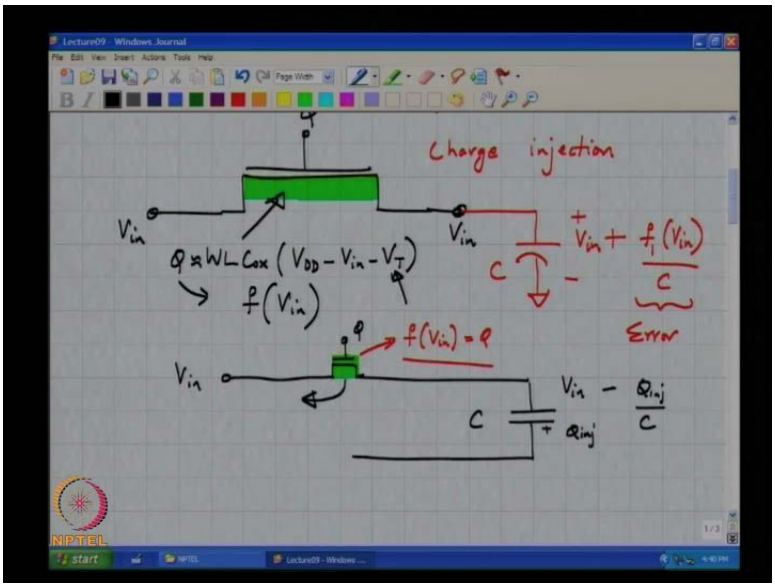

So, now let us examine the process that happens or what happens when you turn the switches off. So, why the most transistor conducting in the first place let me now make a blowup of the transistor. So, let us say this is V in this is V D D and this is the sampling end of the switch this will also be equal to V in all right. I am assuming a held input, so that the current through the MOS transistor is now 0; is this cleared everybody the nature of the difference between a continuous time input and a sampled and held input. Now, why is a MOS transistor conducting.

Student: Sir thereby channel unit.

There is a channel when you apply V D D there is a channel charge the channel charge is a what is a responsible for conduction right. And given V D D and V in on the dimensions of the transistor and it is properties like threshold etcetera, what do you think is the amount of charge in this channel

Student: ((Refer Time: 13:44))

It is a very crude approximation it is.

Student: W L.

W L times C ox times.

Student: V D D.

V D D minus.

V D D minus V in minus.

Student: V t.

V t right this is please note only a very crude approximation and is not quite correct a detailed analysis of this charge will reveal that this charge Q is some non-linear function of the input and a whole bunch of other things. I mean one state we have seeing that is that the threshold voltage itself through the body effect is dependent on.

Student: V in.

V in on v in, so even this crude approximation is telling you at the channel charge of a transistor depends on the input does it make sense. So, if the channel charge of an N MOS transistor depends on the input it follows that the channel charge of the P MOS transistor also depends on the input alright. So, when this potential at the gate goes from high to low and when does it go from high to low, when you are transitioning from the sample phase to the hold phase that is when you turning it the switch off.

And turn the switch off what are you going to do you are going to yank the gate towards ground. Now, the question is what happens to this charge clearly, when the gate is connected to ground what is the channel charge.

Student: ((Refer Time: 15:33))

Channel charge is 0. So, when the gate was high the channel charge was this when the gate is low the channel charge is 0. So, something must have happened to this channel charge right. So, where do you think or what do you think happen to this do you understand by argument right. So, the gate was just now connected to V D D there is a channel charge of I mean C ox times W L times V D D minus V in minus V t. And now I have turn the gate off and we all agree that there is no charge in the channel the transistors off clearly this charge must have gone somewhere a it is vanish into thin air right, where do you think it could have gone The MOSFET has four terminals it is got the body, it is got the gate, it is got the source, it is got the drain, if there was some charge and then it vanished it must have gone out through.

Any of the 4 terminals.

You know any or all of these four terminals which do you think it cannot go through.

Student: Gate.

Gate and body it cannot go through because there is a depletion region on one side and this oxide region on the other side. So, this charged must have gotten squeezed out through source and drain.

Either the source or the drain or.

Student: Both.

Both. So, without doing you know any more complicated calculations it is at this point impossible to figure out how much of the charge went towards the left and how much went towards the.

Student: Right.

Right you understand because it must clearly depend on the nature of the impedances of the on the left side and the.

Student: Right side.

Right side you understand. So, there was some non-linear amount of channel charge when the switch is conducting, when the switch will conducting of course, just before it was turned off the voltage across the whole capacitor was V in. Then we turned the switch off and some fraction which we as yet do not know of the channel charge has gone and lodged itself on the capacitor correct. So, if this is c that amount of channel charge will cause a voltage jump of value the injected charge.

So, this is call charge injection because the channel charge when the switch is turned off at least from the little we know about devices we are not in a position to predict how much goes back into the source and how much goes into the into the sampling capacitance. And this point one thing we can definitely say is that some unknown fraction which could change depending on the input perhaps of the channel charge gets on to the hold capacitor is this clear.

So, if some unknown charge f 1 which has we have already discuss is a function of the input voltage gets on to the whole capacitor that will result in a change in the capacitor voltage by value f 1 of v in divided by c and this therefore, represents an error in the held value does it make sense. So, what do you think we can do about this any suggestions ideally want to make the error as small as possible see that two problems with the error cause by charge injection one is. Of course, it is not the signal that you want to you want to have sampled right and two more importantly perhaps this error is a non-linear function of the.

Student: Input.

Input that you are trying to sample many times in electronics you will find that if something is linear even though there is a gain error for example, right it is usually not problematic in a system because gain errors and offset can be corrected at a system level alright. So, for example, instead of V in if I measure always V in plus 1 milli Volt this is usually not a problem because I know that the error is constant and does not depend on input.

The moment the errors starts to depend on V in, in a non-linear fashion then it appears as if the input is getting distorted right, which in fact, is a problem in MOS systems you understand. So, as far as we are concern now we have two problems with the error one of course, is that it is causing loss of accuracy and more importantly this error is nonlinearly dependent on the input voltage. So, the question is what do you think we can do about this, one tempting thing to say is that I will increase my sampling capacitance any comments on that.

Student: If you increase sampling capacitance speed we need increase a resistor decreases the resistance after you have to increase the switch size again channel charge will increases.

So, please note that increasing the sampling capacitance is not does not solve the problem because if we increase the sampling capacitance the RC time constant will remain will now change; the RC time constant will become larger if we keep the same switch. So, in an attempt to bring the RC time constant back to this same value in order to have the same tracking bandwidth as we had earlier the resistance of the switch has to.

Student: Decrease.

Decrease which means if the size of the switch has to.

Student: Increase.

Increase, which means that there is more charge in the channel I mean finally, please note that the low I mean the low resistance of the of the MOS transistor is fundamentally due to the large amount of channel charge present you understand. So, there is no way of reducing resistance while having the same amount of channel charge.

Student: Sir while MOS is training on this charge set complete and then it is going out right, so we canceling.

No, no, no, no, but what you are looking at is the held value on the capacitor is it not. So, what you are interested in is the final value which is stored on this capacitor after you open the switch.

Student: But, when we close the switch.

When you close the switch of course, this needs charge and some unknown fraction again of that charge will come from the left and some of it will come from the right it is likely that it compensates, but that does not really help me. Because I have already you know use the information I mean all the information is on the held value correct, the fact that when I turn it on you know something comes back does not help me because input might have changed you understand.

Student: Sir, function of these inputs.

So, the input has changed right I need to estimate the input with that was there in the previous clock cycle correct. Now, it is true that when I turn the switch on the next time around some of this may actually go back the injected charge, but that does not help because the input has changed.

Student: Sir what if the sampling frequency was it is an all sampled time going to be held because input has cannot change much between the.

No, not really because during the next sampling period you are I mean you are you are

you are you are still sampling is it not. So, the all the information is in the that has is the whole mode voltage right the held voltage is simply the input plus some injected component. So, one thing that is that is apparent is that increasing the size of the sampling capacitor is not really helping, because in order to maintain the same time constant you want to make sure that this error is…

I mean you got to make sure that the resistance of the switch scales in the same manner has the capacitance we choose bring us back to an increased amount of injected charge and increased capacitance the 2 cancel out alright. So, as I said in electronic system design often gain or offset errors are a benign errors in the sense that there offset can of course, be corrected given its constant from cycle to cycle gain error can be is often acceptable because it is a linear phenomena right.

So, we know that we now cannot use this kind of sampling scheme without incurring significant nonlinearity in the form of charge injection, but we will at a pinch be willing to accept a solution where the there is an error. But, in that error is either a linear error in the form of a gain error or in the form of offset then we would not be to worried about. So, finally, in order to sample or an hold on to this capacitor c they must be a switch somewhere correct.

So, one way of thinking about this is to say we already have a switch here earlier the bottom plate of the capacitor was being connected to ground correct. I mean in principle there is nothing wrong if I use another switch in the bottom plate, correct I mean you might wonder why use two switches when one is good enough is it not right.

So, this is exactly identical to having in principle there is no difference between this and the earlier circuit where you had only one switch both are them accomplish the job, but there is. And finally, if you want to implement this with switches with transistors this is probably what we would do can you comment on the charge in this transistor and the charge in this transistor.

Output depends on this input signal ((Refer Time: 28:27))

This charges.

Student: Instead of being.

W L times C ox times V D D minus V in minus V t right this was this is basically some function of V in whereas, what is charge in this channel, it is some constant Q naught which is independent of the input correct. So, even though in principle these two you know switches seem to be do this doing the same thing and we do not seem to be gaining anything from these having two switches rather than one. We see that there is a crucial difference a crucial difference is that the charge in this switch is input dependent.

Where as the charge in the bottom switch a switch in the bottom plate is independent of the input all right. So, we have turn both these switches on in order to sample the input voltage on the capacitor c then we need to in order for the input to be held we need to open the switch. So, what do you think we should do, we would turn both the switches off. So, is there you know do you think I mean; obviously, you can either turn the top switch off first and the bottom switch later or vice versa or both at the same instant of time. So, what do you think is a reasonable thing to do.

Student: Sir bottom could be turned off first.

So, and why would that help.

Student: In that while turning off it switch that charge will not.

Very good, so it make sense to turn off the bottom plate first right. So, you turn this off first. So, what happens when you turn the lower plate off again some part of this channel charge will go to the left and some of it will go to the right we do not know what fraction goes where. So however, the charge in this channel is constant and independent of the input, which means that this injected charge will cause an error on the capacitor voltage and that error will be q injected divided by c with the difference from the earlier case being that Q injected is independent of the input does it make sense alright.

So, now, if this transistors turned off this is the situation we have here, the top switch is still on right and we are getting ready to turn it off and there is a charge in the channel which is nonlinearly dependent on the input, now when you turn this off what do you think will happened to this charge. Whatever we know or we do not know about the dynamic of charge injection one thing is for sure if on one side there is an open circuit.

Student: Charge cannot flow in that

Charge cannot flow in that direction. So, now, when you turn it off all this charge which is signal independent goes into the source. So, the voltage on the capacitor is basically the input voltage minus Q inject by c, so there is an error on the sample voltage however, this error is, is independent of the.

Student: Input.

Input. So, this is another very crucial circuit technique that is used routinely in a switch capacitor circuits.

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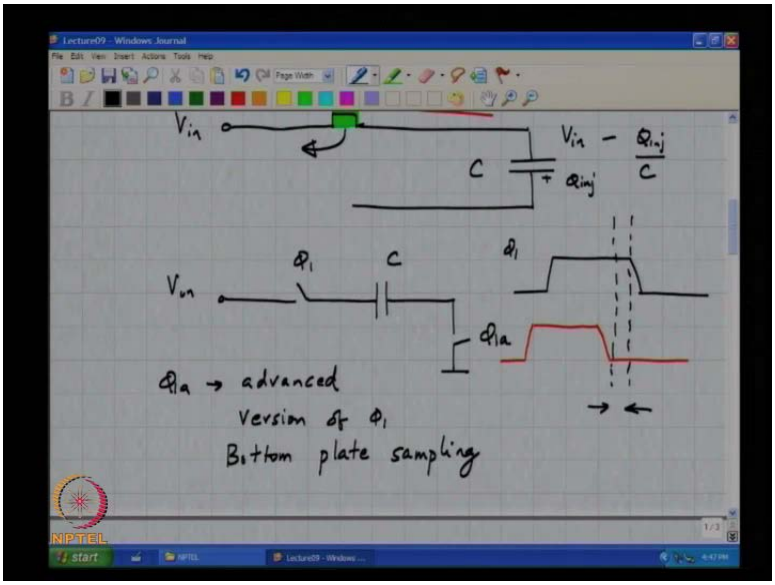

And this is called bottom plate sampling often drawn in this way. So, this is phi 1 and this is often called phi 1 a where phi 1 a. So, this is phi 1, phi 1 a is something which needs to fall to 0 before phi 1 falls to 0 right and the reason for calling this phi 1 a is an advanced version of phi one. So, phi 1 a is an advanced yes is it required to

Student: Ground the bottom plate as a capacitor once you to once you open that phi 1.

Once you open phi 1 [FL], so once you open phi 1 the capacitor is floating.

Student: Both ends are floating

Both ends are floating which is a perfectly legal thing to do right, how it is going to be use there that we can figure out later right because you have these two ends I mean we now can think of this as you have a capacitor with some voltage across it right. Now, this

voltage is a good reproduction of the voltage you wanted to sample now what you do with this floating capacitor is upto you understand. In fact, this is exactly what you want you want a capacitor with both terminals accessible with the voltage you want on the capacitor if you had the you mean, if you had a grounded capacitor that is constraining you in some respect right because you are now constraint to work with the capacitor where 1 terminal is at.

Student: Ground.

Ground you understand I mean it is as a somebody took the input voltage converted into charge put that charge on these two plates and gave that capacitor to you right, now how you use it is upto you.

Student: Sir

Yes

Student: Suddenly I think the bottom transistors charge is fixed when its independent of V in.

Yes

Student: But the fraction of charge that is going into the c

Correct

Student: Why should not be constant because the.

Well the fraction of charge that goes into c will I mean it turns out that it depends only on the ratio of the impedances its see here on the left to the impedances its see on the on their right for one the impedances it is see on the left is very, very low because it is, is ground right. So, most of it will go to the left right a small amount will go to the right and that impedance remains largely fixed regardless of the input.

Student: Because impedance seem the other side is not only sealed, but also the further way assistance of the transistor.

It is there it is there resistances so

Student: The resistance is varying the speed.

That is very mildly with this thing and more importantly the impedance of the source.

Student: Source itself.

Is also there that you assume to be constant and does not change with input right. So, this fraction you know charge you know is a very, very I mean you are worried now about the change in the fraction of the small injected charge which is independent of the input right and that turns out to be extremely small. I mean charge injection MOS switches is a is a problem that has been addressed you know in many ways. So, you can actually write the complicated differential equations that govern the MOSFET and you know the depending on the gate wave form and all this you can actually go and calculate how much charge goes which side.

But unfortunately that analysis is not really useful right of course, usually inside into MOSFET operation and all this stuff, but there is no point in analyzing a complicated problem when a simple solution exists correct you understand. And if there is no point in trying to figure out you know in how many ways you can fall right, the solution is to work carefully you understand as a lot easier thing to do and you know write by computer code to figure out what will happen when you know you make a wrong put a wrong step.

So, this is one of those things you can write a lot of interesting stuff about what how much a charge goes where, but you know that charge injection is not desired correct and there is an easy way of fixing it. And it turns out this simple thing is a is a what is called bottom plate sampling and is a very, very common. In fact, universally used in all switch capacitor circuits, when you want to sample a voltage on a capacitor you always turn off the bottom plate first.

Now, one question that you might ask is how much time do I need between turning off the bottom plate and turning off the top plate I mean you know I inverted delay is all that is needed. So, these do not have to be big delays a small delay is good enough.

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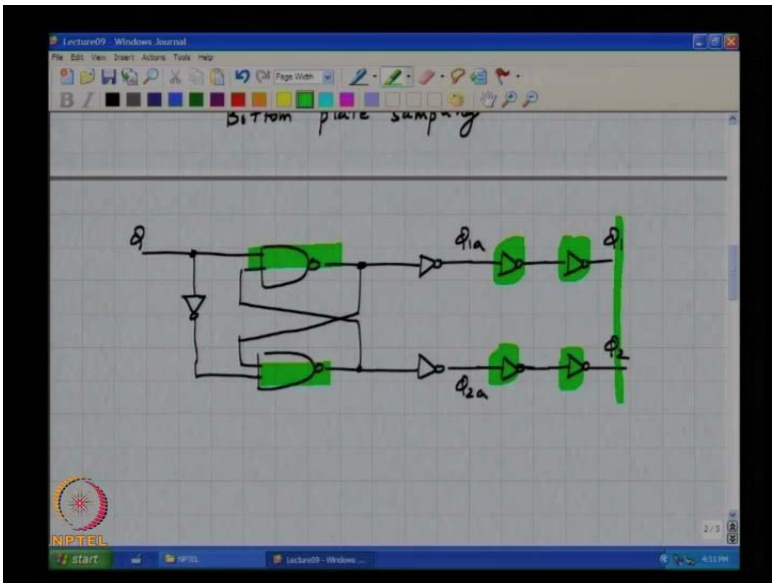

So, often the clock generator as you can see now is becoming more and more complicated this is the core of the non overlapping clock generator phi 1 and phi 2 are non overlapping clocks. Now, you want phi 1 bar these are the complements and so if you call this phi 1 and you call this phi 2 both of them are still non overlapping you understand please note that these two are non overlapping, so these two are non overlapping non overlapping too.

So obviously, it is impossible to advance a clock in I mean you cannot advance a signal you can only delay it right, but since. So, if you call this phi 1 you can call this is not as if you derive phi 1 a from phi 1 you derive phi 1 from phi 1 a you understand. So, this is you can call this phi 1 a and phi 2 a both are advanced versions of phi 1 and phi 2 and you can generate compliments by you know I mean by picking of you know this signal and so on you understand.

And you can also play around with the delays of these inverters right to play around with the time you have to advance phi 1 a with respect to phi 1. And then the delays of these NAND gates will tell you how much non overlapped time you have between phi 1 and phi 2. And finally, these clocks will be use by several blocks it is not as if you know you just generate 1 phi 1 and phi 2, for example, in the various switches we have seen we have seen that some switches need phi 1, some need phi 1 bar, some need phi 2 bar all sorts of stuff.

So, it is not as if these inverters will be driving only you know one inverter loader something like that, often these also had to be you know will be use by other blocks in the A to D converter, so there will be a significantly load on the clock generator. So, you need to put adequately strong digital buffers to make sure that the various blocks which need phi 1 and phi 2 are being supplied with these signals without degradation to much of rise and fall times.

And of course, you must also make sure that whatever queues you have in the clock generator are or non overlap times you have in the clock generator are reasonably accurately reproduced at the site. Where you want that you understand, which means that the drivers which sense the signals and drive the logic gates must a be sufficiently strong and he was make sure that the, this queues between those driverses as small as possible. So, that you do not you do not mess with the what you call the time in relationships between the clocks at the clock generator and verses what happens later is this clear all right so.

Student: Sir

Yes

How do we find the other MOSFET when that bottom plate that MOSFET since ((Refer Time: 44:17)).

Well the question is how will you size this transistor and this transistor.

Student: I mean the one in this the phi 1 I know that depends upon the

No now the what do you think is the tracking bandwidth.

Student: Yes sir

Student: That will determinate by phi 1 a.

No it will be determinate by both phi 1 a and

Student: Advanced phi 1.

The now the you think of these as 2 resistors in series right, so you have to make the resistor sufficiently small, so that you hit the tracking bandwidth. And this also brings out

another a minor point that is you do not need to make the switches any larger than is necessary. Let us say you have a speck on tracking bandwidth all right you have some safety margin all right and you decide to choose a certain switch size.

Now, there is no point in choosing phi times switch size and why because it does not help you know you know improve on your speck in any, I means you are tracking bandwidth speck is so much. And some size plus safety margin allows you to reach that speck, choosing a switch size which is much larger than what is necessary is often contour productive for couple of reasons.

One is that charge injection will unnecessarily increase you understand we all understand that the there is charge injection, because of the of the bottom plate switch if you make the switch much too large compare to what is actually required all that it means is that the amount of charge injected will be more. It is still independent of the input signal and all that, but it is unnecessary a further problem is that somebody has to drive these control signals you understand.

So, if you go on blindly thinking bigger is better and make switches which are you know much larger then there then are really required then you will end up the situation where the clock generator right. Will now have drive huge capacitive loads and those drivers will start to guzzle a lot of power completely unnecessary because you did not need such big switches in the first place.

So, the strategy to make the circuits work is a choose features which are you know large enough, but do not over do it if switch size is too small things will not track properly if the switch size is too big you will unnecessarily end up with charge injection problems. As well as unnecessarily driving you know a lot of parasitic capacitance now which will lead to lot of unnecessary power dissipation you understand. So, going forward in the next class what we will do is you see the following I mean we have learnt now to design a very crude sample and hold.

In other words we learnt how to take continuous time input signal right and sample it on a capacitor without too much a either distortion or charge injection. So, you know when we design a circuit like this the first thing we did be interested in is figuring out how good is it I mean how good is good right. You must have some metric or we must have way of figuring out how good a sample and hold and how linear a sample and hold will

make you understand.

So, if you are given an amplifier which operates completely in continuous time and told go and measure how linear this amplifier is what do you think you will do, here is an amplifier I am clamming it is very linear I am selling to you how will you make sure that I am not lying to you what will you do for what test will you subject the amplifier to make sure that the linearity I promise is indeed there.

Student: ((Refer Time: 48:49))

So, a common thing to do is to apply a sinusoid which itself must be very clean right and then look at the output if I am indeed giving you a linear system as I claimed the output should also be sinusoidal and it must be free of harmonics.

Student: Sir harmonics

Harmonics because a linear system by definition cannot produce harmonics. So, the level I mean no real system will be perfectly linear, so it is only a matter of how small the harmonics are. So, if have within codes of very linear system I can expect that for a given agreed upon input amplitude the level of the or the amplitude of the harmonics is very, very small right.

So, in other words putting a harmonic sinusoidal input and measuring the harmonic strengths is a standard well known well accepted way of measuring the linearity of a system, which operates in continuous time. Now, we have got a slightly different problem we need to find the linearity right; however, the input is the input is continuous time whereas, the sample output is naturally discrete time and we would like to since you have been comfortable with using you know sinusoidal test signals to measure linearity.

We would like to be able to do the same thing even for this particular system we would like to put in a clean pure sinusoid and measure within codes if possible the harmonic distortion that occurs at the in the samples of the sample and hold you understand. But, there is something that we need to be aware of one thing is that if you take a sinusoid in continuous time which is naturally you know periodic and you sample it the discrete time sequence as we have seen need not be…

Even though the input continuous time signal is periodic once you sample it at some rate

f s the result in discrete time sequence need not be periodic. So, A I mean if this discrete time sequence is not periodic then it hardly make sense to talk about harmonics because a non periodic signal I mean what does the meaning of harmonics and all this. It means a I mean harmonics or distortion is a simple way of saying this following complicated thing I take the output of a continuous time system decompose this into Fourier series right.

And give you the Fourier coefficients that is what a harmonic distortion test is right, if the discrete time sequence is not periodic then it does not make any sense at all. So, there must be some way of choosing because not all input sinusoids after sampling will result in a periodic sequence we must find or we must be able to excite the sample and hold with only those sinusoids which after sampling will give us a periodic sequence.