VLSI Data Conversion Circuits
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Lecture - 8
Gate Boosted Switches - 2

This is VLSI Data Conversion Circuits lecture 8. In the last class we were looking at ways of making, the sampling switch, linear, in other words the device that we are familiar with which can be used as a switch, dependent on an external control signal is the MOS transistor. This input voltage needs to be sampled and held on this sampling capacitor, and the basic idea is during the sample phase, the switch is turned on by connecting this to a high voltage, and when you want to hold the voltage you just turn the switch off, so that the input is sampled on the capacitor.

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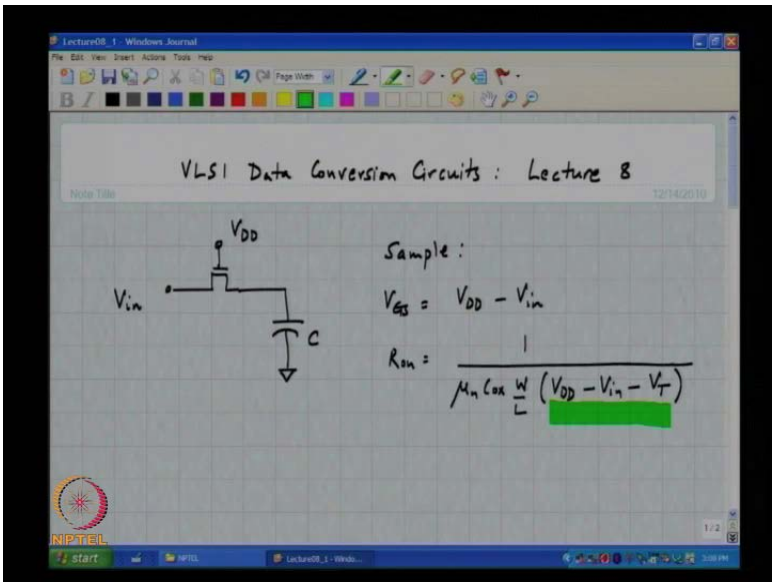

And we were looking at the various non idealities that could happen during this whole process, and one thing that was responsible for distortion was the variation of the resistance of the switch. And why does the resistance of the switch vary, if as we are normally used to we connect this voltage to VDD, during the sample phase or the during the track phase, the MOS transistor has a resistance which unfortunately depends on v g s minus.

Student: V

V t. Now, the v g s of this transistors, so during the sample phase the v g s is nothing but, VDD minus v in, so the gate over drive is v g s minus v t, which is VDD minus v in minus v t. And the resistance of the switch, therefore is given by 1 over mu n C ox W by L times v g s minus v t, for the time being we neglect, the fact that v t is also modulated by the input voltage through the.

Student: Body.

Through the body effect. So, when we are discussing this the last time around, we said that there is a fix for this, and the fix actually quite straight forward, when you look at the expression you see that the problem of distortion is occurring, because the resistance of the switch is getting modulated by the input signal. So, the fix chooses problem is to prevent the resistance from getting modulated by the input signal, and how do you prevent the resistance from getting modulated by the input signal, the culprit is this character.

So, we see that, the gate is being held at a fixed voltage VDD in order to turn it on, unfortunately the source voltage is the input voltage and is varying with time, therefore if the gate is held at a fixed potential in order to turn the device on, v g s is varying. So, this suggests the solution of.

Student: ((Refer Time: 03:32)).

We do not want to keep the voltage of the gate at a fixed potential, we want on the other hand we want v g s to be.

Student: Constant.

Student: Constant.

Constant, not v g.

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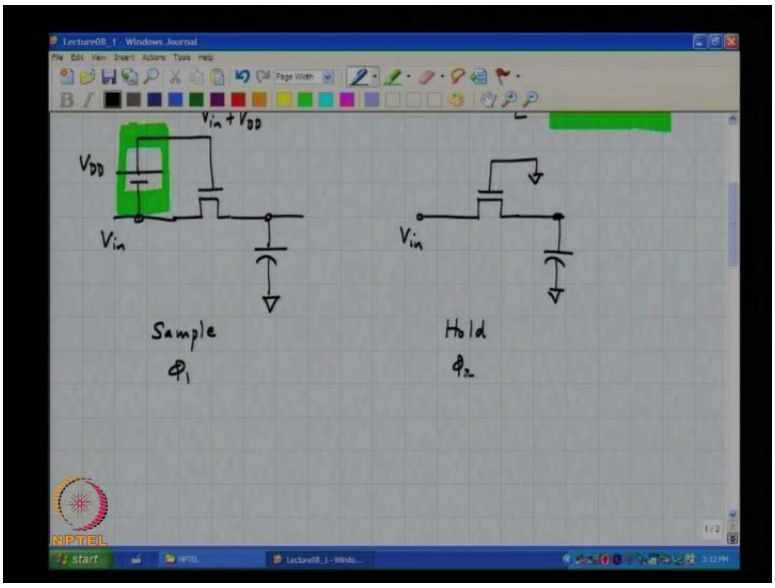

So, basically in the sample phase, what we do want is to keep v g s fixed, which is accomplished in principle by putting a battery of value VDD between the gate and the source. This way the absolute potential of the gate will be what.

Student: v plus VDD.

It will be V in plus VDD, which means that the gate source voltage is simply VDD quite independent of the signal v, this way the resistance of the transistor of the switch becomes independent of the input signal, and therefore nonlinearity is avoided. We have seen expressions earlier for the second and third harmonic distortion, where the resistance varies as a function of the input signal.

And the strategy used here which used to make sense, is to say the problem is coming because the resistance is varying with the signal, so in order to solve the problem you make sure that the resistance of the switch remains constant, independent of the signal. And how do you keep the resistance of the switch independent of the signal, when the gate, when the source moves the source is connected to the input, the gate also moves by exactly the same amount, there by v g s remains a constant.

Again I like to bring to your attention that, in this analysis we have neglected this small variation of the v t with respect to the source voltage, and of course, in the whole phase we would like to turn the switch off, and that is done in quite a straight forward manner.

Now, the next question is how would we implement this battery, this is what we are looking at the last time around, and we said that, one important thing that one must observe regarding this battery, is that there is very little current being drawn from the battery.

And further this battery is only needed in.

Student: 1 phase.

In 1 phase, so during the sample phase, during the other phase the battery is not really required. So, from our prior experience in the analog circuits class, a capacitor which is charged to a voltage VDD is indistinguishable from.

Student: ((Refer Time: 06:49)).

A battery of the same voltage provided you do not draw any current from it. And this is particularly convenient, because here we need the battery only for 1 phase, which means that even if the capacitor looses charge, it can be.

Charged replenished.

Replenished in the next phase.

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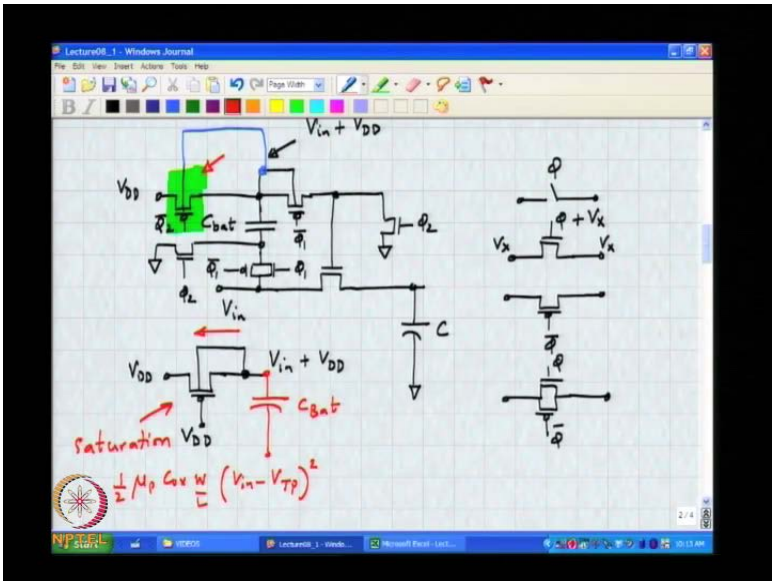

For simplicity I am just going to call the sample phase phi 1, and the hold phase phi 2, and so the in principle diagram of the switch will look something like this. During phi 1, this capacitors C bat is connected between the gate and source of the sampling switch, during phi 2, what to do, what do you want to do.

Student: Propagate.

Student: Propagate.

We want to connect C bat across.

Student: ((refer time: 08:16)).

Student: Propagate.

Student: VDD.

voltage source of value VDD. And what do we do to the gate of the in the sampling switch, during phi 2.

Student: Must be connected to ground.

Must be connected to ground, now the question is how do we implement these switches. So, we have 5 switches in all, which also need to be implemented with transistors, and let us just quickly recall. That if we want to have a switch which has to be turned on during any phase phi, there are at least 3 ways of doing it, one is to use an N MOS transistor, whose gate is clocked it by. Another one is to use a p fet, whose gate is clocked with.

Student: Phi bar.

Student: Phi bar.

Phi bar, and the third one is to use a combination of the 2 also called the transmission gate. Let us also quickly remind ourselves, where each one of these possibilities makes sense, so when would you like to use, switch number 1 which is the N MOS transistor clocked with phi.

Student: ((Refer Time: 10:25)) Corollary.

It makes sense to use when.

Student: ((Refer Time: 10:29)).

In after all you are trying to equalize these 2 voltages, so N MOS transistor make sense when v x is.

Student: Close the ((Refer Time: 10:38))

Is very low typically close to ground, on the other hand a P MOS transistor make sense when.

Student: Phi.

Student: Trying equalize the.

When the voltages you are trying to equalize are.

Student: High.

Both high or both close to VDD, in several circumstances you have a situation where the voltages that you at the 2 ends of the switch, it can vary from.

Student: ((Refer Time: 11:07)).

All the way from low to high, I mean a classic case in point is they are very input signal, which can in principle take on different values as a function of time, in which case it make sense to use a transmission here, is this clear. Now, let us start with the switches, so what would you do for this switch.

Student: ((Refer Time: 11:34)) of the mos.

They are great it make sense to use, an N MOS transistor clocked with.

Student: Phi

Student: Phi.

Student: Phi 2.

Phi 2. what about this switch.

Student: Transmission.

Student: Transmission.

Here it make sense to use a transmission gate, simply because the input can vary all the way from.

Student: 0 to VDD.

0 to VDD, may be not all the way from 0 to all the way to VDD, but sufficiently closer, so instead of this we have a transmission gate. So, where will the gate of the N MOS transistor go in the transmission gate.

Student: ((Refer Time: 12:35)).

Psi 1, how about the gate of the P MOS.

Student: Phi 1 bar.

Phi 1 bar, what about this switch here.

Student: N MOS.

Student: N MOS.

Student: N MOS.

That is also an N MOS transistor, but where does the gate go.

Student: Phi 2.

Phi 2, what about this is a difficult switch, let us let us start with this, where do you think that switch will go, how do you implement that, we do not know we go through all the 3 possibilities see which works. So, let us see if the N MOS switch works there, can I have any comments what do you think.

Student: No.

Student: No.

No, why.

Student: Because the voltage can be higher than the V D D.

So, clearly the minimum value of this voltage is.

Student: VDD.

Student: VDD.

VDD, please note that this battery capacitor c bat is charged to VDD, so the minimum value of the top plate of that capacitor is at VDD. So, clearly it does not make sense to use an N MOS transistor, which also means that the transmission gate must be removed from the picture, because if the N MOS is not doing anything. Even, if you put it along with the P MOS, it is not doing anything, which means that if the N MOS is out of question, it must also follow that the transmission gate is out of question. The only possibility left seems to be the.

Student: P MOS.

P MOS transistor and definitely the voltage is high, so it seems like a P MOS transistor will help. Now so, let us now replace this with the P MOS transistor, and see if it indeed works as expected and this must be clocked with.

Student: Phi 1 bar.

Student: Phi 1 bar.

Phi.

Student: phi 1 bar

Phi 1 bar that is correct. Now, a P MOS transistor has 4 terminals, the 4 terminal being the body, and what do we know about the body terminal, what should we do with it is potential.

Student: ((Refer Time: 15:12)).

The by terminal of the P MOS transistor must always be connected to the.

Student: High.

Student: Higher.

Highest possible potential, that the transistor is exposed to, and which is the highest possible potential that the transistor is exposed to.

Student: Half rate of b capacitor.

Student: V v d.

Student: VDD.

So, this voltage is VDD plus V in, this voltage is either VDD plus V in.

Student: Or ground.

Or.

Student: Ground.

Ground correct, so which do you think where do you think you connect the body.

Student: ((Refer Time: 15:48)) VDD test.

Student: Top.

Student: Top.

So, you will good, so you will connect it to the left side, please note that this is somewhat of a departure from normal practice, normally in digital circuits what would you do you would without thinking, simply connect the body of the P MOS transistor to VDD. And the body of the N MOS transistors in many technologies, you do not have any choice at all, it is automatically ground. And why do you normally connect the body of the P MOS transistor to VDD.

Student: ((Refer Time: 16:33)).

Because, you expect that no node voltage inside the circuit exceeds VDD, so VDD is a safe place to tie the body of the P MOS transistor. In this case; however, clearly the potential of this node exceeds.

Student: In VDD.

Student: VDD.

VDD. So, you cannot simply tie the body of the P MOS transistor to VDD, you need to tie it to the highest potential that the transistor is likely to see, and in this particular case that happens to be VDD plus V in. And quite luckily, in fact this potential always occurs at the same node on the left side, you understand it turns out, as we you will see going forward, that we will not be, so lucky with the last switch, which is the 1 highlighted in green. So, what do you think, we should use for this switch, again the answer is not immediately apparent, we go through.

Student: ((Refer Time: 17:51)).

What we know which are these 3 switches, if one of them works, it is fine we are done, if none of them work we figure out what to do. So, let us start with the pure N MOS, how many votes for the pure N MOS ((Refer Time: 18:16)), why.

Student: Because the ((Refer Time: 18:19)), so high.

The potential is too high, so N MOS is not helping, if the N MOS is not helping the transmission gate can hardly be used, so it seems like.

Student: P MOS is absent.

P MOS is the only candidate which even remotely fits the job description. So, now, let us try and see if P MOS works, and where would you connect the gate 2.

Student: Phi 2 bar.

Student: Phi 2.

Student: Phi 2 bar.

Student: Phi 2.

Phi 2.

Student: Bar.

Phi 2 bar, now there is the 4 th terminal called the body, and we need to figure out where to tie the body, the body must be tied to the highest potential that this transistor is ever likely to see. So, can you now comment on what that highest potential will be, so clearly this voltage here is going to be v in plus VDD, simply because the battery is c bat has been charged to VDD in a previous cycle.

So, one would, therefore conclude that a reasonable strategy would be to simply connect the body of the P MOS transistor, to the highest potential namely this; however, if we think over it carefully there is a problem due to the following. So, this voltage is v in plus VDD, when this switch here is supposed to be off, how would the terminal voltages look like 1 terminal would be at VDD, I am simply redrawing this switch to focus exclusively on this.

To turn it off one would normally connect the gate to VDD, and this node would be at V in plus VDD, since V in plus VDD is indeed the highest potential that any of these terminals will see, it is quite legal to connect the body of the transistor to V in plus VDD. Unfortunately; however, while we are interested in keeping the various junctions reverse biased, we are also interested in making sure that there is no drain current at all.

Unfortunately, as we can see here this is not true, because this potential is v in plus VDD, and these 2 potentials are at VDD each, which is equivalent to having the transistor operate in the saturation region, with the source gate voltage of V in. So, this is V in plus VDD, this is VDD, and this is VDD, which therefore means that when this switch is supposed to be off, it will actually start to remove current from c bat, because c bat is connected here, and is at a potential V in plus VDD.

And because this transistor is in saturation now, we see that this will draw away current, which is and the current is given by 1 half mu p c ox W by L times V in minus v t p the whole square. And this is completely undesirable, because you want the battery to hold on to that voltage VDD without loosing that voltage, and therefore using a P MOS which here is also not a permissible solution. So, we now need to figure out what to do, because it seems as if the various features we know namely the N MOS transistor, the P MOS transistor or the pass gate, none of them are suitable for use in this situation.

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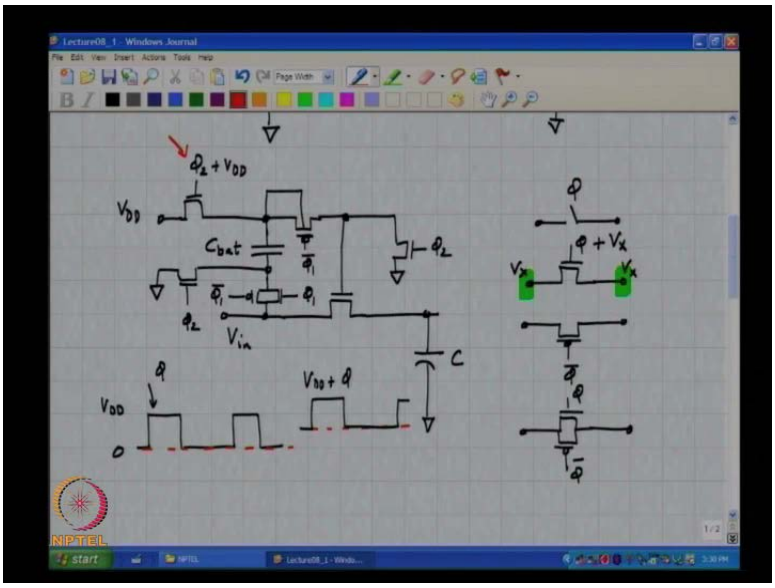

So, now let us the stuff that we have the 3 switches, that we have do not work, so let us now go back to 1 of the switches, and see what can be done to make it work, you understand. So, let us recall for the N MOS switch, if this is v x the minimum voltage required to make this turn on, is what.

Student: V t plus v x.

Student: V x plus.

I mean it is v x plus v t, but if you want a good switch we normally, you know used to the fact that this v g s is VDD, so in other words if this was ground, if v x was 0 the gate would be connected to VDD, in order to make it a within quotes good switch. Now, if v x is not 0, but something higher, but you want to make the switch just as good, what do you think you should do to the gate.

Student: ((Refer Time: 24:02)).

I mean it seems like if VDD was good enough for v x equal to 0, then if v x was non 0, what I would apply at the gate would be the non 0 voltage plus.

Student: VDD.

Student: VDD.

A VDD. See in a similar fashion, if you want to turn off the switch if v x was 0, what would you connect the gate to.

Student: ((Refer Time: 24:30)) ground.

Normally, you would connect it to ground.

Student: Ground.

Now, if this if this v x was non 0, what do you think you could do.

Student: But non 0 connect.

Student: connected.

Student: Connected.

You could have connected to either to.

Student: Ground.

Ground or you could connect it to.

Student: Non 0.

V x in other words, you do not need to connect it to ground where the gate shows voltage it become negative, a v g s was 0 is good enough to turn the switch on. In other words if v x is non 0, then this will work just as well as a regular N MOS, which would have worked at v x equal to 0, if instead of applying phi at the gate, where phi goes from 0 to.

Student: VDD

VDD, I apply.

Phi ((Refer Time: 25:23)).

Phi plus.

Student: V x.

V x, in other words earlier v x was 0, and phi would go from 0 to VDD with v x being 0, now v x is non 0 something which definitely works is adding that same non 0 component to 2 phi does it make sense, so this is phi and this is VDD plus. Now, let us focus, therefore based and to this information, let us focus on this switch, so v x is now.

Student: VDD.

Student: VDD.

The 2 potentials that we want to make the same are VDD, so what should happen to the gate, based on our discussion just now.

Student: ((Refer Time: 26:42)). Plus 2 VDD's.

Instead of having phi 2, what should we do, you must have.

Student: Phi 2 plus.

Phi 2 plus.

Student: VDD.

VDD, so the next question is how would you generate phi 2 plus VDD.

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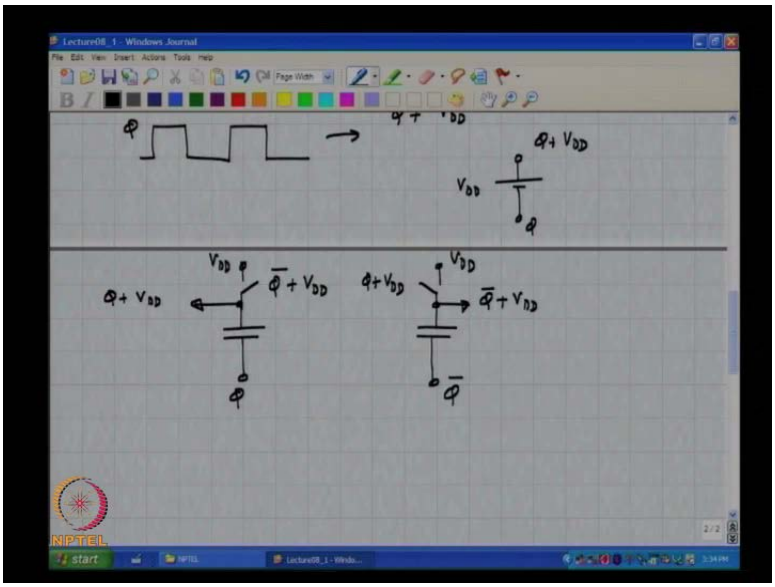

So, let us say you have a clock, phi and you are faced to the general problem of generating, phi plus VDD, what would you do, I mean in principle what would you do.

Student: ((Refer Time: 27:55)).

So, if you have phi, then to generate phi plus VDD, if I add a voltage source of value VDD or a battery of value VDD, this voltage will simply be phi plus VDD. Now, we resort to the usual trick of how do we implement the battery, or what do we do what do you think we can do.

Student: ((Refer Time: 28:24)).

The usual thing of taking capacitor charge it to VDD, and so if there was a capacitor, and this end was tied to phi, when phi was 0, and phi is 0, when phi is low the capacitor must be charged to.

Student: VDD.

Student: VDD

VDD. So, how will you charge this, and by with what signal must the gate be controlled, when phi is low this switch must be open or closed.

Student: Closed.

Student: Closed.

Closed, so it means that it must be controlled by it must be high, it must be closed when phi is low which means that it must be.

Student: Controlled.

Controlled by phi bar; however, please note that we are faced with the same problem all over again, because this switch needs to equalize 2 nodes with voltage VDD. So, in other words this must need phi bar plus VDD, we tried to generate phi plus VDD, and then we found that or rather we are finding that in order to generate phi plus VDD, we need.

Student: Phi bar plus.

Phi bar plus.

Student: VDD.

VDD, so then you say let me try and generate.

Student: Phi bar.

If I had instead tried to generate phi bar plus VDD, I would have needed.

Student: Phi plus VDD.

Phi plus VDD, you understand this is a situation where I have phi, but I need phi bar plus VDD, now if I imagine that I needed phi bar plus VDD, then what would I have to do, I put phi bar here, and this switch would be controlled by.

Student: Phi plus ((Refer Time: 30:50)).

Student: Phi plus VDD.

Phi plus VDD, and this would give me what signal.

Student: Phi plus VDD.

Phi plus VDD, and this would give me phi bar plus VDD. So, now, putting 2 into together, what do you think we can do, the circuit on the left has got something, but needs the compliment, the circuit on the right has got the compliment, but needs you know phi plus VDD.

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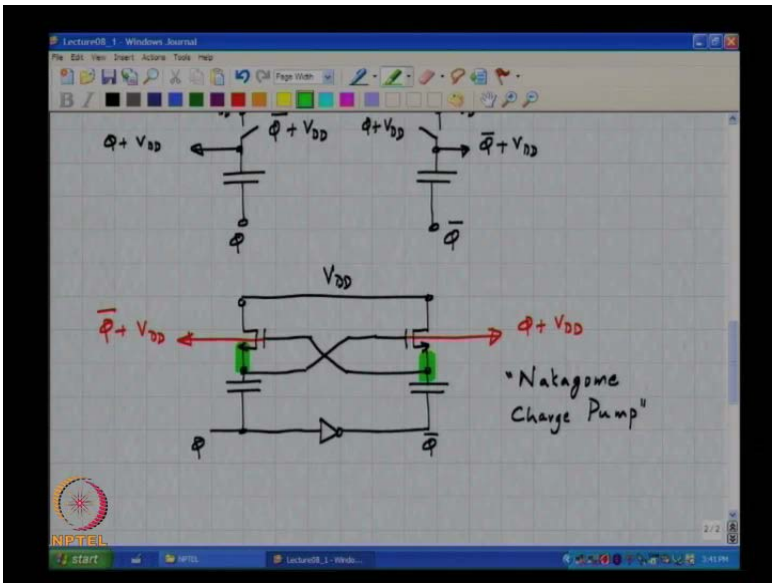


So, now if you now marry these 2 circuits together, hopefully we will be able to get both phi plus VDD and.

Student: Phi bar plus VDD.

Phi bar plus VDD, and that is precisely, what we are going to do, and this is phi, if you generate phi bar it is straight forward, you just put an inverter, does it make sense and let us kind of quickly trace the circuit and see what happens. When phi is 0, what is the absolute voltage of the output of this inverter.

Student: VDD ((refer time: 32:50)).

It is VDD, let us assume both the capacitors are initially.

Student: Uncharged.

Uncharged, so what is the voltage at the top plate of the left capacitor.

Student: 0.

Student: 0 plus VDD.

It is 0, what happens to the voltage at this point.

Student: ((Refer Time: 33:17)).

The capacitor is uncharged, so this absolute potential will be.

Student: VDD.

VDD, now consider this transistor, the gate is at VDD, the drain is at VDD, so what will eventually happen to this capacitor.

Student: ((Refer Time: 33:36)).

What will that potential eventually.

Student: ((Refer Time: 33:39)).

Reach.

Student: VDD minus.

Student: VDD minus v t.

It will reach VDD minus.

Student: VDD.

V t, it will not go to VDD, because the transistor will turn off the moment it goes to VDD minus v t. Now, that the state of phi has changed it has gone to from 0 to 1 which means the absolute voltage has gone to VDD, what is the absolute voltage it to a at the output of the inverter.

Student: 0.

Student: 0.

0, what is the absolute voltage at the top plate of the left capacitor.

Student: 2 VDD minus ((Refer Time: 34:16)).

It is 2 VDD minus v t, now if this is 2 VDD minus v t; that means, this potential is 2 VDD minus v t, what happens to this potential now.

Student: ((Refer Time: 34:32)).

Student: VDD plus v t.

It will get charged to.

Student: VDD.

VDD, because the gate is at 2 VDD minus v t, the drain is at VDD, so the source will become VDD, and, so this capacitor is now got in charge to the lower plate is at ground, the upper plate is at.

Student: VDD ((Refer Time: 34:56)).

VDD, so this capacitors got in charge to VDD, now if this is VDD in the next phase what happens to this gate.

Student: 2 VDD.

Student: 2 VDD.

It goes to 2 VDD, which means what happens to this potential.

Student: VDD.

Student: VDD.

This gets charged to VDD. So, now, we see that both the capacitors are charged to, once you run this for a couple of cycles, we see that both these capacitors are charged to.

Student: VDD.

VDD, and therefore this way from will be what.

Student: Phi plus VDD.

Here phi plus VDD or phi bar plus VDD.

Student: Phi plus.

Student: Phi plus.

Student: Phi plus VDD.

It is phi plus VDD, and what is this wave form, phi bar plus VDD, as you can see the solution is not a very obvious solution, in fact it is a very elegant circuit, which is not at all immediately obvious. And this is part of what is called a Nakagome charge pump labelled; obviously, after the inventor, this is originally discovered or invented for use in d amps, where apparently high voltage is needed. And if phi and phi bar are complementary, then by muxing between phi bar plus VDD and phi plus VDD you can generate.

Student: Constant.

A constant potential of value.

Student: 2 VDD.

2 VDD. So, this can be in principle used as a by appropriate muxing between phi plus VDD and phi bar plus VDD, used as a voltage doubler, which doubles the supply, so anyway that is not the focus in this course at least, so what we do is therefore.

Student: ((Refer Time: 37:40)) beta kind of analysis material which ((Refer Time: 37:45)).

There is no I mean there's no feed back here.

Student: I mean ((Refer Time: 37:47)) are loop which takes from.

Once, the capacitors are charged, this loop is not pretty much not doing anything, only the only thing that happens is that once, I mean because of the p n junctions at the source, and source here and here. There will be a very, very slow leakage of charge, and all that is happening is that charge is getting replenished every cycle, so once after couple of cycles things the capacitors are charged to VDD there is pretty much, you can almost think of it as batteries which are just holding a VDD.

Student: Sir ((Refer Time: 38:37)) charge of circuit, capacitors and negative voltage.

Well, not quite because if you go through the same analysis that we did before, if the capacitors were charged to a negative voltage, then during in the first cycle, 1 will come up to VDD minus v t the other one.

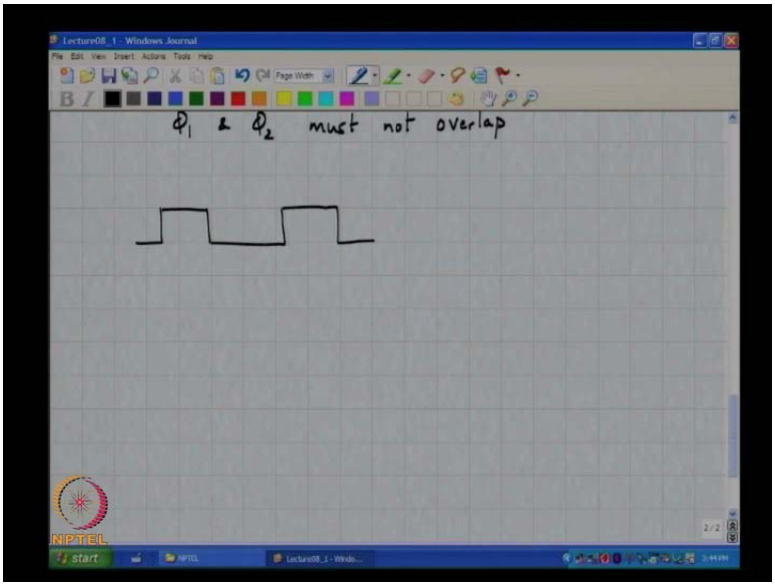
Student: Top plate of capacitors go to the gate of the v g s.

So, after a you know 1 or 2 cycles it will simply settle to the right voltage, so now, that we have established this, then it is straight forward, so one uses the level shifted clocks to go, and clock that switch. Now, the last thing that needs to be done to make this work is what, do we know about phi 1 and phi 2, you want to make sure that when these switches are on, these switches are off and vice versa. So, is extremely important for phi 1 and phi 2 both not to be active at the.

Student: Same time.

Same time.

(Refer Slide Time: 40:02)



So, in other words phi 1 and phi 2 must not overlap of course, one can say allow a chip and then it is your business to send me the non overlapping clocks, but that is hardly an idea that will fly, what you want to do is to take a clock, and internally generate the 2 non overlapping clocks you understand. So, how would you take a clock and generate, so in other words the problem is this you have a clock, from this you need to generate 2 clocks, phi 1 and phi 2 which are.

Student: Non overlapping.

Non overlapping, and of course, using standard state diagrams, it is possible to derive the circuit trans scratch, and this is an asynchronous circuit.

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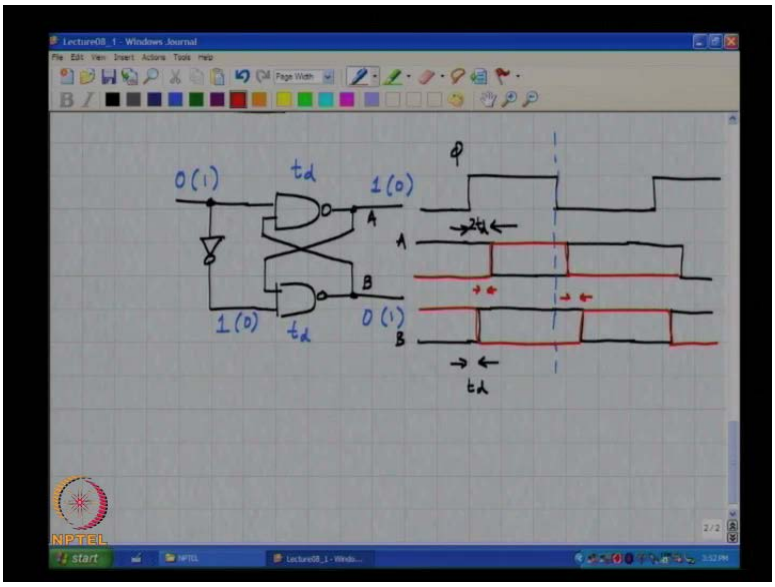


At this sub point I will not do that, I will just quickly show you the core of the circuit and analyse it and show you that it works, and those of you are interested can actually go and see how you can come up with this circuit from first principles. So, the core of the circuit is an R S latch made with NAND gates, for argument sake let us assume that the inverter is delay free, but the 2 NAND gates have delays t d, which are deliberately made large.

Why do you want to make them, why do you think we did want to make them deliberately large, we need to have a control all over the non overlap time between phi 1 and phi 2, if all gates are delay free clearly you know not to turn at all you understand. So, as I will show you in a couple of minutes, this t d is a parameter which controls the amount of dead time between phi 1 going low, and phi 2 going high, so let us quickly analyse this circuit, before we get into the transient part. Let us see what happens in for steady state, if this is 0 and has been 0 for a long time, what will be the logic value here at the output of the inverter, this will be a logical 1, if this is a logical 1, what will be the output of the lower NAND gate.

Student: 0.

Student: 0.

Student: 0.

This will be 0, and this will be 1 is this clear to everybody, so if this is 0, and this has to be 1, if this is 1 and this is 1 this is got to be 0, I mean please note that there is positive feedback loop here. Now, if this changes to 1, and remains there what happens to the logic value at the output of the inverter it is a 0, if this is a 0 what happens to the output of the NAND gate.

Student: It goes to 1.

This will go to 1, and this will go to 0, now let us trace the wave forms as to what happens when phi transitions from.

Student: 0 to 1.

0 to 1 . So, this is the input clock phi, let me call this A, and let me call this B in order to help us identify the signals, so phi let us assume has been 0, for a very long time prior to going up. So, if phi has been 0 for a very long time, what do you think A will look like.

Student: 1.

Student: 1.

A will be a.

Student: 1.

Logical 1 and what about b.

Student: 0.

Student: 0.

B will be a logical 0, so this is phi, this is A, and this is B, now an phi goes up from 0 to 1, what do you think will happen.

Student: ((Refer Time: 45:38)).

When phi goes from 0 to 1, what happens to this NAND gate.

Student: 2 t d.

Student: Within 2 t d equal to 0.

Student: 0 sir.

Student: ((Refer Time: 45:54)).

So, the output of the inverter immediately goes to 0, because we have assumed that the inverter has got.

Student: 0 delay.

0 delay.

Student: B goes goes where after delay of t d.

So, B must go high after a delay.

Student: T d.

T d very good, and after B goes high and after another delay t d, what happens to A.

Student: A goes to 0.

A goes low, so now what happens at the falling edge.

Student: ((Refer Time: 46:21)).

So, life continues on like this, until the next edge comes which happens here, next what happens.

Student: It goes ((Refer Time: 47:07)).

When phi goes low.

Student: A goes.

A goes.

Student: Higher.

High after a delay.

Student: T d.

T d very good, and B goes low.

Student: After another t d.

After another t d, and this keeps repeating itself. So, this is t d and this delay is 2 t d, does it make sense, and how do you get a non lapping set of signals from A and B, you just simply invert A and B, which I will draw in red. A bar and B bar are non overlapping signals, so if a goes low, B goes high only after delay.

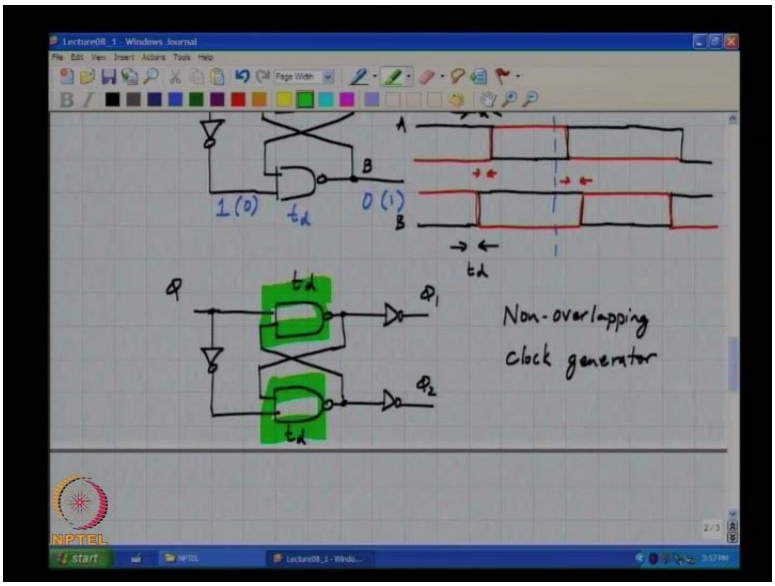
Student: T d.

T d, and after B goes low, there needs to be a delay of t d before A can go high, is this clear, one can also vary the difference between I mean one can vary this delay versus this delay by doing what.

Student: ((Refer Time: 49:23)).

So, if the 2 NAND gates do not have equal delays, then you can change the non overlapping time between B going low and A going high, and make it different from the delay that there exists between A going low and B going high, is this clear.

(Refer Slide Time: 49:52)



So, this is often one of the most commonly used core circuits, used to generate non overlapping blocks you understand, and these are in many cases deliberately made, especially when you are dealing with very low frequency signals. You want to be absolutely sure that, the 2 do not overlap, when the clock rates are not very high you want to be absolutely sure, that there is no overlap between these 2.

And what you do is I mean in very fast technologies, it is often very difficult to get sufficient delay in the gates, so you put a chain of inverters something in casket, you mean this is where you deliberately want to make the gate delay slow. So, that you get an appreciable non overlap time, we are dealing with very high speed designs you often do not have the luxury, because if you waste significant period of the clock for non overlap.

Then I please note that these non overlap times are eating into the total clock period, direct during these times all the switches are open, so if you waste too much of the clock period in these non overlap times. You are; obviously, reducing the amount of time you have for phi 1 being active, and phi 2 being active, so in high speed designs you know you are often you know you try to optimize this.

So, that you would do want non overlap, but you cannot afford to waste a lot of that clock period, just for non overlap in low speed designs often if your clock rate is very low. And then it becomes very I mean you kind of get nervous, when you cannot see the non overlap period on a simulator for example, so in a high speed design if you are designing something at 2 for example, the clock period is 500 picoseconds.

The inverter delays are like 50 to 60 picoseconds, so if you plot phi 1 and phi 2 on a computer, you will definitely be able to see visually the non overlap time. Now, if I suddenly reduce the clock rate to say 2 mega hertz, and use the same circuit the non overlap time will still be the same you know whatever you decided, but now your clock is a 1000 times slower.

So, when you plot the thing you know even though phi 1 and phi 2 are technically non overlapping, you cannot see them anymore and you begin to get nervous, so a normal thing is to say you now if there is a lot of time and you want to be absolutely safe. You put a few more inverters and satisfy yourself, that sure even if things get is cubed, finally it is not that phi 1 and phi 2 being generated at a place and being used, they are going to be circulated to various parts of the chip.

And you want to make sure that, where they are needed also they remain non over lapping, it does not make sense for the you to generate phi 1 and phi 2 at 1 point on the chip, transport them you know 2 millimetres away. And then you find that because of skews the non overlap has gone completely, you understand, so to have some immunity to skews, you must make sure that non overlap time is reasonable you understand.

So, this is what is called the non overlapping clock generator, and how do you generate phi 1 bar and phi 2 bar from this, just use inverters, and the understanding is that these are the guys which are giving you the non overlap VDD.