VLSI Data Conversion Circuits
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Lecture - 7
Gate Boosted Switches - 1

In the last class, we saw that if the switch is non-linear and the resistance of the switch varies as a function of the input voltage in the following fashion, so R switch we saw can we modeled roughly as R on, plus something which depends on the input plus, r 2 into v in square. In that case we could approximate the drop across the resistor by approximating the voltage across the capacitor to be the input voltage, because we know that eventually when we have a working design, the drop across the switch will be very small.

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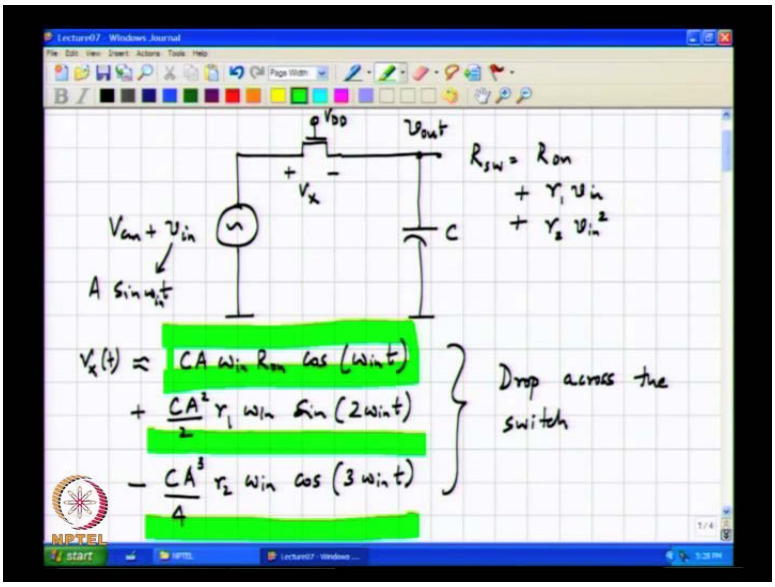

In which case the input voltage is approximately the voltage across the capacitor, which means that the current through the capacitor can be approximated as c d v in by d t rather than d v out by d t. And that in turn means that the voltage drop across the switch can be written as R switch multiplied by capacitor current, and in the last class we derived these expressions for a sinusoidal input.

Couple of observations to make the drops corresponding to the fundamental the second harmonic and the third harmonic, are all proportional to c times omega in, and why does

that make sense. And that makes sense because the drop is current times resistance the current increases with frequency as well as increased value of the sampling capacitor, the dependence and amplitude we discussed.

And it made sense that the second order term that is the second harmonic is proportional to A square, and the third harmonic is proportional to A cube. And if we choose a sufficiently large tracking bandwidth, we see we should choose that this drop all these 3 drops must be much smaller than the input voltage, but one thing you must observe is that this is at the input frequency itself. So, this corresponds to a linear effect, the nonlinearity is coming because of r 1 and r 2 because there is where the dependence of the resistance on the input voltage lies.

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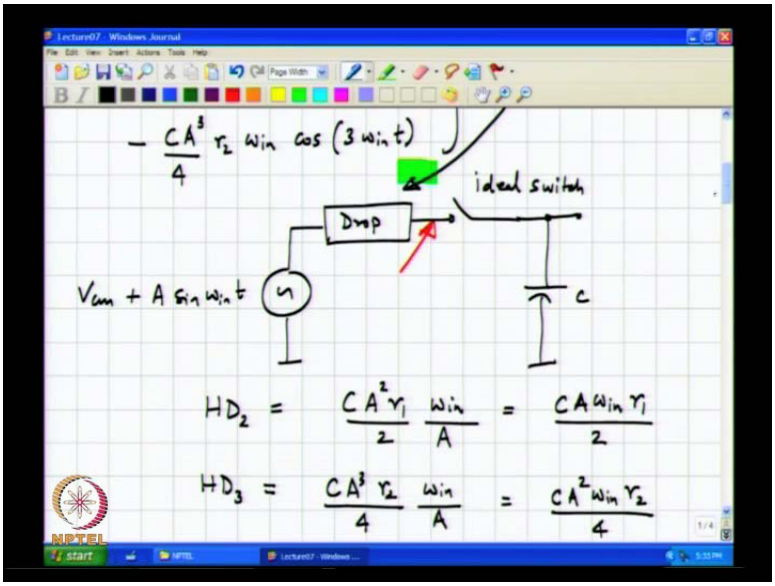

So, the second harmonic distortion, therefore as far as the track and hold is concerned you can modulate this way, so you have the input which is a pure sinusoid riding around a common mode.

Student: ((Refer Time: 03:23)) the input is a ((Refer Time: 03:27))

Phase shift, so the input is v c m plus A sin omega n times t, you can model this drop in the following way, you have, you can think of it as a component, which is added to the input, and you otherwise have an ideal switch, which is connected to the capacitor. You can think of a real switch with a drop across it, as an ideal switch with a voltage source

in series with the corresponding drop, now, therefore it appears as if an ideal sample and hold is being excited with an input which is.

Student: Input plus or minus.

Input plus or minus drop, in other words the true input that this sample and hold this ideal sample and hold is sampling, is not the one that you really want to be sampled to it are added some terms containing the non-linear components, which occurs 2 omega in and 3 omega, in does it make sense. So, what do you think is the ratio of the second harmonic tone to the fundamental at this point, the ratio of the second harmonic to the fundamental is a measure of distortion or how much nonlinearity there is in the sample and hold.

And is given by the ratio I mean the, so this is called second harmonic distortion or HD 2, and is given by the ratio of the amplitude of the second harmonic, which is C A square r 1 by 2 times omega in to the amplitude of the fundamental which is A, and we see that this is c a omega in times r 1 by 2. In the same way one can define the third harmonic distortion, as the amplitude of the third harmonic component which is c a cube r 2 by 4 times omega in divided by A, and this happens to be C A square omega in r 2 by 4. And clearly we see that as the input amplitude increases HD 2 and HD 3.

Student: Increase.

Increase and this is it make sense, if you have take a non-linear system and increase the input amplitude one can expect, the amplitude of the harmonics to increase with the input signal level. And more importantly the third harmonic level goes up as A cube, the ratio of the third harmonic level to the fundamental goes as A square, and similarly HD 2 which is the ratio of the second harmonic to the fundamental goes as A. So, and it also is clear that r 1 and r 2 influence the second and third harmonic levels, please note that this is only valid if the switch can be modeled in this way.

Student: ((Refer Time: 08:53)) function ((Refer Time: 08:55)) linear ((Refer Time: 08:57)). Actually we take only linear, because it is easy to calculate (( )) second harmonic Means the.

The question is why are we interested in the second harmonic and the third harmonic, well we are not interested in them we want to make sure that, they are not there, because these terms correspond to distortion. You ideally want only the input, but due to the non-linear operations of the switch the equivalent effect is that you are sampling with an ideal sample and hold an input which has been already corrupted by some nonlinearity you understand.

So, if you for example, use this non-linear sample and hold, and look at the discrete time sequence, you will see their tones corresponding to the input frequency twice the frequency and thrice the frequency. If you did not know that the sample and hold was non-linear, what would be your obvious conclusion.

Student: ((Refer Time: 10:04)).

You would think that the input consists of 3 frequency components one at omega in, one at 2 omega in and one at 3 omega in clearly you made a mistake.

Student: There is no practical ((Refer Time: 10:17)) it happens third.

I mean there will be other harmonics also hopefully those harmonics are much smaller than the second and the third, in practical systems you would find that mostly the second and third harmonics are dominant with higher order nonlinearity is contributing, you know much smaller signal strengths than. And as I said this is only true, when the switch can be modeled using this expression, which will only be valid over a limited range of input voltages.

For example, if the input amplitude is so large, so as to cut off this transistor, then no polynomial can model this exactly you understand so, but the utility of this kind of model is for us to be able to appreciate what the problem is and what 1 can do to solve the problem. Here, we see that as we expected perhaps that r 1 and r 2 must influence the non-linear components that one samples, and r 1 is responsible for the second harmonic well r 2 is responsible for the third harmonic distortion.

Another point is that even though the input is band limited, let us say you are sampling a signal at f s, and the input tone is less than f s by 2, because we have put in anti-alias filter before sampling and so on, and taken care of the fact that there is no aliasing. Now,

comment on what will happen to the second harmonic, if the input lies between 0 and f s by 2, where does the second harmonic lie. It can potentially lie from 0 to f s, and please note that this sample and hold circuit is occurring is happening after the anti-alias filter, so the second harmonic is; obviously, not filtered out by the anti-aliasing filter at all.

So, even though the input to the sample and hold is band limited, the second harmonic can appear at in the range 0 to f s, so when you sample this, what happens the second harmonic can alias and appear like a.

Student: Low frequency tone.

Low frequency tone, a classic example for is the following.

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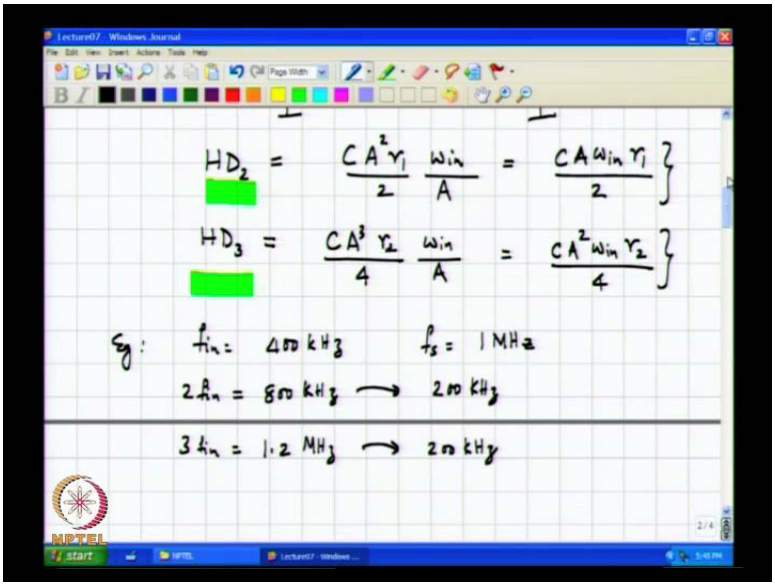

So, let us say f in is 400 kilohertz, f s is 1 megahertz clearly I have not violated Nyquist, 2 f in is what 800 kilohertz, and if we just recall if the switch is non-linear, it is like adding a component at 800 kilohertz, and at 1.2 megahertz, before the ideal sample and hold. So, if I add, if I sample at 200 of 800 kilohertz at 1 megahertz, how will this look like, in the discrete time spectrum it will look as if it came from a continuous time signal which was at.

Student: 200.

800 kilohertz, when sampled at 1 megahertz, will result in a discrete time sinusoid, how will that appear as far as I mean if you try to figure out, what input tone gave you that discrete time sinusoid, what would you infer.

Student: 200 kilohertz.

It will appear as if.

Student: 200.

This will this has come from a 200 kilohertz tone, is this clear similarly 3 f in will look like.

Student: 203.

3 f in is 1.2 kilohertz, say 1.2 megahertz and this will also appear like.

Student: 200.

200 kilohertz, do you follow, so if you take a continuous time signal which has been passed through a non-linear system, harmonics will appear, and if you look at the continuous time spectrum the harmonics will all be higher than the fundamental. However, if you take a signal, a continuous time sinusoid and pass it through a non-linear sampled and held system, the harmonics can lie at frequencies.

Student: Less than the input.

Less than the input frequency, because of aliasing, does it make sense, so let us say we had a switch we put in some signal amplitude, we found these distortion that there is some distortion. So, how will you choose how much distortion you can tolerate, clearly either sample and hold is good enough for your application or it is not good enough, how will you determine whether your sample and hold as far as nonlinearity is concerned is good enough.

Student: HD 2 ((Refer Time: 16:25)).

HD 2 and HD 3 must be even if it is too high you know you cannot accept it, so what is too high how will you define that.

Student: Signal to noise ratio.

one common way of doing it is to say.

Student: quantizer.

The ratio of I mean you are anyway going to pass this through a quantizer, so you got to make sure that some measure of h term in HD 2 is telling you how much second harmonic amplitude, you are adding in relation to the fundamental. One way of making thresholding what HD 2 or HD 3 are acceptable, is to say the error due to distortion must be less than some fraction of the quantization step, I mean that is the reasonable way of going about it.

As, we go forward we will see that there are spectral measures for this, we can talk in terms of signal to distortion ratio or signal to noise plus distortion ratio both noise and distortion are undesired. The noise thermal noise is coming, because of sampling and that mean square value is k t by c, on top of this because of non-linear operation of the switch there is distortion.

And we said that signal to noise ratio must be some threshold, if it is too low in other words if the thermal noise is too high, then it does not make sense to go and build a spend a lot of effort building a great quantizer, because you have already ruined the signal, because of thermal noise. So, in a similar fashion you can say if I want an end to end resolution of so much then I will allocate this much to thermal noise, and so much to distortion components and after this there is anyway quantization, which also adds some amount of error.

So, we are not getting into details, one thing one can say is that ball park amount of error that one adds, because of distortion will be somewhere in the range of how much you can tolerate with respect to noise. There is one error which is noise, there is one error which is distortion, and there is 1 error which is.

Student: Quantization.

Quantization, if end to end you want so much error, we said that the error due to thermal noise must be much smaller than the quantization step, in a similar fashion we can say the error due to distortion must also be much smaller than the quantization step. And you

know how much smaller is up for debate, but there must be much smaller, and HD 2 and HD 3 are numbers which characterize, the ratio of the errors due to second and third harmonics respectively.

So, if the resolution of the converter of the a to d converter is large it must follow that you will also be, naturally shooting for HD 2 and HD 3 which are what, which is small, does it make sense. Now, let us say you had a switch and you put in some input sinusoidal amplitude, and you have found that HD 2 and HD 3 were too high and, so in other words input amplitude is fixed, input frequency is fixed.

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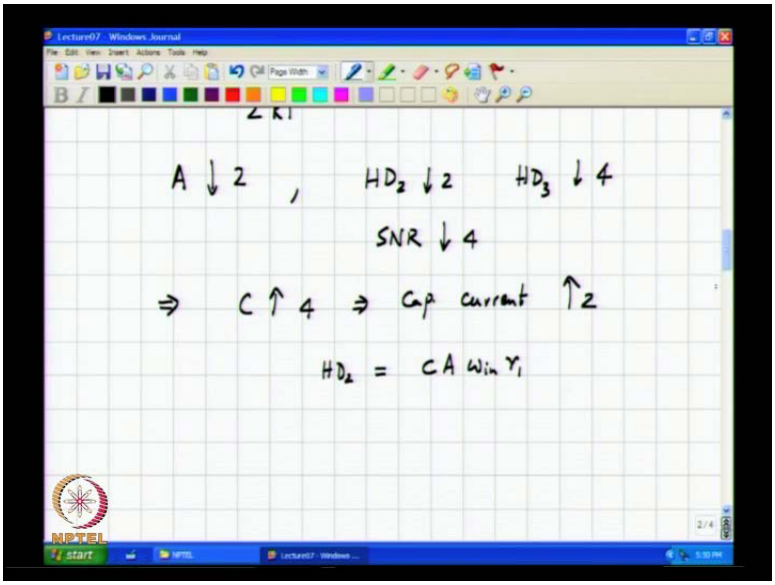

Let us also assume that the capacitance has been chosen to satisfy.

Student: noise ((Refer Time: 20:39)).

Thermal noise. So, in other words the capacitance has been chosen to be large enough, that the signal to thermal noise ratio is adequate, in other words a square by 2 c times k t is the signal to thermal noise ratio. And c has been chosen, so that it just meets the desired signal to thermal noise ratio; however, when a real switch was put the switch happens to be non-linear, so apart from thermal noise you also get.

Student: distortion.

You get distortion. So, let us say the HD 2 and the HD 3 were too high, so what do you think we can do.

Student: MOSFET transistor.

What is the simplest thing you can do to reduce HD 2 and HD 3.

Student: Reduce the input signals present.

I mean the most straight forward thing that you can think of is to say a, if I put too large an amplitude we know the distortion goes HD 2 goes a and HD 3 goes a square, because the no linear components are proportional to A square and A cube. So, if you find that the system is way to non-linear for comfort, the most obvious thing to do is to simply reduce the signal amplitude, so if I reduce the input amplitude by a factor of 2, what do you think will happen to HD 2.

Student: ((Refer Time: 22:34)).

HD 2.

Student: ((Refer Time: 22:37)) amplitude.

The second harmonic amplitude will go down by a factor of 4, but HD 2 will go down by a factor of.

Student: 2.

2, what about HD 3.

Student: ((Refer Time: 22:49)).

Goes down by a factor of 4, so it seems like a simple and straight forward way of fixing the problem; however, if we now reduce amplitude what has happened.

Student: ((Refer Time: 23:09)).

The signal to thermal noise ratio has now, increased or decreased.

Student: Decreased.

Decreased how much was the signal to noise ratio gone down by.

Student: 4.

By a factor of 4, but this is not acceptable we want a minimum signal to noise ratio, so what do you think you will do.

Student: Increase the capacitance.

So, you will increase.

Student: Capacitance.

This means that the sampling capacitance must go up by how much now.

Student: 4.

A factor of 4. So, if you try and increase the capacitance by a factor of 4, what has happened to the displacement current in the capacitor.

Student: ((Refer Time: 23:53)).

The input amplitude has gone down by a factor of 2, but capacitance has gone up by a factor of 4.

Student: So, the expression cannot ((Refer Time: 24:03)).

The current has increased or decreased.

Student: Decreased.

By what factor.

Student: 4 times.

Student: c into d.

Amplitude has gone down by a factor of 2, capacitance has gone up by a factor of 4, so the displacement current or the capacitor current has gone up by a factor of.

Student: 2 .

2, which means that, the distortion components across the switch if the switch remains the same what would happen to the I mean we saw that HD 2, for example is c a omega in r 1 by 2.

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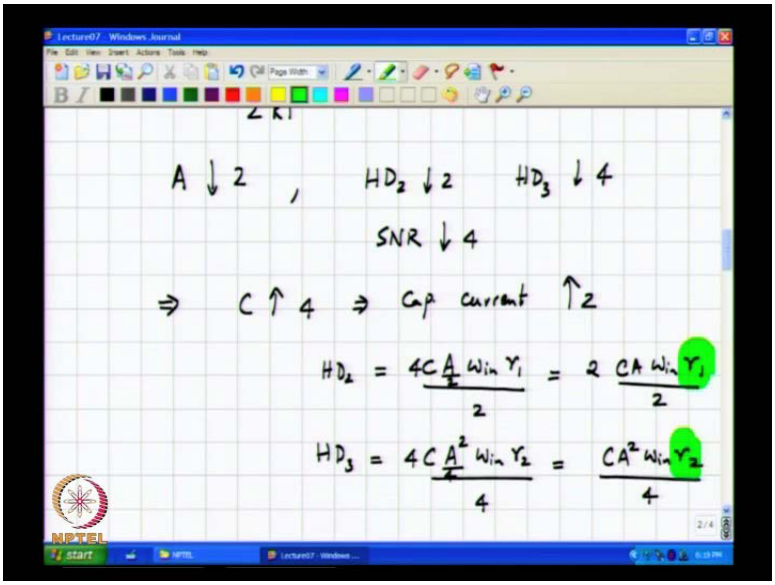

So, in an attempt to reduce HD 2, we said I am going to make a equal to A by 2, but to maintain SNR I have to increase C 2 4 C, so what has happened to HD 2.

Student: ((Refer Time: 25:29)).

Which is it is 2 C A times omega in times r 1 divided by 2, does it make sense, and similarly HD 3 is what C A square omega in r 2 by 4, and what have we done we have increased C by A factor of 4, and reduced a by A factor of 2, so A square by a factor of 4 So, HD 3 actually becomes remains what it was by 4 you understand, now what was the whole idea in trying to reduce the input amplitude.

Student: It is harmonically.

We are hoping that if the input amplitude reduces, then non-linear effects will reduce which means distortion will reduce, and what do we find now find that there is lot of the noise and distortion has increased. So, we see that the instinctive thing to do when whenever distortion is a problem is to try and reduce input amplitude, because distortion depends on nonlinearity, non-linear components are proportional to signal amplitude to the power end.

So, it seems like an obvious thing to try and conquer distortion by reducing the input signal amplitude; however, reducing input signal amplitude has a cost in terms of signal to thermal noise ratio. So, in this fictitious example, if we reduce the signal amplitude by a factor of 2, the signal to thermal noise ratio falls down by a factor of 4, in order to get back the signal to noise ratio.

Student: ((Refer Time: 28:04)).

You need to increase the sampling capacitance by a factor of 4, which in turn increases the displacement current, which in turn increases the voltage drop across the sampling switch, which in turn increases the.

Student: Distortion.

Distortion for specifically, we see that after we do all this by reducing the input amplitude the second harmonic distortion has actually increased, because the sampling capacitance is increased by a factor of 4, and there is no change at all in the third harmonic you understand. So, the reason for going into this argument is that is to demonstrate that, the quick fix way of making things work, which seems to be to reduce amplitude given distortion as a problem does not really work. So, the only choice you know I mean that 1 has in order to reduce distortion is, therefore to reduce.

Student: R 1.

R 1 and.

Student: R 2 .

R 2, in other words

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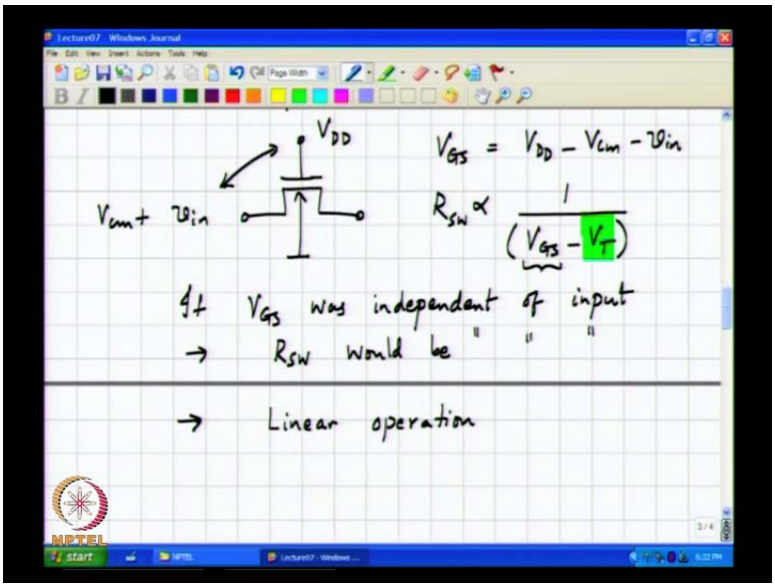

We need to make the resistance of the switch as independent of the input signal as possible is that clear, so that is the motivation for going into the next topic, which is we need to reduce r 1 and r 2. In other words this is equivalent to saying that, the resistance of the switch must be made independent of the input signal, so for the simple MOSFET switch, let us recall why the resistance was dependent on the input signal in the first place.

So, during the track phase the gate is connected to VDD, and the source is v c m plus v in, resulting in a gate source voltage which is VDD minus v c m minus v in, and the resistance of the switch is proportional to 1 by v g s minus v t. For the time being let us neglect the variation of threshold with respect to the input, we call that the threshold voltage is also dependent on the input through the body effect.

And for the time being I will just neglect this threshold let us assume that this quantity is constant, and we see that as the input voltage varies v g s varies, which therefore measure the switch of the resistance of the switch is varying with input. So, the solution that suggest itself is the problem is that v g s is varying with input, so what is the solution.

Student: It is constant with v g s ((Refer Time: 31:47)).

The obvious thing to say is that if v g s was independent of input, R switch would be independent of the input, which means this will result in a largely linear operation, again I wish to bring to your attention that we have in this discussion neglected the variation of the threshold with the input voltage, does it make sense. So, what do you think, how do you think we can make the v g s constant with input.

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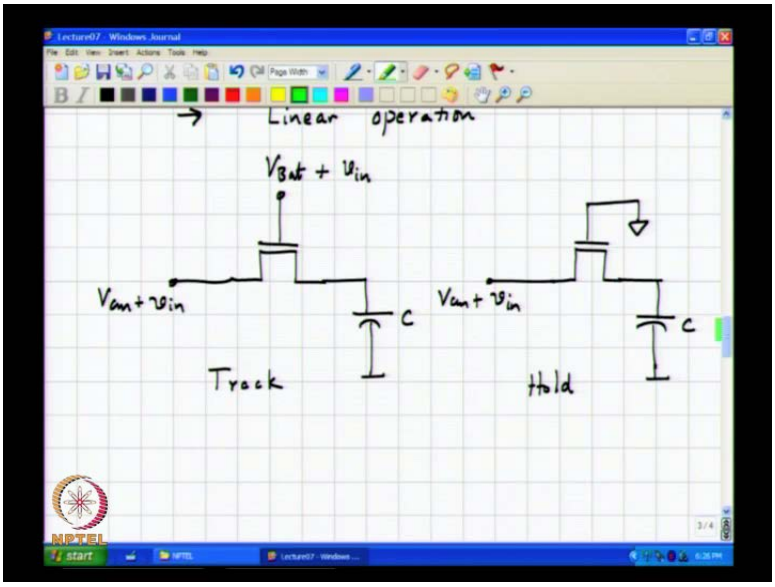

So, this is the transistor I am not going to denote the body, I am assuming that is going to be grounded, the input voltage is v c m plus v in normally the gate would have to be would be connected to VDD, but that results in v s being dependent on the input. So, what do you think we should apply to the gate in order to keep v g s a constant.

Student: VDD plus

Student: something minus VDD.

Some constant I mean, earlier this used to be VDD, one way of keeping the gate source voltage constant is to add a component, to the gate voltage which is also has.

Student: V in.

V in. So, let me in general some voltage v bat plus v in, so during the track phase this must be the equivalent circuit, and during the hold phase what happens what should I do to the gate, I need to turn the MOS transistor off, so one choice of doing that is to

connect it to ground. So, how do you suggest that, I generate this voltage in principle what do you think, you would need.

Student: Somewhere to some of the.

We need some of voltages.

Student: ((Refer Time: 35:43)).

So, in principle what we need to do is to have some way of adding 2 voltages, one being the input, and the other being

Student: Some constant

Some constant value v bat, so conceptually 1 can say that if we had a battery with us.

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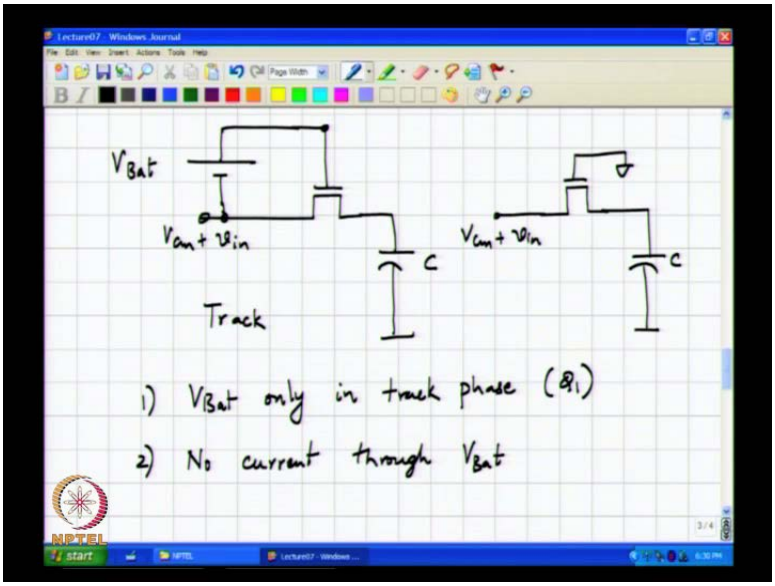

And let me I beg your pardon, let me just call this v bat plus v c m plus v in, just, so that what will be v g s the constant value of v g s which we now get is simply v bat, it is just a notational thing it is got nothing no fundamental value. So, if the gate voltage during the track phase only was made v bat plus v c m plus v i, then the gate source voltage is v bat independent of v i or v in, which in principle means that r 1 and r 2 are 0. So, during the track phase what we must do is if we had a battery v bat, v bat is not good enough we must generate v bat.

Student: Plus.

Plus v c m plus v in, so what was the easiest way if we had v battery and the input terminal is v c m plus v in, how will you generate v bat plus v c m plus v in, the most straight forward thing is to connect the battery like this, and do this. So, this is during the track phase, and during the hold phase it is this, so how do you suggest, what do you think we should about the battery, what are the things that about the battery that we can exploit, is this I mean should I go and go to the store and buy a battery.

Student: ((Refer Time: 38:56))

That is fine.

Student: The distance by a capacitor charged to the voltage v bat.

And why is that.

Student: It is that the charge drawn by the voltage source is, it is like an infinite capacitor charged to a voltage v bat.

So, couple of things we need to know about the battery, 1 we observe that the battery is needed only in.

Student: ((Refer Time: 39:32)).

In 1 phase, if you divide up the whole clock into 2 phases the track phase and the hold phase, 1 the battery is only needed the track phase which I will call phi 1, and 2 what is the current flowing out of the battery.

Student: 0.

So, no current in other words there is no constant current being drawn from the battery you understand, and we have already seen in earlier classes that, if you want to realize a battery with a having a given voltage, one way to do it, is to take a capacitor and charge it up to v bat you understand. In other words a capacitor charge to a voltage is indistinguishable from a battery of that voltage as long as you do not draw any.

Student: Current.

Current from that capacitor, you know this principle already, so in other words what this leads us to is during phi 1.

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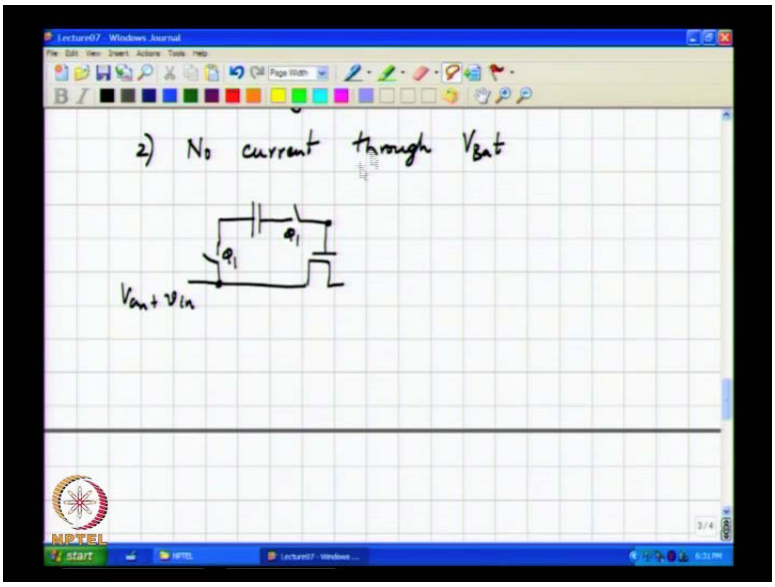

So, this is the sampling switch during phi 1, I take a capacitor and connect it between the input and the gate of the sampling switch.

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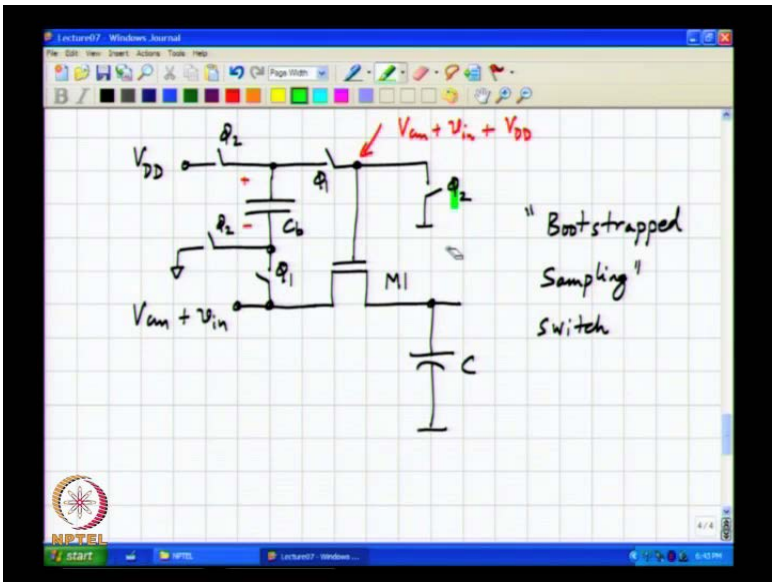

So, let me just make this bigger, the assumption is that this capacitor C b has been charged to v b earlier, during phase 2 which is the hold phase, what should I do, to the gate of the sampling switch, so during phi 2 and if connected to ground. And during phi

2 the battery is not needed after all, so what can you do during this time, this capacitor is not needed during phase 2, so what can you do in principle.

Student: Charge.

You can charge use phi 2 to charge this capacitor to V b or v bat, and can you suggest one convenient value of v bat.

Student: VDD

VDD, why not VDD by 2.

Student: ((Refer Time: 44:02)).

I mean please note that after we do this the gate source voltage is v bat, and you want to have the lowest possible switch resistance for a given transistor size, so it makes sense to choose v bat to be equal to VDD. So, in other words this is VDD, so couple of questions arise here, one is do we need to keep refreshing C b every cycle, or can we just charge c v once to VDD, and leave it like that and keep going for ever, what is your opinion.

Student: ((Refer Time: 44:52)).

Why do we need to refresh.

Student: leakage current will be more.

Leakage current from where.

Student: Switches.

The switches will all have leakage current that is one thing, another one is there anything else.

Student: of the switch the ((Refer Time: 45:13)).

Well one another thing is the gate leakage of this transistor, for those of you who are not aware of gate leakage it turns out that the in modern C MOS technologies, where the channel lengths are very, very small, and oxide thickness is very low. It turns out that the thickness of the gate, I mean the stumbling current through the gate, and there is a very

small gate current also in the MOSFET, if there was no gate current do we need to worry about it or.

Student: ((Refer Time: 45:50)) discharge through ((Refer Time: 45:52)).

No, what I did not understand.

Student: C b can get discharged through v the source itself.

No, because during phi 1, I mean let us say you charge C b my question was if you charge c b once to v bat, and never bother to refresh it every cycle would it still work.

Student: MOS C b.

Let me name the MOSFET, let me call this as m 1, yes.

Student: when the v in is changing, the c b can have a that mosfet also has a capacitance, so through that something like depending on frequency.

While that is correct, because please note that during phi 2 what was the charge on this plate, I mean during phi 2 this node is connected to ground, during phi 1 this node voltage is supposed to be v c m plus v in plus v bat. So, there will be since the potential of that node has changed it follows that the charge on that node must also change, only then only if you inject charge will potential change, so that charge must be coming from where.

Student: ((Refer Time: 47:25)).

It must be coming from the top plate of that battery C b you understand, so it is not just sufficient to charge C b up once and let it go, that might be if c b was truly infinite; however, C b is a I mean for practical system C b must be finite. And every I mean all lost charges must be replenished, otherwise eventually it will tend to it will get completely discharged, and will not get any voltage across C b, which is why it was there in the first place, is this clear.

And this is I mean refreshing it in phi 2, which occurs every cycle is not a problem at all, because c b was sitting idle anyway and you might as well use that time to charge C b

back to VDD is this clear. So, under these circumstances during phi 2, this potential will be v c m, so why is this suppose to be a fraction of VDD.

Student: Initially, C b was with VDD.

C b.

Student: Or phi 2, and then your when it comes to phi 1, so the charges will be coming to that.

So, you are indeed, so if the charge with the parasitic capacitance at this node is very high, then some amount of charge from the top plate of C b will have to, go and supply that charge, so the voltage across c v will.

Student: Reduce.

Reduce a little bit; however, it turns out that you know usually the MOS transistor is much smaller than C b, so the amount of parasitic charge here at the small, and you have to choose as he pointed out, if we choose c b to be too small, then you will end of this problem. So, as you will see in your assignment the size of C b does indeed matter, but is usually not a problem, you understand now that is a design consideration for C b.

So, in phi 1 in principle at least, this potential which is the gate of the main sampling switch goes to v c m plus v in plus VDD resulting in a gate source voltage, which is VDD, which means that the switch resistance in principle. If you neglect the threshold voltages variation with v in remains constant at 1 by mu and c ox W by L times VDD minus v t, is this clear.

So, this principle is called boot strapped sampling applied to a switch, so what do you think is the next step, what all do we need to do, I mean are we done or we need to do something else.

Student: Switch ((Refer Time: 51:11)).

I mean we were trying to realize 1 switch, now all of a sudden on the board you see that we have we have figured out this, but now there are 1, 2, 3, 4, 5 switches, so how do you think we are going to realize these switches. They are also going to be we have to use

mass transistors to analyze these switches, hopefully these switches are not any more complicated than the first 1.

If each of these switches becomes very complicated then you are ending up with a non-converging series, it turns out that most of these switches are easy to do with standard arrangements of N MOS and P MOS transistors, we will discuss that in the next class.