VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture No - 56
Current Steering DACs-2

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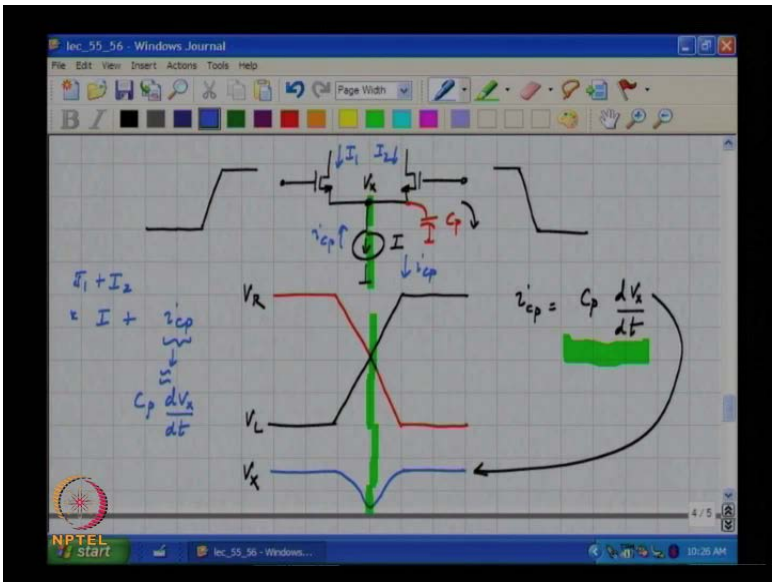

This is VLSI data conversion circuits. Lecture 56, In the last class, we were looking at a current staring pair, and what happens to this tail current waveform when the drive waveforms changed it. And we saw that as the drive waveforms make a transition. The node V x assuming everything was done sufficiently slowly would do something like this right. Now in practice of course, there will be a whole lot of parasitic capacitance at the source coupled node. So, to first estimate what do you think is the current flowing through C p. Pardon. To first approximation the current flowing through C p is nothing, but i c p which is nothing, but C p times d V x by d t, and why do I say it is a first approximation.

Will check, so please note that why I call this an approximation is because the V x that we have drawn here was drawn based on the fact that there is no capacitance and that or the current through the capacitance is negligible right. So, this is purely from a DC picture, and once we draw this we say that they actually the current flowing through the capacitor is C p times d V x by d t all right, but the V x that we are using is not the true V

x that will be there at the source couple node. So, in reality the total current that is flowing are the sum of the two source currents of the transistors must be equal to.

This is I 1, and say this is I 2. I 1 plus I 2 must be equal to I plus C p times d V x by or plus I C p which is approximately equal to C p times d V x by. This is clear. Now, during this period the first half what is the direction of the current through I C p or rather the current through C p. Pardon. Is it unit direction of capital I or opposite to the direction of capital I. So, this is during this time, this I C p is in this direction and in the other half the time is in this direction correct. So, what can you say about I 1 as a function of time. Ideally it must be when V L is low, what must be I 1.

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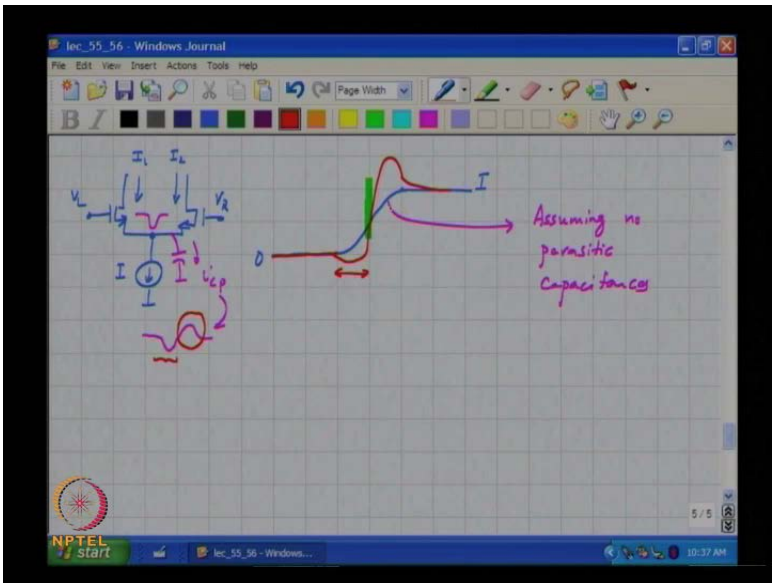

Let me redraw the diagram here for you, when V L is low I 1 will be 0. When V L is high the current will be it will eventually reach I. And if things were going very slowly the current will do what the DC equations predict, which is this let assuming no parasitic capacitances. Does it make sense? Now as we discussed earlier right the fact that the rise time and fall time. You know when these for example, these transitions as we saw can cause non-linearities in the DAC.

So, I mean the basic idea would be to try and make sure that these transitions happen as quickly as possible, which basically means that the voltage at V x will take a rapid dip and get back to I. If you want to reduce the size of the transition and make it as thin as possible; that means that the voltage at V x will also become a thinner sleever, which

means that the slope of the voltage across those across the parasitic capacitance will increase causing the reactive current to increase.

Now during the second half what happens to this, this current the reactive part of the capacitor current is it flowing in the same direction as I or is the parasitic this voltage is doing this. So, after the dip and when it is coming back the current through the parasitic capacitances do you think it is in the same direction as I or is in the opposite direction, same direction. And during the second half where is most of the current flowing, which transistor is it flowing. I C p will be some current which does this correct this is this is I C p this is the waveform correct. So, what do you think the current in the I 1 will be as a function of time when you kind of consider the parasitic. Pardon.

In the second half at least what do you think the current should be like. It will be more than what is predicted by the DC equations. So, does this and then you will see that this must be added to the I S O what you will see is that, the current will kind of peak like this because during the first half the current is in the opposite direction. And they also be some overlap capacitances between the clock waveform and the output node and so on.

So, for the first part of the transition period you will find that the current actually is negative this is only a reactive component, and then this transistor start should turn on. And as it turns on assuming the waveform is like this. The current in the second half will be higher than the DC tail current because of the reactive component of the current in the tail capacitor, which will cause an increase in the current and of course, this waveform settles to its steady state value at which point the current will come back to I I.

So, as you can see there is a within quotes glitch in the output current waveform, and this glitch is there whenever there is a transition all right. So, do you think this glitch is a linear phenomenon or a non-linear phenomenon. Now, you just told me it depends only on the transition if it is a linear phenomenon it must depend on the so let me. So, if you look at just the waveform of I 1. Let us say the waveform was doing this right and then we did not if there was a transition of 1 to 0 it would do this. So, this is 0 1 0 now because of this strain stuff happening at the source coupled node whenever there is a transition you will have the glitch correct. So, it does not depend it does not seem to depend on. I mean. So, this stuff happens whether or not it is a raising edge or a falling edge.

So, this glitch is basically a non-linear phenomenon. So, because strange things happen only when whenever there is a transition it does not depend on the sign of the transition, which is why this effect is non-linear one and therefore, the key point I mean of course, you go and sit and analyze this very carefully, but as designers were interested in avoiding the problem rather than try and understanding in detail what happens to how it manifests as nonlinearity and so on. So, the basic idea must be to try and keep the problem is the glitch. So, to avoid the problem you avoid the glitch as much as possible and the glitch is coming because of the reactive currents through the capacitances, parasitic capacitances right, at the switching node.

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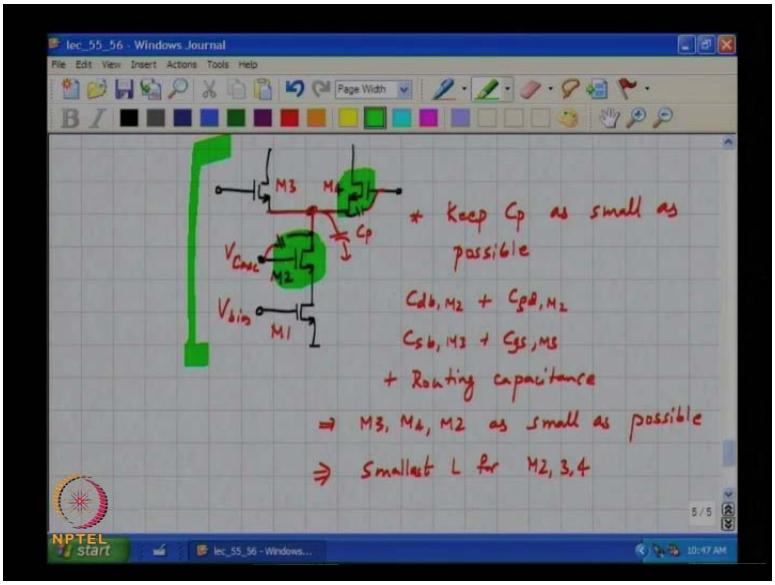

So, you cut a long story short what you want to do is to keep the total parasitic capacitance at node as small as possible, and how do you think you can keep this net parasitic as small as possible?

Student: ((Refer Time: 18:10)).

Pardon. Decrease. So, this parasitic capacitance C p is coming because of what are all transistors. It is coming because of these transistors and the cascade correct. So, here the are the source drain parasitic sorry. The drain bulk parasitic of let us say this M 1, M 2, M 3 and M 4. C d b of M 2 plus C g d of M 2 correct, please note that this is the bias node V cascade, V bias correct. Then there is one of the transistors either M 3 or M 4 is off correct, which means that the C g s of that transistor is I mean you have a C source to

bulk of M 3 or M 4 plus some C g s of M 3 or M 4 plus whatever routing capacitance there is in this wire. Does it make sense right? Now what happens to you have to reduce the glitch you are going to keep total C p as small as possible. So, what do you think you can do?

Keep M 3, M 4 and M 2 as small as possible, which means that what can you say about their lengths. If you want them to support the same current, but you want them to be as small as possible and have the same I mean have a small a headroom as possible because you want to maximize the headroom for the, which of these transistors do you think should have largest overdrive voltage. Of all the transistors here M 1 through 4 which transistor would you allocate the highest over drive?

Student: ((Refer Time: 21:45))

Which of these transistors would have the largest overdrive?

Student: ((Refer Time: 22:06))

And why?

Student: ((Refer Time: 22:14))

Which one will would have the largest gate overdrive voltage?

Student: ((Refer Time: 22:29))

Why?

Student: ((Refer Time: 22:38)).

Then which one M 2, why the W value low?

Student: ((Refer Time: 22:38)).

Now therefore, there are transistors here M 1 through M 4 right. So, which of these transistors will you allocate the largest gate overdrive 2 and why?

Student: ((Refer Time: 23:26)).

We discussed this in the last class.

Student: ((Refer Time: 23:31)).

For you want to keep whatever headroom you have to stack up these three transistors the largest amount must be allocated to M 1 because that directly influences the matching. Is that clear or it is not clear. Yes. Now after that you these transistors mut carry a current must be sized so as to be able to carry the current tail current I right, but you want them to be as small as possible, so as to minimize the capacitance at the source coupled node C p. Now that can be accomplish by choosing right. The for that given let us say you decide to split up this available headroom after you remove the one allocated to M 1. The rest of it you split among two transistors.

Now, if you want to make both the transistors as small as possible. For that headroom you will choose you know whatever W by L is required correct to support that current. Now once W by L is required is chosen you have to choose the W and the L is not it. So, the question is, what I will you choose? Pardon. So, you will choose the smallest length possible in the tech. Well let us come to that now if these transistors are made very small right it means that their threshold voltages can also change by a large amount, but do you think mismatch in M 2 is an issue.

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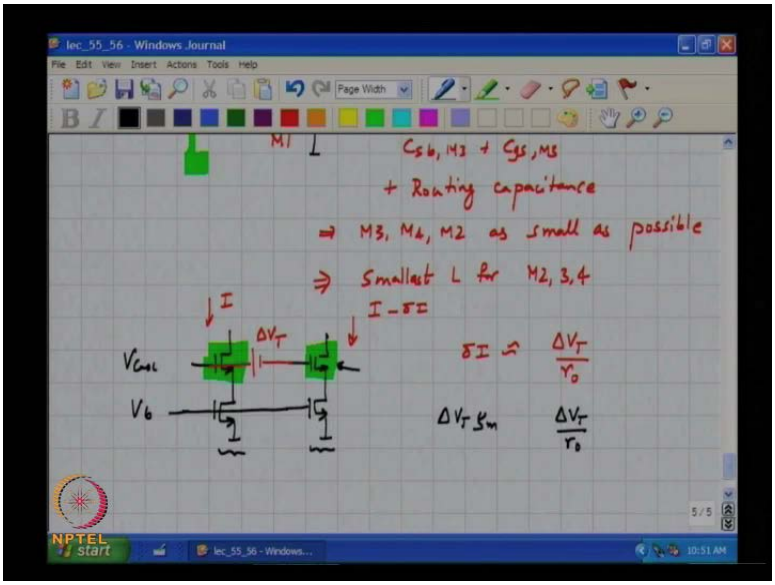

Let us say you had two cascode current sources. So, clearly the mismatch here is the problem as we saw before and we figure out you know how you can calculate the sizes to get a certain certain delta I by I now the question I am asking you is what happens to the

mismatch in these transistors if their thresholds are different let us assume that the lowered transistors are matched, but these thresholds are different from each other what do you think will be the mismatch in the current. So, let us say this threshold is off from this by delta v t what will be this current is I this will be I smaller or larger.

Student: Smaller.

Smaller and what will be delta i.

Student: delta v t is r naught.

Pardon.

Student: Delta v t by r naught.

It will approximately be delta v t by.

Student: R naught.

R naught which transistor.

Student: Lower.

The lower transistor right why because this behaves like a source follower. So, the source voltage would be lower by approximately delta v t. So, the delta will be delta v t by r naught. So, the question now is is mismatch in the in the cascode devices important. Pardon.

Student: lesser than the…

Yeah. So, the if the same mismatch was there in the lower transistors the the mismatch in the currents would have been delta v t times g m of the lower devices now it is only delta v t by r o and since g m r o is a much much is a very, very large number hopefully much much larger than 1 which would particularly be true because for matching you would have chosen a large length I mean right for the same w times I mean for the same w by l you want to you want to have a large w times l and that was accomplished by taking w and l and multiplying both by some.

Student: Some factor.

Some factor to achieve the given a v I mean sigma v t correct which means that the g m r o of the lower devices will be large, which means in turn that the effect of mismatch in the cascode devices is small. So, we do not really have to worry about the fact that we're using a device with a very small.

Student: W.

W times l right the motivation for choosing a small transistor on the top would be to make sure that the capacitance at the top at the source couple node would be as small as possible the same thing also holds for the current switch transistors, you were also choose them to be small or as small as possible the mismatch if mismatch in the cascode devices is not an issue mismatch in.

Student: Current source.

The current source transistor I mean the current switch transistors should be also not an issue as far as d C current is concerned, simply because it will get divided down by some g m r over the.

Student: Whole square.

Whole square all right, and to reduce the glitch or the distortion dynamic distortion in the DAC you want to make sure that the interconnect between the transistors the switch transistors and cascode devices is you know as short as possible does it make sense. Now let us see what happens I mean the last time around we assumed that the 2 currents at the 2 drive waveforms crossed each other exactly in the in the middle

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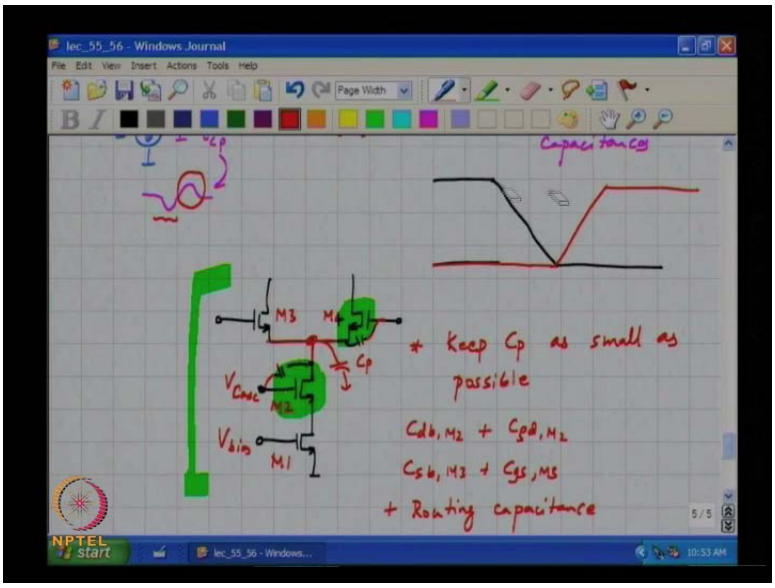

Let us say by some of it the drive waveforms did 1 of the drive waveforms was q. So, that it did this.

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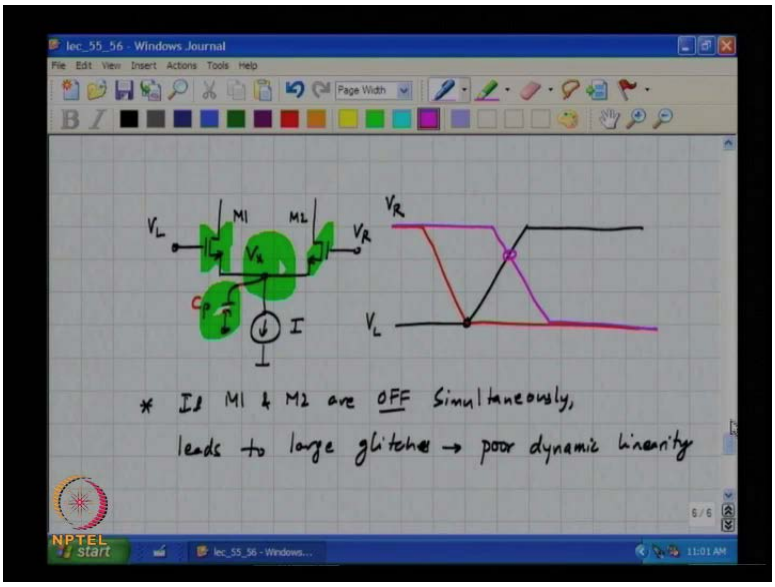

Let me… So, we will say let us say this is v l and this is v r what you think will happen to v x now.

Student: The intersection point is v x would be 0.

At the intersection point what is happening.

Student: V x.

Why?

Student: Sir finding both the…

No.

Student: current refers to the input.

So, at the intersection point what happens now.

Student: V L V L V L.

I mean if v l . So, if the waveforms are like this. So, that momentarily both the transistors v l the 1 corresponding to the left and the right if both of them are off at the same time what happens this current source has no option, but to simply discharge whatever charge there is on.

Student: C p.

C p I mean please note that this is all happening for a very very short interval of time. So, there is no danger of C p going hopefully all the way to ground you understand if this voltage goes to low the current sources are will get get crushed and get out of the triode region right assuming that such eventualities do not arise what will happen is that this capacitance C p will now lose an awful lot of charge. So, when 1 of these transistors get back into action what will happen this voltage v x is at a level which is much lower than what it would conventionally have been right which means that the initially glitch in the current which is must be propositional to v g s minus v t the whole square right and. So, this voltage the source voltage is now much lower than what it would have been right, if it had if the drive waveform and arrived on time and therefore, the initial glitch current will be higher or lower than otherwise.

Student: Much higher.

It'll be much higher than otherwise you understand. So, if let me call this m 1 and m 2 if m 1 and m 2 are off simultaneously leads to large glitches which means poor dynamic linearity right please note that this non-linear phenomenon due to the glitches occurs

regardless of whether the tail current sources are matched or not matched all the tail current sources being matched will only mean that the static linearity which is the steady state settled value of the current as a function of digital code is is good; however, these parasitic capacitances contribute to nonlinearity of the entire waveform not just the settled value and as we discussed last time around there are many instances or applications where the linearity of the entire waveform is of interest and not just the settled value ok.

Student: So, the key point is to try and avoid.

Large voltage swings at the source coupled node. So, at to achieve good dynamic linearity you want to make sure that the voltage excursions at v x are.

Student: As small as.

As small as possible 1 particular point to avoid is to keep to make m 1 and m 2 both simultaneously off which is easily possible if the timing waveforms are skew you understand so. In fact, 1 common thing to do is to move this cross point such that.

Student: Neither of these.

Neither of these transistors is off simultaneously you understand

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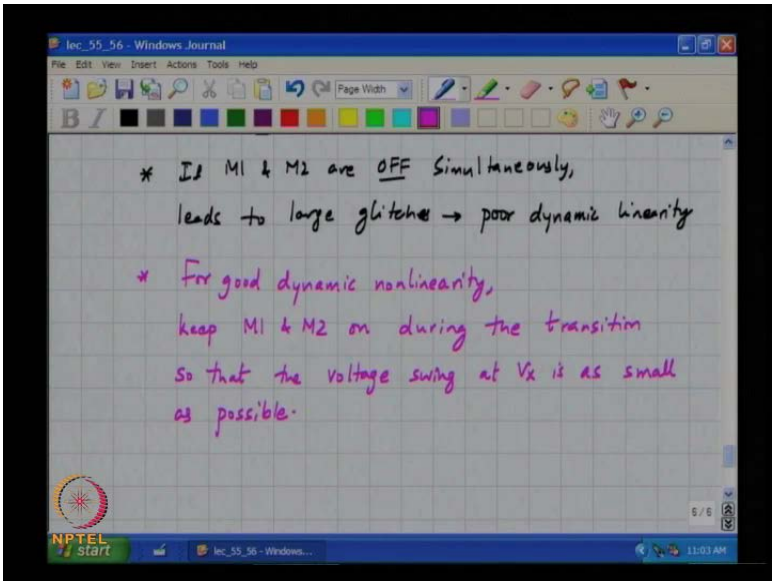

So, for good dynamic nonlinearity keep m 1 and m 2 on rather than during the transition. So, that the voltage swing at v x is as small as possible all right ok

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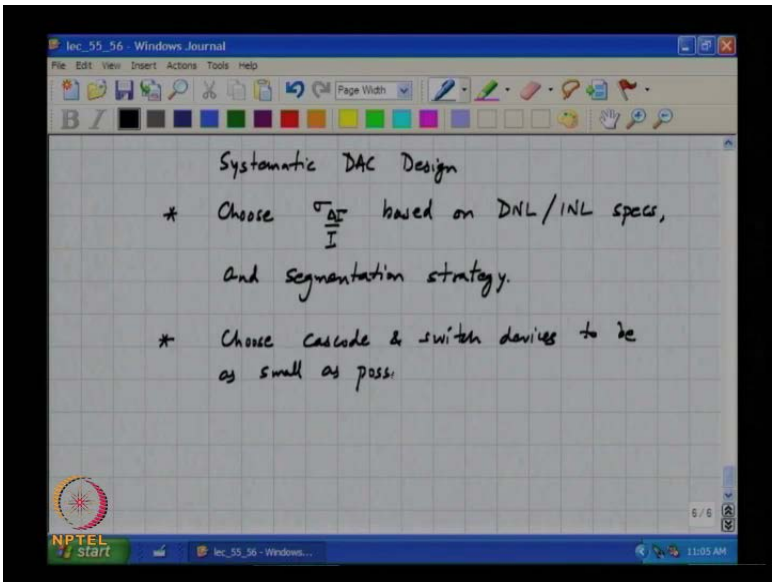

Now, putting all these together if you want to design a DAC first choose sigma of delta I by I based on DNL slash INL specs and segmentation strategy all right as we saw the last time around to achieve a given sigma DNL and sigma INL you have 2 knobs to play with 1 is the segmentation percentage segmentation and the other 1 is, the sigma delta I by I and we saw that for a given sigma delta I by I there is an optimum.

Student: Segmentation.

Segmentation right for minimum area once you do that we choose the current shell design I mean you basically know the size you need for the tail current transistor right and the cascode device and the switch devices are chosen to be as small as possible while being able to support the current. So, choose cascode and switch transistors as small as possible the next thing is to try and play the whole thing out. So, now, the question is let us say I have a ten bit converter with six plus four segmentation six thermometer bits and four.

Student: Binary binary.

Binary bits.

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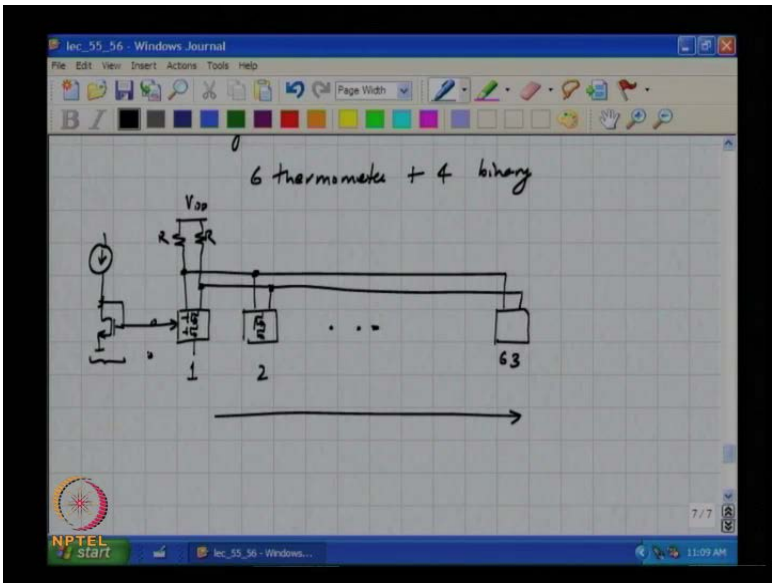

Now, this means that I will have 603 current sources for the thermometer DAC and and I have four bit binary DAC all right. So, I have a 6 bit thermometer DAC that is a you know there are any number of waves which you can place sixty 3 current sources. So, 1 thing is to say I am going to place current source 1 here physically current source 2 here and. So, on until I have current source sixty 3 here right each 1 of these has got tail current source and switch and. So, on you understand and then I will join up all these and go to v of p and v over what do you think is the disadvantage with this.

Of course the DAC looks very unwieldy simply because it is thin and and long you understand if you put I mean imagine your bricks and you put them all like this they will run from I mean these are very thin and the skinny kind of layout right and it turns out that in practice on an IC it is not just that there is random mismatch there is also some systematic gradient of process parameters. So, for example, the oxide thickness may change slowly along this direction which means that whatever current mirror you use to set the bias voltage assumes that the oxide thickness is what there is on the left side of the.

Student: Array.

Array right. So, if the oxide thickness vary slowly as you keep going from the left to the right you will find that there is I mean there is systematic mismatch or gradient because

of the small change in the oxide thickness or for instance the mobility across the as you go across the DAC it may also turn out that threshold voltage varies in a systematic way.

Student: Across.

Across the dive which will which is which will also happen with the oxide thickness changes slowly you understand another thing is that if you connect all these the sources of all these transistors together there will be some small drop along.

Student: Source interconnect.

That source interconnect right because the bias voltage you are applying is between these 2 voltages, but the interconnect is got.

Student: Small resistance.

Some small resistance and as you keep going from the left to the right the drop across the interconnect resistance keeps.

Student: Increasing.

Increasing does it make sense. So, to prevent I mean 1 way of preventing you know gradients from accumulating is to. I mean fundamentally what is 1 way of accumulating I mean if you are if you layout current sources from left to right in an array they will go across this entire table and let us say this the there is a gradient which slowly.

Student: Is happening.

Is happening from the this end to the other end if you want to avoid the gradient what will you do you would ideally like to put all the current sources.

Student: As close.

As close to each other as possible. So, that.

Student: Any.

Any variation across they dye does not. Cause problems of course, physically it is not possible to put all the current sources at the same place you will try and minimize the

area occupied by these current sources I mean in other words you want to make them all as close to each other as possible right 1 way of doing that is to put them as a square array rather than as a linear array and it turns that also simplifies the decoding logic a little bit.

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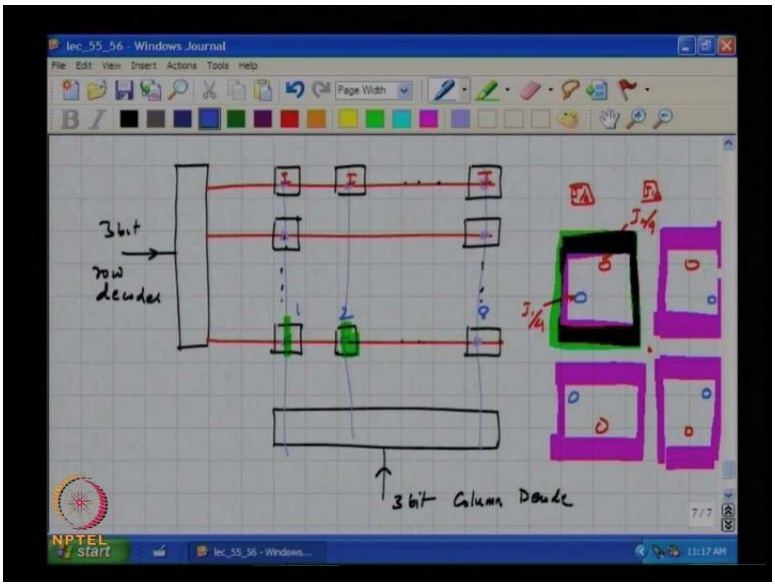

So, for example, we can lay them out as a square array of current sources. So, in our example it was a six bit array all right. So, if you break it up as an arrangement of 3 by 3 then you can play them out in rows and columns 8 rows by eight columns. So, you have what is called a column decoder and a 3 bit row decoder this is very similar to how you address a memory set and locally this is a 3 to eight decoder and this is also a 3 to eight decoder and locally you can when a particular cell needs to be selected both its row and column address must be 1 ok.

So, you can appropriately generate logic signals which will make sure that the right number of cells are selected and this way the extent occupied by these current sources the physical extent occupied by these current sources is much smaller than what you would it would be when you laid them out.

Student: Linearly.

Linearly now you can do a better job by breaking this up for example, into four sub quadrants right. So, let us say instead of having current sources of value I here a given

current source is broken up into four sub current sources of I by four each . So, now, you can make 1 way of making it more uniform is to say I will make four arrays of I by four current sources each and then arrange them I mean each of these sub arrays will be much smaller then this big square array.

Now, if I do that let us in abstract it out like this a certain current source I 1 has got a representation here a representation here a representation here and say a representation there right and this is and then I will choose I 2 here say here here and here all right. So, 1 thing you can see is that all these I mean this is I 1 by four if you like and four of them connect in parallel this is I 2 by four and so on. So, what happens is that all of these are chosen to have the same centroid therefore, linear and I mean if you have linear gradients it will get.

Student: Simply.

Simply average you understand and. So, now, you have to only worry about the mismatch you know between there will apart from linear gradients they are also be quadratic gradients and. So, on so, but the average separation between current sources is now a lot smaller then it was if you had a single big array. So, a this is also a fairly common thing to do this is also a ways of I mean placing these current sources in such a way that you get better spectral properties by you know a placing the I mean at this point it is not clear whether you must arrange these current sources is 1 2 number 1 2 all the way to eight nine ten and. So, on and there is any number of ways of arranging these things correct with appropriate change in the logic you will be able to address them properly.

So, it turns out that their techniques of choosing arranging these current sources properly in ways that kind of randomize the errors due to gradients not mismatch random mismatch is nothing you can do about, but if they are systematic gradients by choosing these locations randomly right you can do things the final thing that we wish to add is that the delay in these decoders will be data dependent and it is combination of logic. So, depending on the sequence and prior history that delays may change correct if you use these these signals directly to go and address the cells the times at which that these these cells which will depend on prior history in some non-linear fashion and cause distortion

at a high frequencies right. So, what? So, what is the standard solution to avoid these random delays. Every time these signals at the.

Student: Current cell.

At the current cell. So, at the switch level

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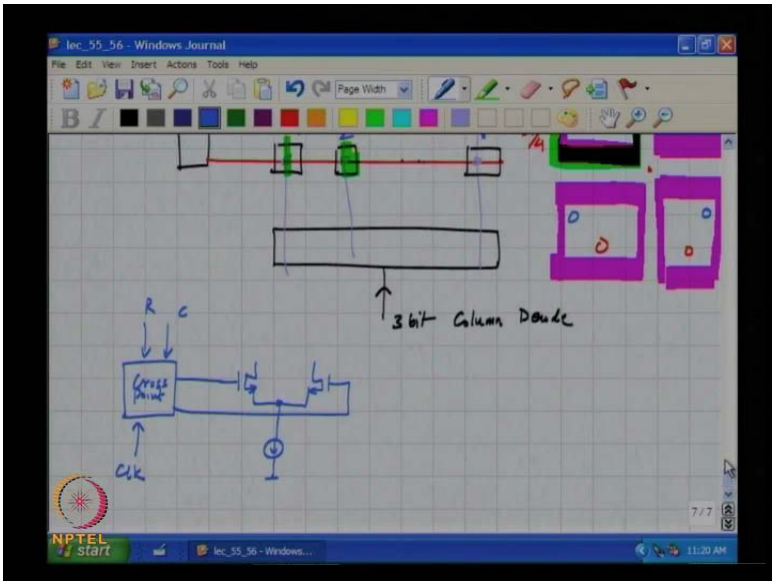

There is some switch driver logic which looks at the row decoder the column decoder and the master clock and make sure that adjust the cross point properly and sinks it up with the clock. So, this way the drive waveforms of all the current sources are sinked to the clock and therefore, random variations in delay due to data dependent delays in the combinational logic also become no longer a problem. So, this is what a basic current cell will look like.

There is a method which bring you top load that rating 3 sets 2 into 2 four coordinates and that is thing saying that we are randomizing the this systematic offsets so. We are I mean actually the average separation between current sources is going down by this thing correct. So, on the average that separation between I 1 these 2 current sources is much smaller then what they would be if you are made a.

Student: Arrays.

Big array that is all correct. So, so this. So, I guess I will have to stop here as far as current steering DACS are concerned this is you know it just touches the surface of a current steering DACS hopefully with the with this background you should be able to read up with the papers and understand stuff and a lot more detailed fashion . So, in the next class we will take a look at I mean the last topic that I wish to cover namely. So, far we have seen that the I mean if for example, a current steering DAC like this was used in as the feedback DAC in a delta sigma convertor there is going to be.

Student: Mismatch.

Mismatch between these elements and as you've seen in your assignments mismatch in these elements will cause I mean ideally for a multi bit modulator the spectrum

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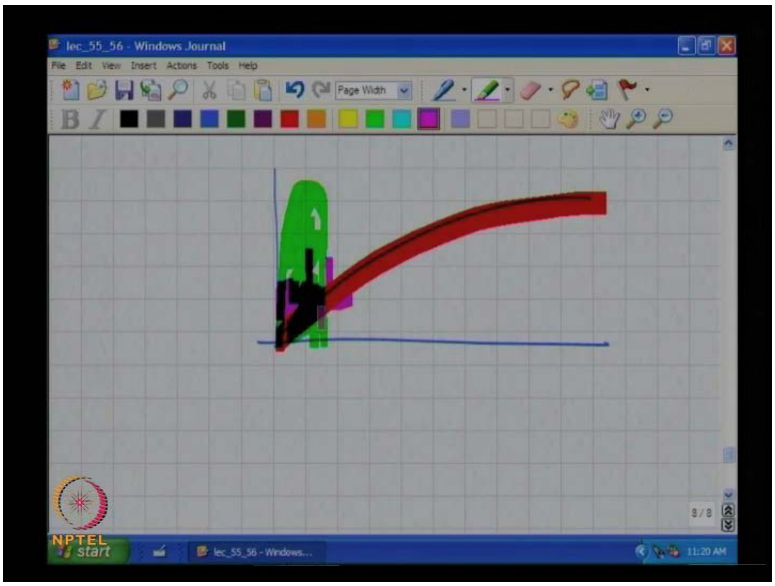

The p s d must look like this with and this must be the input signal and this is the shape quantization noise if the DAC was perfectly linear if the DAC is not linear what happens as you have seen in your assignments there is the low frequency part you know noise floor rises and there is also distortion when the input is the sin wave. So, in the next class we will see the intuition for why this happens and what we can do to.

Student: Prevent this.

Prevent this. So, we will continue on Monday.