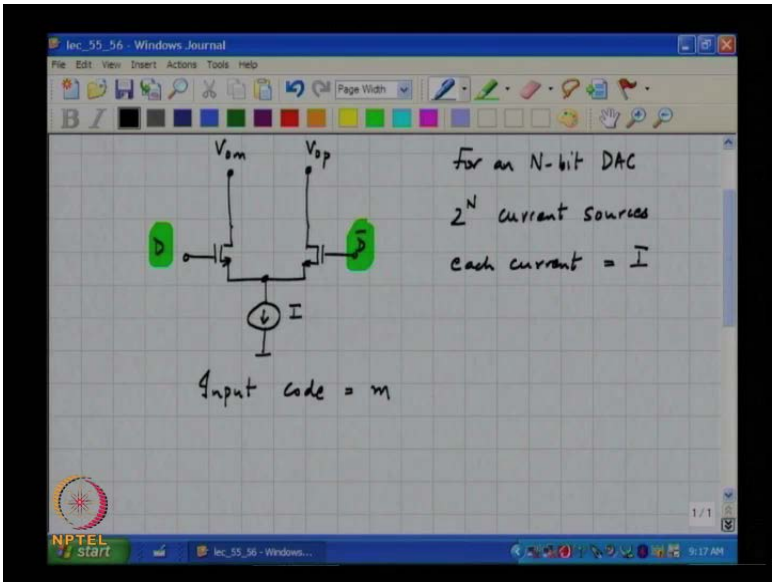
VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 55
Current Steering DACs -1

This is VLSI Data Conversion Circuits lecture 55. In the last class we were talking about Current Steering DACS, today we will continue along in that direction.

(Refer Slide Time: 00:28)



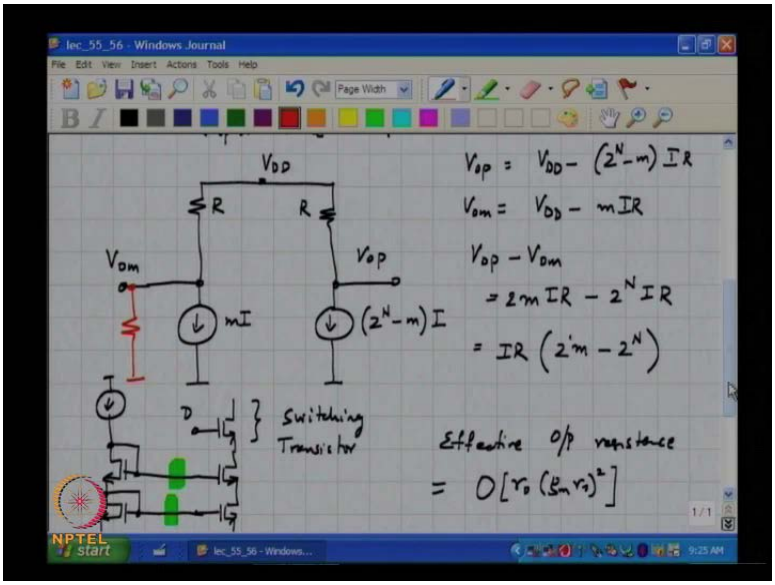
So, as we were discussing the last time around the basic idea behind a current steering DAC is to have a tail current source of a differential pair being driven by complimentary signals. And if D is a logical high D bar is a logical low in which case this current gets cleared towards the left and vice a versa.

So, if this is V o m and this is V o p, then you can combine a whole bunch of current sources right, you can add them up using Kirchhoff's current law by connecting them together. And this way depending on the digital code D you will get an output current which can be converted into a voltage in any number of ways the simplest ways to simply pass these currents through a resistor alright. Or you can go into a trans impedance amplifier type structure where you have an op amp based feedback loop and you can convert that current into a voltage.

Now, for an n bit DAC you have a 2 to the n current sources these current sources are

each assumed to be I. And you can address these current sources in many ways as we were discussing the last time around, they can all be addressed in a thermometer fashion or they can addressed in a binary weighted fashion or some via media. Where you can use the knowledge of the requirements in the DNL and INL to go and choose the appropriate degree of segmentation. But, the bottom line is that the total amount of current that you need to steer one way or the other remains equal to 2 to the n times I right.

(Refer Slide Time: 03:29)



Now, for a input code M, whichever way you decode the digital data and supply them to these current steering cells, there will be M current sources eventually steered towards the left and 2 to the n minus m current sources steer towards the right. And if you assume that we have a voltage to current conversion which is simply based on resistors then V o p will be V D D minus 2 to the N minus m times I, V o m is V D D minus m times I. So, V o p minus m I R V o p minus V o m will simply be m I R times 2 minus 2 to the N times I R which is I R times 2 m minus 2 to the N.

So, when all the current is flowing towards one side which will happen when either m is 0 or when m is 2 to the N, or could the N minus 1 actually right. You will find that the output of the DAC will reach 2 to the N times I the differential output is 2 to the N times I times are plus or minus at midcourt the output will be 0. Now, unfortunately each of these current sources will have a finite output impedance and therefore, what happens is

that this current source is not ideal please recall that as we were discussing the last time around. These current sources are actually implemented using MOS transistors and an example of a good current source, where the output impedance is been enhanced is to use some kind of cascade.

This is not a particularly good choice of biasing the cascade voltage, but I hope you get the idea in your other classes I am sure you have seen better ways of biasing the cascade where you do not waste, so much head group right I am assuming that you know all that stuff. In any case whatever you do finally, the output impedance of the current source will not be infinite we can only make it larger and larger and larger right.

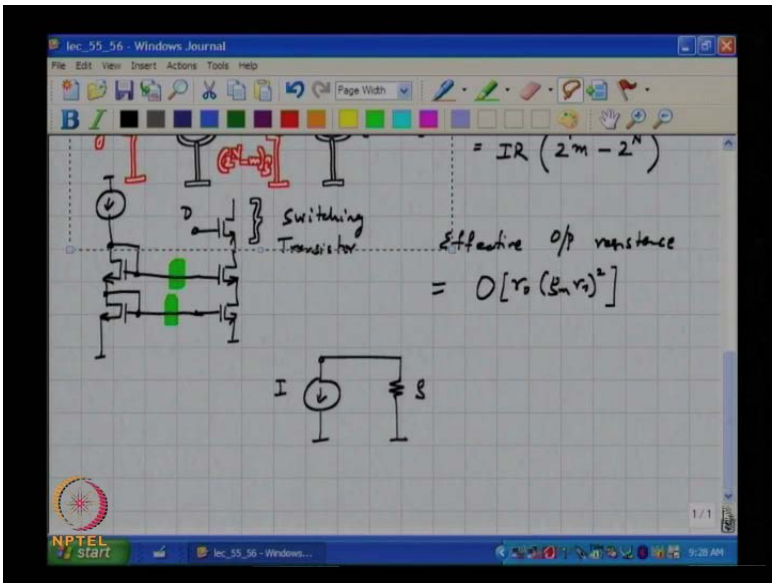
And on top of this you also have in effect another cascade because when the current source is fully switch to one direction. The switching transistors which are 2 in number one of them will be off and the other one will be on. And effectively if you make sure that the switching transistor does not get into the triode region, which is easy enough to do all that you need to do is make sure that V D D is high enough right.

So, if the switching transistor is in the saturation region then effectively the switching transistor also acts like a cascade device right it is another common gate stage. And therefore, the effective output impedance of the tail current source is multiplied by a further factor of g m times r o. So, the effective output impedance is of the order of r o from the lowest transistor times g m r o the whole square. Of course, the r o's of the all the three transistors will not be the same, but this is intended to give you an idea of the order of magnitude of the output resistance is this clear.

So, in other words what we have is not really this scenario where we have an ideal current source and where in the ideal case we have two current sources which are digitally controlled both of them pump current in to the same resistor; and we are looking at the difference between the outputs of these the voltages across these resistors.

In practice what we have is that on one side we have a conductance of value conductance I mean the idea behind using conductance is that you do not have to keep carrying you know 1 by has all over the place. So, what is the output conductance of this m I current source, if you call the output impedance of each one of these current sources..

(Refer Slide Time: 11:16)



Let us assume that each of these current sources has an output conductance g right, this g is of the form 1 by some g m r o square times r o in this particular example. So, if you have n current sources coming together the output conductance will be m times g and you have 2 to the N minus m current sources coming together we will have 2 to the N minus m times g right. So, this is a model to understand what happens with finite output impedance. So, what is I mean before we get into the details what do you think this does; well that is can you guess what this will do to the output characteristic of the DAC is it a linear effect or is it a non-linear effect.

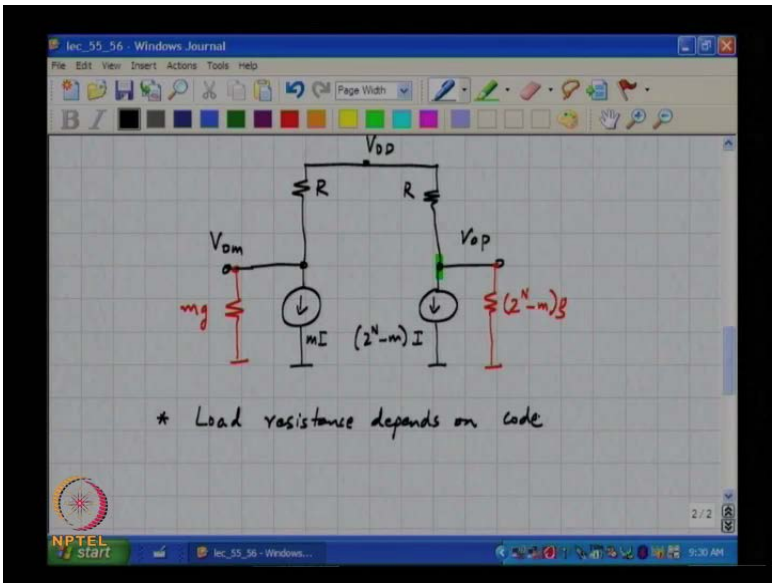
Student: Nonlinear sir.

Why is this a non-linear effect.

Student: There is error in the n-th code is dependent on that.

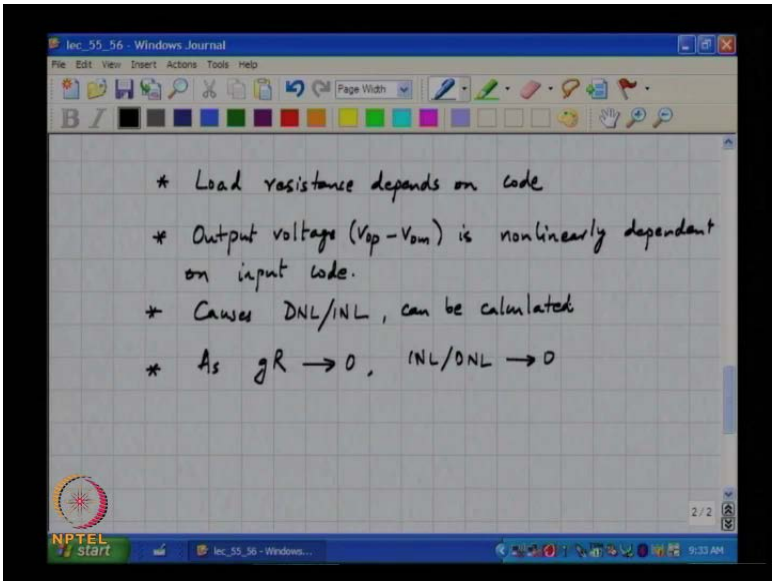
So, as you can see the differential voltage depends on the differential current, which is a linear function of m finally, we want the output voltage to be a linear function of m that is what a linear DAC will do correct. So, as far as the Norton equivalent or the short circuit current is concerned that seems to be quite linear with the digital code m the problem is that the effective load resistance becomes is also code dependent. So, when you multiply this current with the output resistance which is code dependent the characteristic becomes non-linear all right.

(Refer Slide Time: 14:45)



So, the output voltage this is m I is 2 to the N minus m times I and this conductance is 2 to the N minus m times g. So, we can convert this into a Norton equivalent right and so, not going to go at the details of the calculation here I think you can do it yourselves, the bottom line is that the load resistance depends on code.

(Refer Slide Time: 15:58)



So, output voltage V o p minus V o m is nonlinearly dependent on input code, which means this causes DNL slash INL you can of course, do the math and find what the DNL or INL will be for a given g correct. So, but one thing we can say with certainty is that as

g times R tends to 0 the INL and DNL will also tend to 0, why g times R why not simply g.

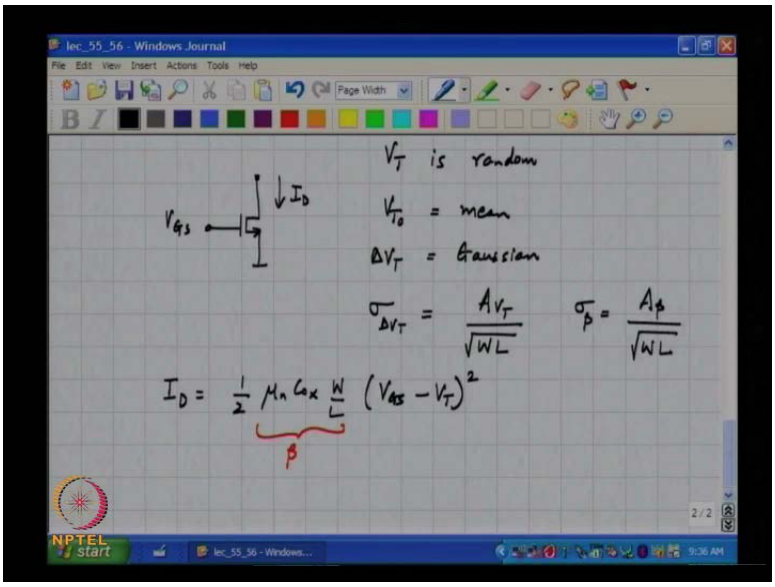
Student: ((Refer Time: 17:55))

[FL]

Student: ((Refer Time: 17:58))

So, finally, you are only interested in how much of this current passes through these two resistors right. So, for a given g if the R of the conductance of the load resistors is much smaller, then a larger fraction of this current flows through the load there by which is equivalent to saying there are smaller fraction flows through these conductance's and the current through these conductance's is responsible for the error correct. So, as a limiting case if the load resistance was 0, regardless of what g was all these current would flow into R correct, which means that the output voltage will be linear you understand. So, in other words depending on the D C DNL and INL requirements and the desired resolution of the DAC one can go and figure out what the ratio of the output impedance of the current sources 2 v load resistance must be, so this determines all right. So, the next thing is the matching of the current sources itself as we saw the last time around.

(Refer Slide Time: 20:00)

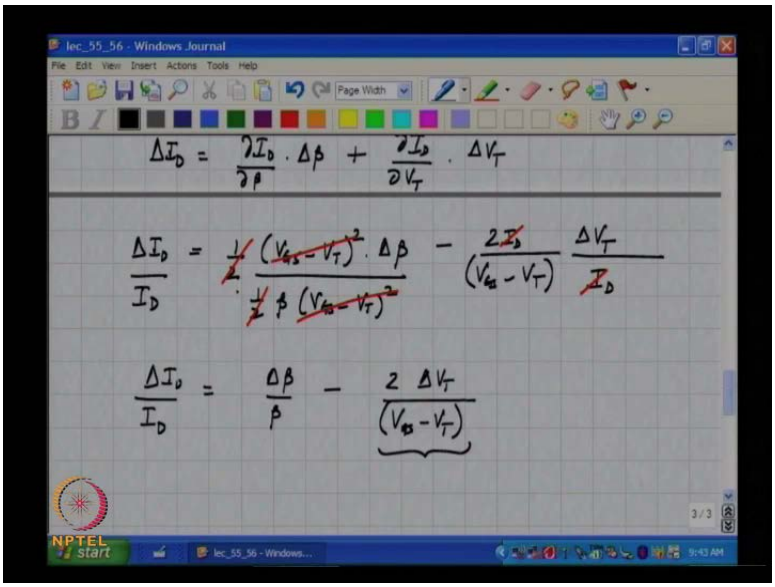


The matching of the current sources along with the choices of segmentation determines the sigma of the DNL and INL correct So, it turns out that the v t of the transistor is a

random variable and with some mean V T naught and a delta V T which is assumed to be Gaussian with a sigma delta V T of which is of the form, A V T divided by square root of W times L. And assuming where the transistor current I R is written as half mu n C ox W by L times V A S minus V T the whole square.

The fact that this V T is varying randomly around a mean means that the current I D will change in a random fashion and unfortunately it also turns out that this. So, called mu n C ox W by L it is beta factor is also a random variable. So, there is also this is often called the beta factor and this sigma of beta is nothing but, some a beta divided by square root W into L

(Refer Slide Time: 22:51)



So, the change in the current due to a change in beta and due to the change in V T is given by dou I D by dou beta times delta beta plus dou I D by dou V T times delta V T; and this is nothing but, half into V G S minus V T the whole square all right times delta beta plus dou I D by dou V T is nothing but, by definition is the same as.

Student: It is minus g m.

Correct. So, and g m is nothing but, 2 I D by VGS minus V T times delta V T, so sigma or delta I D sigma square of delta I D is nothing but, squared sum of these thing. So, it often make sense to do finally, we are interested in the percentage change the absolute change in the current is I mean it is relevant, but it is only half the story you need to

compare the absolute change in the current to the actual current right.

So, at you have something which is dimensionless and these goes into all those DNL slash INL calculations that we saw earlier; there we saw that with respect to resistors here it is with current sources, but the change in the unit element is delta I by I which is got some variance is it not. For different devices the you know the properties of the equations of the device mandate different expressions for this sigma of delta I by i, but otherwise beyond this the calculations you will do to determine what this variance or mismatch factor must be in order to achieve a given DNL and INL still remains the same.

So, let us do, so delta I D by I D is nothing but, 1 half beta into V G S minus V T the whole square and this is 1 half beta into V G S minus this I will just call this I D and we see that this goes away. And this goes away leading to delta I D over I D is delta beta by beta minus 2 delta V T by V G S minus V T the whole square V G S minus V T and this makes intuitive sense alright. Why do you think this expression makes intuitive sense this is telling you that, if you want let us say for a given current you want to reduce the error in the current for given delta V T.

Let us say that threshold changes by a certain amount this expression is telling you that for the same current if you increase the get over drive voltage the error in the or the mismatch in two nominal currents will be smaller if VGS minus V T is larger. So, why do you think this makes intuitive sense, now what I am saying it is all fine that this comes out of the math right, but the question is why does this make intuitive sense or does it make any sense at all.

Student: ((Refer Time: 28:32))

It that is correct that is what comes out of the math that is correct.

Student: ((Refer Time: 28:39))

No we are interested in for the same current right, if you had you want to have the same unit current only than you can compare a things reasonably.

Student: ((Refer Time: 29:05))

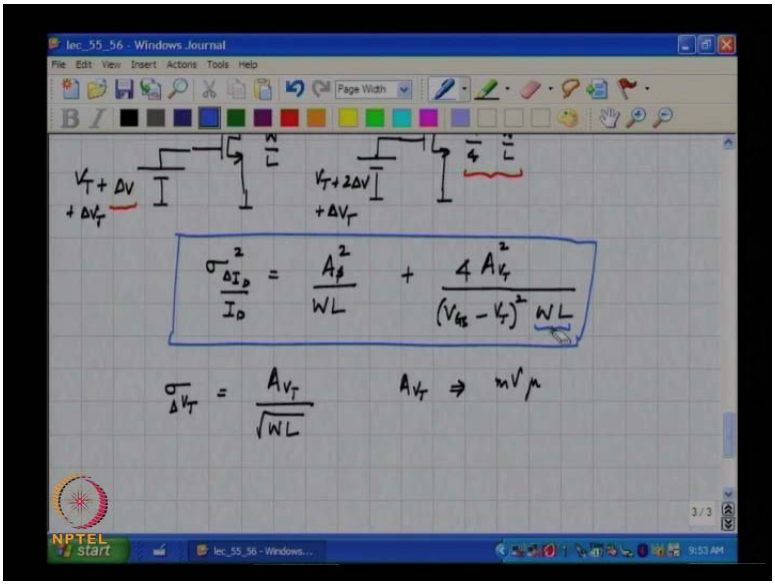
Delta beta of course is a acts like an incremental VGS that is correct, so what

Student: ((Refer Time: 29:28))

No, no what I am getting at or what I am trying to point out is why do you think this VGS minus V T appearing in the denominator make sense.

Student: ((Refer Time: 29:50))

(Refer Slide Time: 30:06)



Let me, so let us see you have two transistors let us say for argument sake say this is W by L and this is 1 4th W by L right both of them are biased, so as to have the same current, so what must this voltage be.

Student: ((Refer Time: 30:45))

[FL] this voltage if this is V T plus it is plus delta V this must be V T plus 2 delta v it must have twice the over drive in order to result in the same current. Now, let us say the v t changed by a little bit this is delta V T this is delta V, clearly this drain currents in both the transistors will change, which of them will have a larger change or which is larger delta I 1 or delta I 2.

Delta I 1, now why does that make sense.

Student: ((Refer Time: 31:40))

No, so the W by L is higher is one way of looking at it alternately you can say that the

overdrive is smaller for the transistor on the left. So, the trans conductance of that transistor on the left is higher which means that for the same change in the, in the threshold the change in the current will be larger for the transistor which has a higher trans conductance you understand. So, in principle if you want to be immune to threshold mismatch you should make this transistor infinitely small and have an infinitely large VGS minus V T right.

In which case a small change in threshold will mean no real change in the current, in practice of course, you will always be limited by head room is it not. If you want to have a very large VGS minus VT, it means that somewhere I mean this transistor needs at least VGS minus V T to remain in saturation. So, if you go on increasing VGS minus V T you will find that you use a polyhedron just to maintain one device in saturation, so that is a practical limit.

So, when you are designing a current stating DAC for example, if you have resistive loads the peak to peak output swing is some specified quantity right, which and the load resistors are also specified which means that the sum total of all the currents is known which means that the unit current cells current is known alright. And you want to keep all the transistors in the saturation region including the switches right, I mean one straight forward argument to say why you want the switch transistors to remain in saturation. Is that we saw just now that you want to make sure that the output resistance of each of these current sources is as high as possible.

So, that is one reason to make the switch transistors operate in saturation you understand. So, once you know the peak to peak voltage swing at each of the output nodes of the DAC, it then means that because you want to maintain at least three devices in saturation right, the supply voltage minus the peak to peak swing must be split in some way across three devices alright, which will boiled down to the fact that for a given supply voltage there is only.

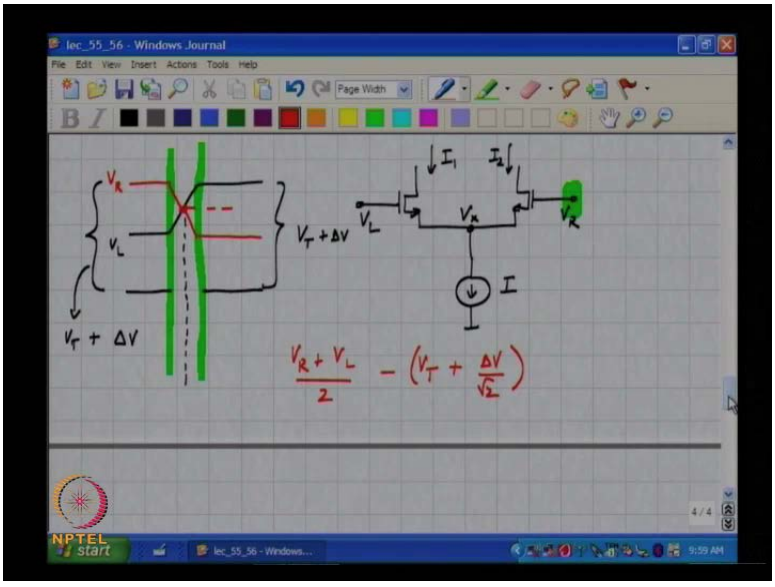
So, much VGS minus V T that is possible across the lowest drain the lowest device which is what sets the current all right. So, for that VGS minus VT if you find that the mismatch is too high this delta I by I D is too high, then there is no way out for a given threshold volt VGS minus VT you simply have to go on reducing this delta VT and how do you go on reducing delta V T. You keep W by L the same right and go on increasing

W into L and that can be done by simply scaling W and L by the same factor you understand.

So, the sigma delta I D by I D is a sigma square is given by sigma square of delta beta by beta plus 4 by VGS minus VT the whole square times sigma square of delta VT. So, sigma VT as we just discussed or sigma delta VT is A V T divided by square root W by L square root W times L and what are the units of A V T.

I mean voltmeter often coated in milli volt micron. So, sigma square VT will be A V T square divided by W L. So, this will be A V T square times W into L and sigma square delta beta by beta will also be some a beta square divided by W times L does it make sense. So, if for the same current you want to reduce the mismatch or in other words if you want to reduce this delta sigma delta I D by I D, the only way you can do it is to keep W by L the same and keep increasing W times L alright. Assuming that you have maxed out the V G S minus V T does it make sense alright.

(Refer Slide Time: 39:25)



So, the next thing is to try and figure out what happens when the current cell is actually switching. In other words assuming this current is I 1 and this current is I 2 and this tail node is denoted as V x the voltage here is probably doing something like this while V E left I will call it and V right and V R is doing this. So, can we comment on what happens to V x, what is it way before this transition.

Student: ((Refer Time: 41:52))

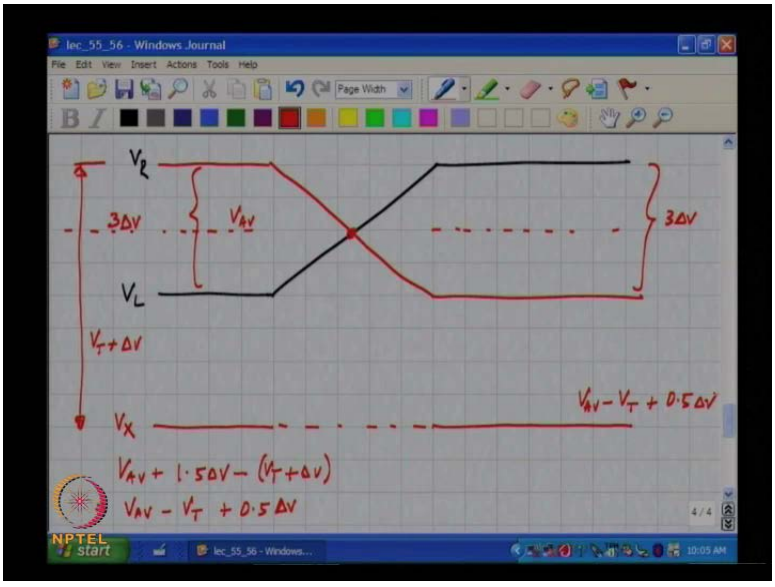
So, way before the transition all the current I will be flowing through there a transistor on the right. So, the voltage will be this voltage will be V R that difference will be V T plus square root of 2 I by V N C ox W by L. If I now call this delta V, I want to say this will be V T plus delta V and way after the transition after all the transients are settled the voltage must remain all the current is flowing in the left transistor assuming the two transistors identical the voltage must remain V T plus delta V.

So, the question now is what happens in the middle, what do you think will happen when we are at this point where the two drive waveforms cross each other, no it will not be the average value of.

Student: ((Refer Time: 44:00))

Both of them are carrying the same current, so the difference you have to worry about is between here how much lower than this waveform the average value of V L and V R will the node V X go to, when both the transistors are carrying current, what happens to their overdrives. The overdrive will go down by a factor of root 2 and therefore, what will happen will be that the voltage will be V R plus V L by 2 minus V T minus A V T plus delta V by root 2 does make sense.

(Refer Slide Time: 45:30)



And so, the V x waveform if I exaggerate draw this in a very exaggerated fashion like

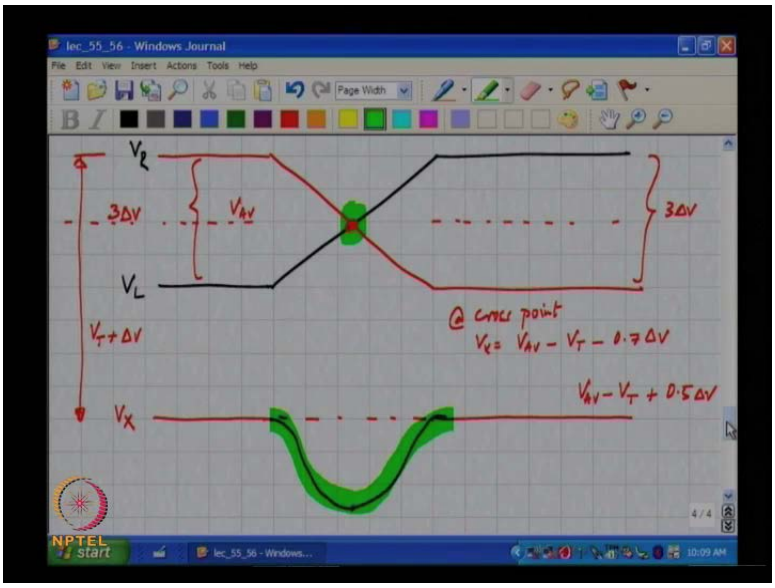
this is V R, this is V L. What will be the difference between V R and V L I mean or rather can you comment on the difference between V R and V L in relation to delta V, what is the idea behind having V R and a large difference between V R and V L. You want to make sure that the current completely switches to one side which means that the difference between V R and V L must be at least delta V right in practice it will be several times larger.

So, let us just assume for argument sake that the this is say three times delta V right definitely a safe value to choose given that this will completely switch the current from one side to the other there is nothing holy about three I just chose it. So, which means that this V x before the transition occurs is the average of V R and V L minus. So, this difference will be V T plus delta v all right and this absolute voltage is V R plus V L by 2 and the same thing happens well after. So, this difference is also assumed to be 3 delta V at the cross point what happens the difference will be a V X will be V T plus delta V by root 2 from this voltage. So, do you think it will be lower than this or higher.

Student: ((Refer Time: 50:08))

You tell me, it is correct this is V T plus delta V from V R that is correct thank you all right. So, from the average how much lower than the average is this let us call this V average this will be V average minus V r is nothing but, V average plus 1 and a half delta V and this will be minus V T plus delta V. So, this is v average minus V T plus half delta V does it make sense; whereas, the middle voltage will be what will be the voltage V X at the cross point of the two waveforms. It will be v average minus V T minus delta V by root 2 correct. So, what happens that is what you think the waveform in the middle will dip or will rise.

(Refer Slide Time: 52:58)



This voltage will be V average at cross point V X must be v average minus V T minus 0.7 delta v. So, what happens in the middle it will go down or go up it will go down. So, we are getting into the details of the waveform at least one you can say is that the waveform actually dips you understand alright. So, in the next class we will see what happens, so please bare this in mind that during the transition assuming perfectly symmetric wave forms.

So, that the cross point occurs exactly at the average of V R and V L the voltage at V X actually undergoes a dip like this, this is assuming that everything I mean all these a calculation was done assuming that everything is within quotes static it is as if V L and V R are moving. So, slowly that the currents through all I mean in practice they will be currents at this there will be additional current in apart from I due to, what parasitic I mean if this voltage is changing with time then the parasitic capacitance at that node will cause a reactive current right which will be in parallel with I, but all are calculations.

So, far based I mean for voltages have all been base based on D C considerations, which means that the, we have neglected the current through the parasitic capacitances. So, in the next class we will see what happens when these parasitic capacitances are considered alright.