VLSI Data Conversion Circuits
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Lecture - 54
DAC Nonlinearities

This is VLSI data conversion circuit lecture 54 in the last class we looked at the various tradeoffs between the degrees of segmentation that are possible when realizing a DAC and we said that all things being equal it makes sense to have a decoding which is more segmented than one which is less segmented and we said the motivation for that was if the sigma INL remains the same and we can have a lower sigma DNL you are; obviously, doing much better than you were doing with a solution which had a higher sigma DNL.

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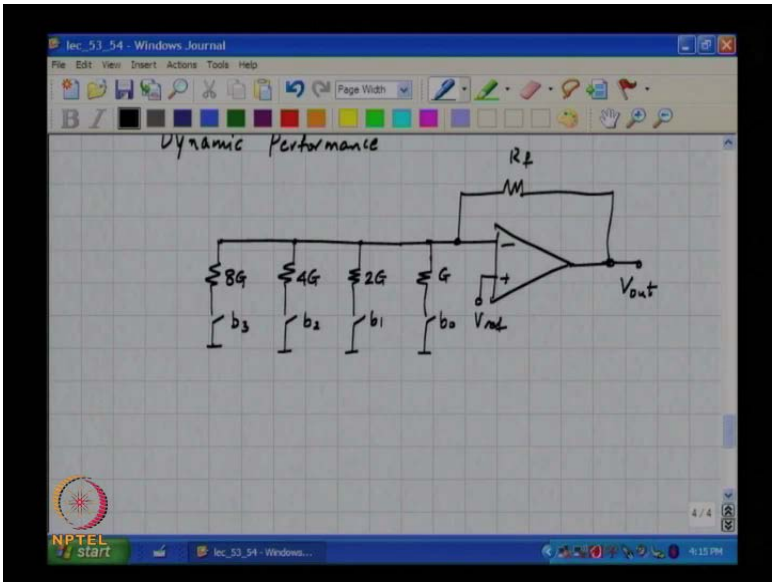

Now, let us look at another allied issue which is dynamic performance especially with regard to binary versus thermometer decoded DAC's. So, again let me go back to my simple example which was a 4 bit DAC example. So, this is G this is 2G this is 4G this is 8G and this is controlled by b 3 b 2 b 1 b 0 V ref R f and V out.

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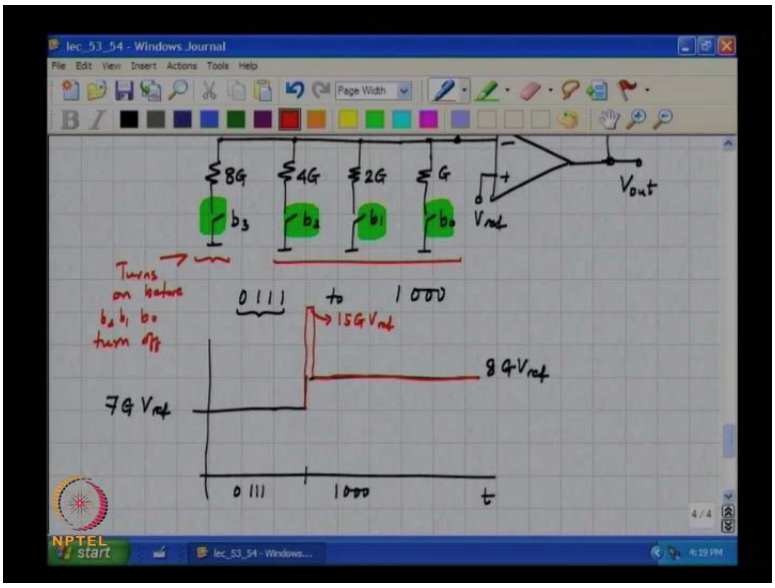

Now, let us kind of see what happens when the digital code changes from 0 followed by all one's to 1 followed by all zero's when the digital code was 0 followed by all one's the output voltage if I plot it as a function of time would be seven times G times V ref let us assume that this is the instant at which the code changes from 0 followed by all one's to 1 followed by all zero's if all the elements are perfectly matched and b 2 b 1 and b 0 turned off at precisely the same instant as b 3 turned on the output waveform would look like this where this is 8G times V ref on the other hand if there is a small timings queue between the instances at which b 3 turned on and b 0 b 1 b 2 turned off in other words let us say b 3 turns on before b 2 b 1 b 0 turn off.

So, there is now certain instants a certain period of time where all the switches are on. So, assuming the op amp is infinitely fast and such what do you think will happen to the output waveform. It will…

Student: Sir, this will more might be to 15.

It will momentarily go to a very large value in this particular case 15G times V ref and come back to 8G times V ref does make sense. Now consider what happens when the code changes from 2G to 3G any comments

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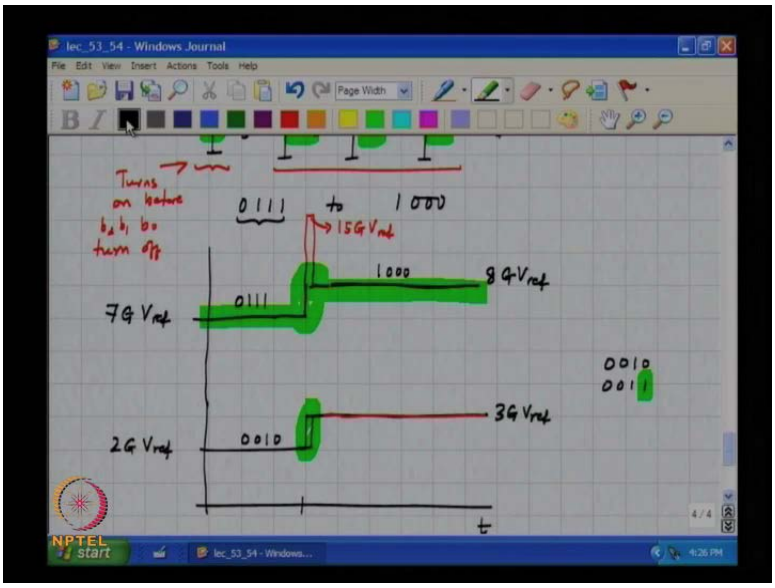

It is 2G what will the when the in other words when the code goes from this is the situation when zero followed by all one's to one followed by all zero's I am interested in what happens to the waveform when I have 0 0 say 1 0 to 0 0 1 1. It should be 2G V ref here and 3G V ref what happens when there is timings queue, when because that transition the transition will be because of I mean it go to that will V be. Pardon why let us say the only thing I mean if here if we assume that say the transition of this is delayed slightly I mean only one current source is switching one conductance is switching. So, the transition will occur.

Student: After delay slight after slightly delayed.

Slightly delayed with respect to the current source with respect to the when the code changes. So, can you comment on the 2 situations we have seen. So, far and what that means. Second times issues like what will happen in thermometer.

Student: well. t should be adding one by one.

But is that something more glaring that you notice.

Student: Number of times V it is.

Pardon.

Student: Number of times with it is?

No the error space in error is means if you had taken the output at the beginning or let us say integrate that and get an error.

Student: No one thing is that nothing is switching off only current sources are getting more and more added.

Correct.

Student: Where as in the previous case three of them were switching off and one of them it is turning on.

That is correct.

Student: If there is a time I mean if there is a time delta t difference between how fast you can turn on and how fast you can turn off.

Correct.

Student: Then you will see the sir kind of spikes you say

Yes that is correct but…

Student: There is even if there is sir such kind of timings queue in the second case you will not see any kind of spike ladder.

So, basically one thing that is apparent is that the actual waveform coming out of the DAC is the ideal waveform plus some error which we will call a glitch correct. Now, if the DAC was perfectly a linear system in other words if you are able to relate the output waveform to the input sequence through a linear system whether you go from the code goes from 7 to 8 or from 2 to 3. The size of the step and the nature of the change in waveform must remain the same correct what do you see here now there are very very different simply because when you go from 2 to 3 I mean the do you get the ideal step plus which is just delayed by little bit, but when you go from 7 to 8 you see that.

Student: Spike

There is a big spike even though the change in the input code remains the same it was the change in the code was one and both cases; however, the change in the output waveform was very different depending on what code was there before you increase it by a by 1.

So, and please note that this is even with all elements being matched perfectly if you look at only the settled waveform there is no difference, but a lot of times we are interested in not just a settled waveform, but in the spectrum of the DAC output. Can you tell me a case in point where you have seen where you think the spectrum is important and not just the settled value.

I mean you have seen this throughout this course in a continuous time delta sigma modulator for instance you are not I mean you are not looking at the simply the settled waveform correct because the modulator is integrating the difference between or filtering the difference between input signal waveform and the DAC feedback wave form not just the settled value of the DAC you understand and there are lot of other situations in practice where is not just the settled waveform of the DAC that matters, but the entire waveform in which case this is clearly a manifestation of nonlinearity. This is called dynamic nonlinearity simply because as far as settled values or static values are concerned everything seems fine because we have assume perfect matching.

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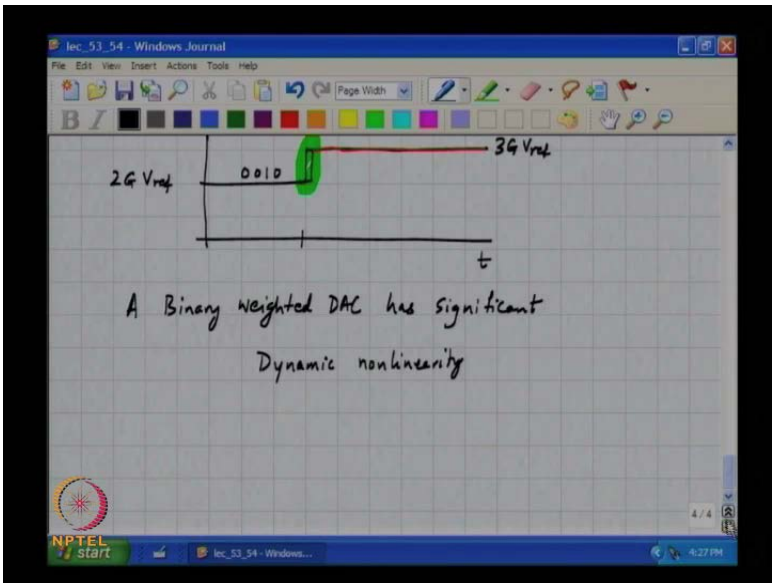

So, a binary weighted DAC has significant dynamic nonlinearity since equal changes in the input code result in different changes in the output waveform depending on the initial value of the code and this is all that is needed to establish the fact that a binary weighted DAC can be terribly non-linear especially when these glitches become I mean clearly if the glitches is infinitely thin then presumably it causes no effect on the output waveform,

but as this glitch becomes a bigger and bigger portion of the switching period this becomes an issue is this clear. Now, the question is how it is a thermometer DAC respond to changes in the input code. So, let me take the same 4 bit example.

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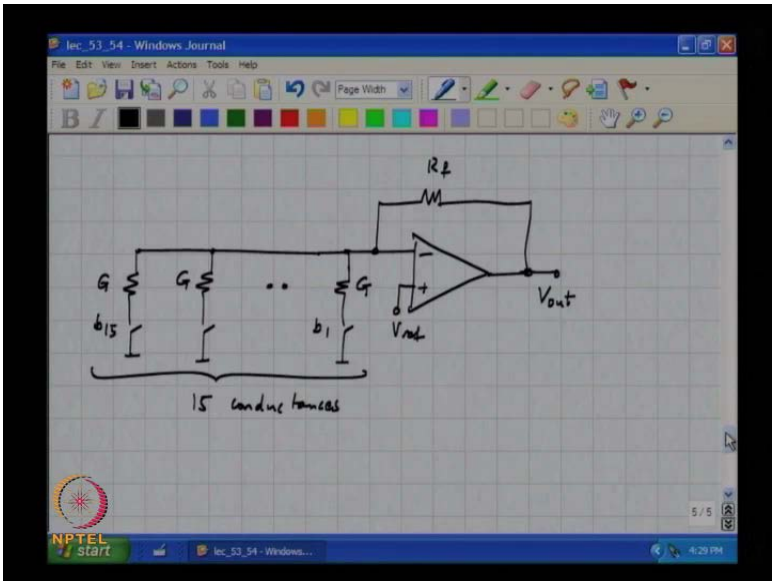

So, this is the thermometer code there are 15 conductance's and whenever the code changes what is happening If you want to change the step by one you are going to add one more element. So, for instance if the code changes by one the output waveform will probably do something like this where as, simply drawn some glitch in the waveform correct that depends on details and timings queue and all this other stuff which we would not get into here.

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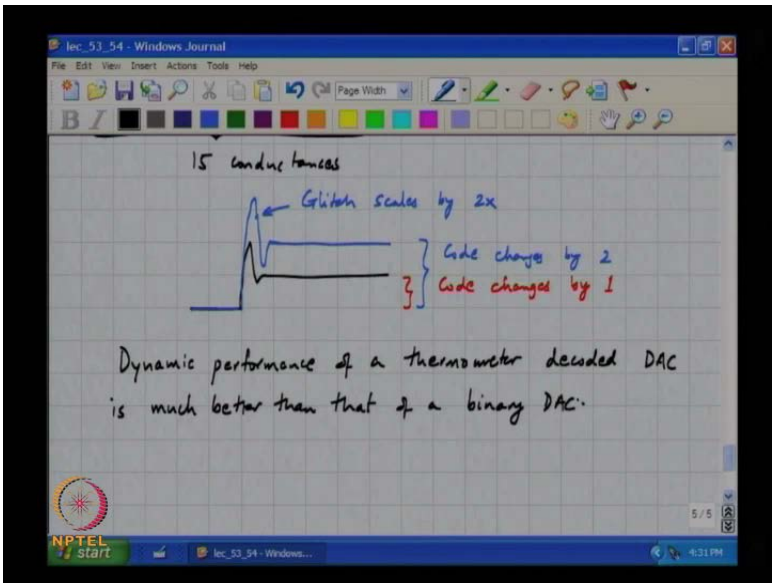

But this is what you will see if the input code changes by 1. Now, if the input code changes by 2 what do you think will happen you will see a height which is double and the glitch will also be twice the height you understand. So, in other words the glitch scales by 2x. So, in general dynamic performance of a thermometer decoded DAC much better than that of a binary DAC which therefore, means that all things being the same you need to you could prefer to increase the levels of segmentation and please note that this discussion had nothing to do with mismatch in the unit elements. So, when the mismatch is also taken into account we see that the sigma DNL also falls down if we increase the area of segmentation.

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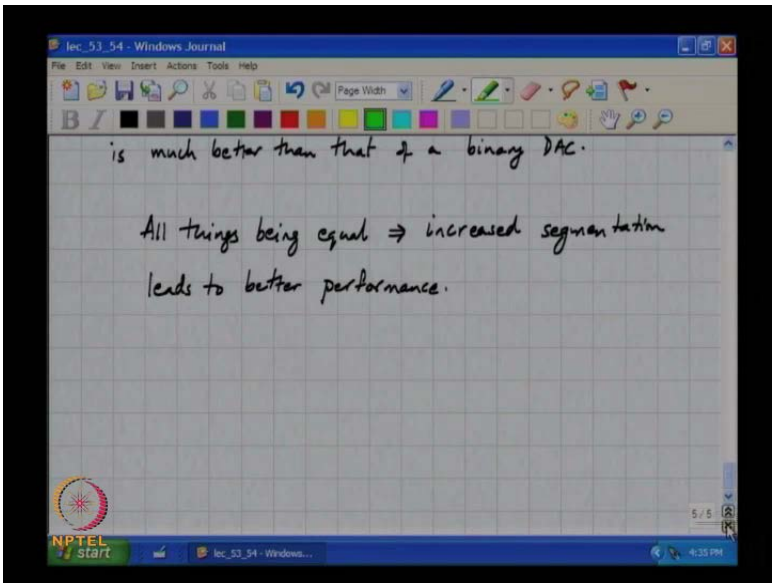

So, all things being equal increased segmentation leads to better performance does make sense. So, in the discussion So, far with respect to binary versus thermometer and levels of segmentation etcetera hold for you know all DAC's I mean in other words this not restricted to any particular kind of DAC as an illustration I just used conductance's in parallel to illustrate the principles.

Now, it is not necessary to have the conductance's in parallel to realize DAC you could also have capacitors in parallel where the quantity of interest is now charge or currents in parallel I mean please note that what the op amp was doing here it is converting it is providing this virtual ground is sensing the current pass through that passes through each of these conductance's and converts them into a voltage.

So, instead of doing this one can say how about I have current sources themselves which I can turn off and on you understand. So, and the output if you have current sources which can be turned off and on depending on a digital code or a digital signal it therefore, means that one can get an output which is a current and if necessary convert this current into voltage where passing this current through a resistor current to voltage conversion at least in on a paper seems like a linear process because you have a current to pass through a resistor and the voltage is I times R if this I depends on a digital code then you are all set is this clear.

Now, this family of DAC's are called current steering DAC's and form a very important class of DAC's used in practice and the reason why there use. So, frequently is that they have very good high speed performance I mean the concentrates matching etcetera will remain the same in the earlier examples the conductance's had to match properly otherwise V times V ref times G would change in the step size.

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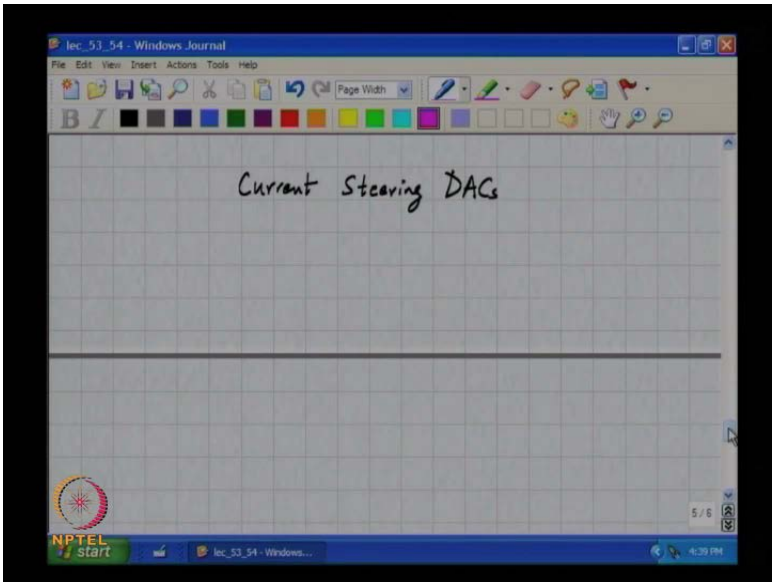

In this case the unit elements are current sources and the current sources much must match properly otherwise they will be DNL and INL just like in the other case; however it turns out that especially at high speeds it becomes very easy to make current steering DAC's work which cannot be said for DAC's like this. The reason being that a you now need a an op amp which runs at very high speed in the resistive case and not only that there is some feedback factor around the op amp which will also reduce the loop gain and therefore, the unity gain band width and to add to all these was you never get conductance's which are just pure conductance's nor do you get the switches which are pure switches which become purely open.

So, what do you will have in practice is that this each of these conductance's will have some distributed capacitances in parallel and each of these switches will have some capacitances between their input and output in other words when we turn off the switch. You will find that these capacitances you know prevent a pure open circuit similarly when you turn on the switch this capacitance which you can small think of a small

capacitances connected throughout the resistor you think of breaking this up into we have many small resistors in series and a capacitances from each of those nodes to ground.

So, the moment you turn the switch on it is not as if these capacitors which are all charged to V ref before if this switch is open all these tiny capacitors along this conductance will have being charged to V ref, now when you suddenly close the switch these capacitors are supposed to this potential supposed to go to ground.

So, the capacitors voltages which were all V ref before must correspondingly go down to some other values depending on their position along this resistor that; obviously, cannot happen instantaneously which means that there is speed limitation to how quickly you can makes such a make the output of the wave or either make the way output waveform switch. On the other hand it turns out that when you have current and you want to steer it one way or the other it can be done with very high speed and therefore, current steering DAC's will become in fact, I will say the defector choice when you want to realize a high speed high resolution DAC.

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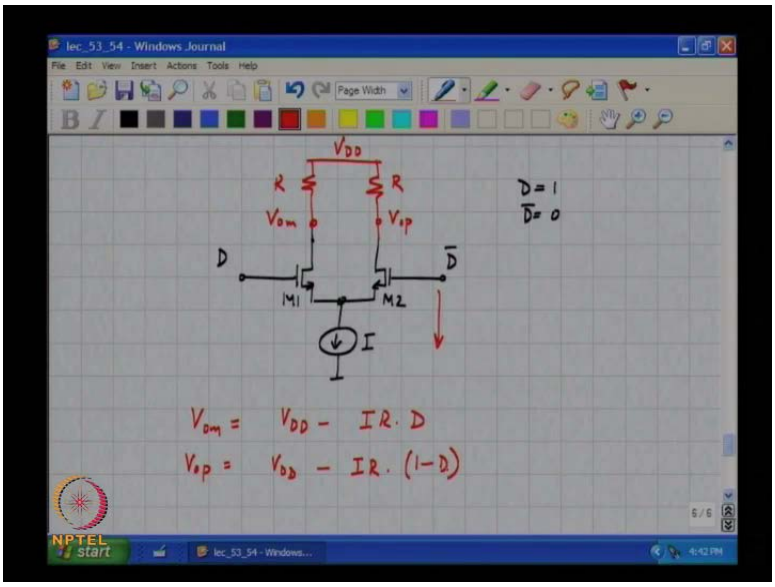

Now, the basic idea is to have a unit element which can be turned on or off and you have seen an example of this already if I draw your attention to the differential pair let us call this D and D bar and this is connected the drains are connected to sufficiently high potential. So, that both transistors M 1 and M 2 are operating in saturation if D bar is 0

and D is 1 when I say 0 and 1 I mean logical zeroes and logical one's then the voltage across this differential pair this is much higher than this which means that all the current flows through M 1. So and no current flows through M 2 when the sign of D is changed the opposite happens, so if you think of this going in to a resistor let us say this is V D D V o m V o p. So, V o m is nothing, but V D D minus I times R times D and V o p is nothing, but V D D minus I R times 1 minus D.

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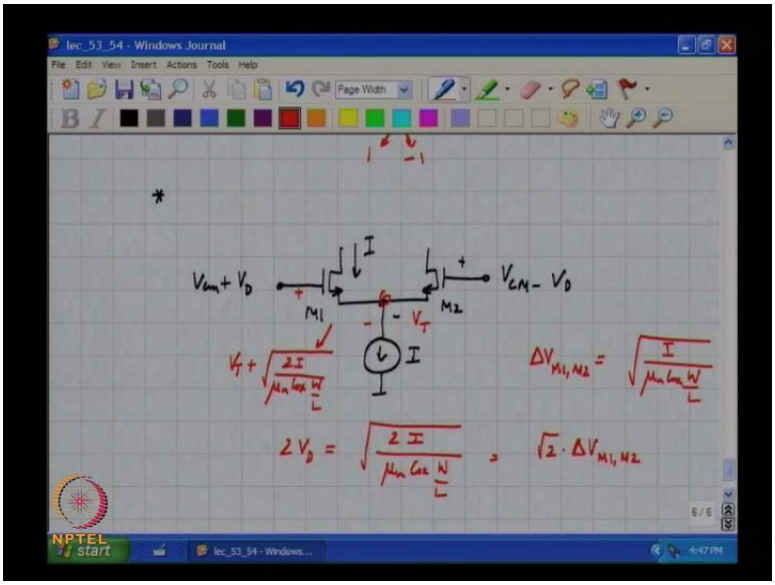

So, the differential output voltage V o p minus V o m is… Pardon.

Student: 2 I R 2 I R D minus 2 I R D minus 2.

2 I R D.

Student: Minus.

Minus.

Student: I R.

I R into…

Student: 2.

2 D minus 1. So, this will take on either values of plus 1 or minus 1 depending on sign of D. So, the output voltage is either plus or minus I times R the reason why this is called a current steering network is because, this tail current is this tail current I is either steered to the left or to the right depending on D sign of D. So, couple of things I would like to bring to your attention one does D have to be a full railed signal in order for asked to be able to steer the tail current completely one side in other words should D b b the D and D bar b connected to 0 in order for this current to move completely to one side.

So, let us see let us call this V c m plus V D V c m minus V D as you go on increasing V D more and more current will flow through M 1 finally, for a critical value of V D all this current will flow through M 1 and no current will flow through M 2 in which case at that time what will be the potential drop here. This potential drop will simply be V t and what will this potential drop be V G s what is V G s is current going flowing through transistor M 1 is I. So, this voltage should be V t plus square root of 2 I by mu n lox W by L. So, the difference between these two therefore, is 2 V D must be equal to root of 2 2 I by mu n Cox W by L if delta V denotes the over drive of M 1 and M 2 when both of them are at the balanced state delta V is simply square root of I by mu n Cox W by L correct.

So, in terms of this V D must be therefore, or 2 V D must be root 2 times over drive the overdrive of M 1 comma M 2. So, this is all the voltage that is needed technically to steer the current completely one way or the other in practice you will have a little more than this just for safety, but in other words there is no real need to go full rail. In fact, you can we you can see later on that having full railed signals actually harmful because it causes to weird things to happen at the source coupled node now given this.

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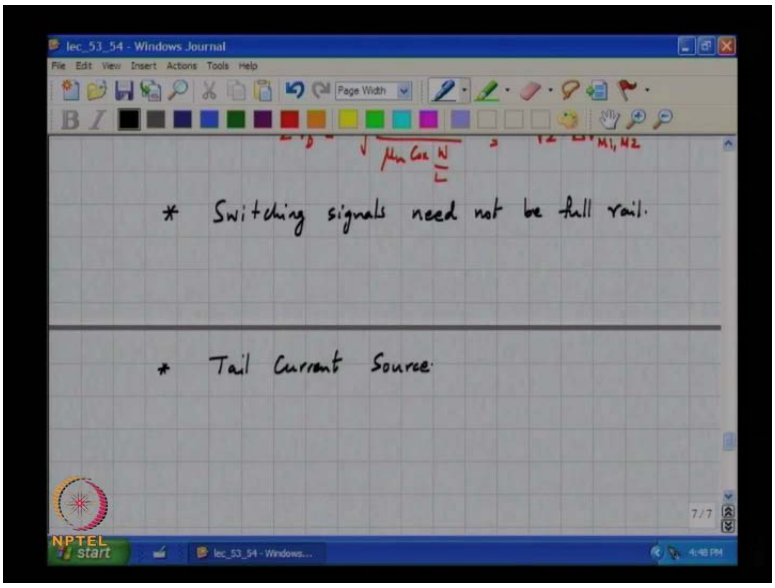

So, the moral of the story is that switching signals need not be full rail now the question is how one would make the tail current source?

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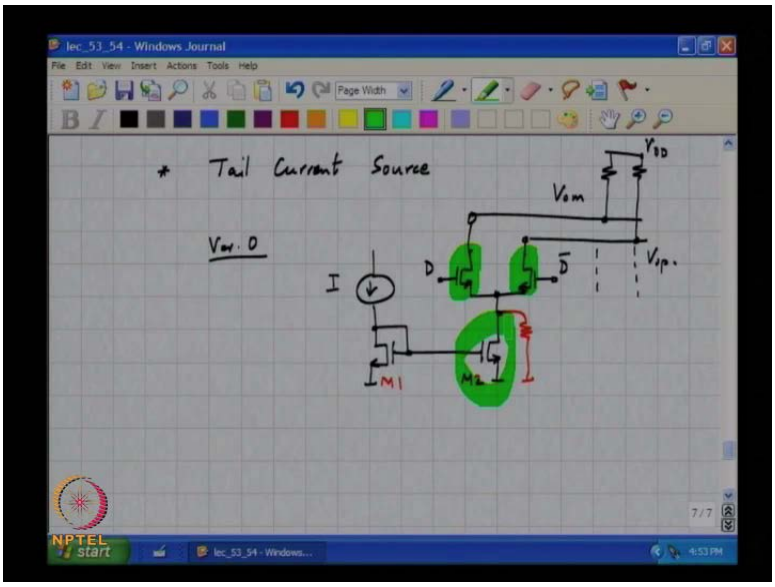

So, how do you make the tail current source by current mirror version 0 would be to say I am going to have a current mirror here and this is my switch or the current switch or the current steering pair which steers current this is I this is nominally supposed to be equal to I what will happen in practice no forget about mismatches there is a systematic problem what current will they will be the will be there here V D s are not the same.

So, there will be some error the error will be proportional to the difference between the drain source voltages of M 1 and M 2 and of course, also the lambda of the transistor correct, but this happens to all current sources if you want to have 10 bit thermometer decoded DAC what should you do.

Student: We put of these the some.

Pardon you put

Student: 10 20 currents sources.

10 24 of the current sources and drive each one of these differential pairs with the output of a thermometer decoder were each line of the thermometer decoder derived from the binary data and some combinational logic does it make sense. So, the change in the current I hat due to finite V D s is something which happens to all current sources. So, as far as the DAC is concerned it just shows up as a gain error more importantly if there is finite g d s. So, that the incremental equivalent is something like this is there a more serious problem.

Student: Pardon.

Please note that these outputs and let us assume that we are doing in a thermometer DAC like this. We have many pairs in parallel and the output is developed by across load resistors which are connected like this.

Student: Sir, D and D bar are the switches.

Correct.

Student: That means they are from linear region and they are from that means

Ok

Student: So, whatever I mean depending on whether D is on or D bar is on the voltage across that rail current source will change

And why is that.

Student: That is because no when D is on the positive terminal voltage will comes straight away because it is in the linear region

This is V o p as call this V o m and let us call this V o p

Student: When D is 5 you will have D o m

Ok.

Student: And if D bar is 1 you will have D o p

Ok

Student: And differences of current sources depending on their individual states you will have different.

That is right. So, the observation is that if I mean if D and D bar are logical levels which were the voltages are so high to cause these transistors the switch transistors to go and the triode region then we V o p and V o m directly come across the tail current source which means that those current sources which are connected to V o p correct will be slightly different from those current sources which are connected to V o m this is clear.

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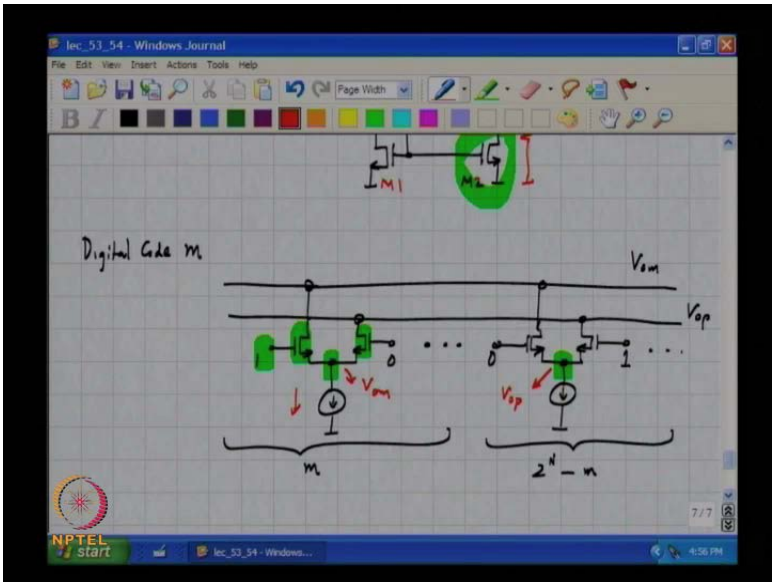

Let us say the digital code is m which means that out of possible 2 to the N current sources m will be having their outputs connected to… So, let us say this is logical 1 the

logical 0 and then you have m sources like this and 2 to the N minus m sources where this is connected to 0 this is connected to 1 if these devices are in triode which is what will happen when these gate potentials are pushed to high and low or if the supply voltage is not sufficiently large then clearly this potential will be What V o m correct because this switch is on the other hand this potential will be V o p.

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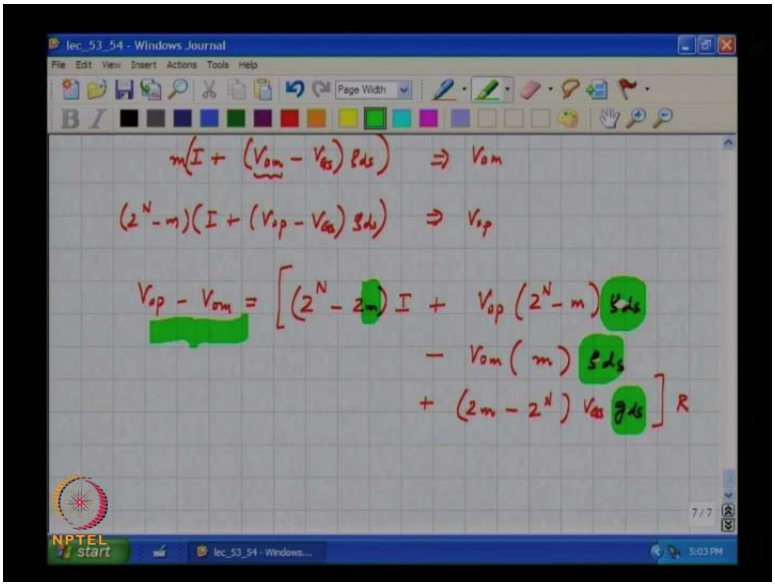

So, this actual current it will be m times I plus V o m by actually it is not simply V o m by add it will be V o m minus some V G S I mean if you assume that all these are coming from a master current source it is actually V o m minus V G S divided by or multiplied by g d s correct. So, V o m is the same as I mean V G S you have I, but the key point is to note that you have V o m here and similarly what is the other current 2 to the N minus m times I plus V o p minus V G S times g d s and therefore, the difference in the output voltage this is V o m this is V o p.

So, V o p minus V o m is therefore, equal to 2 to the N by minus m times sorry 2 to the N minus 2m times I plus V o p minus 2 to the N minus m minus g d s minus V o p times m times g d s plus m times v g s times g d s minus 2 to the N minus m times or I just club these two terms it will be m minus 2 to the N so the m goes away it does not go away it is 2m minus 2 to the N times V G S times g d s. This is right. It seems into the output resistances R.

So, what do you I mean without getting into major competition what can you say about this relationship what do you want finally if G g s is 0 which means the output impedance for every current source is infinite how is V o p minus V o m related to m which is it is basically I mean if you forget about the offset 2 to the N times I. This is a linear relationship in m. I mean here m must go from when 0 it goes from 0 2 to the N; obviously, there must be an offset because the DC values is always positive.

The m goes if m end from minus 5 and I mean whatever 2 the N minus 1 plus 2 to the N minus 1 then you can expect the average to be 0 that 2 to the N times capital I is an offset we would not worry about it what is important is to notice that if g d s was 0 V o p minus V o m is a linear function of m the moment there is finite output impedance what do you think will happen

This whole relationship is no longer linear and not only that it turns out that this g d s will also depend on V o p and V o m. So, this is first of all vastly simplified and make things worse g d is also dependent on V o p and V o m. So, basically if the current source start depending on the output voltage it will mean I mean through which will happen through that finite g d s it means that the DAC will become nonlinear.

In the next class we will do a more careful computation of the DNL and INL that one can expect when you have finite output impedance one other point that I wish to make is that it does not have to these transistors do not have to be in the triode region in for that to happen if these transistors are in saturation also there will be a component of that voltage which will it be dependent on I hope this is clear to you.

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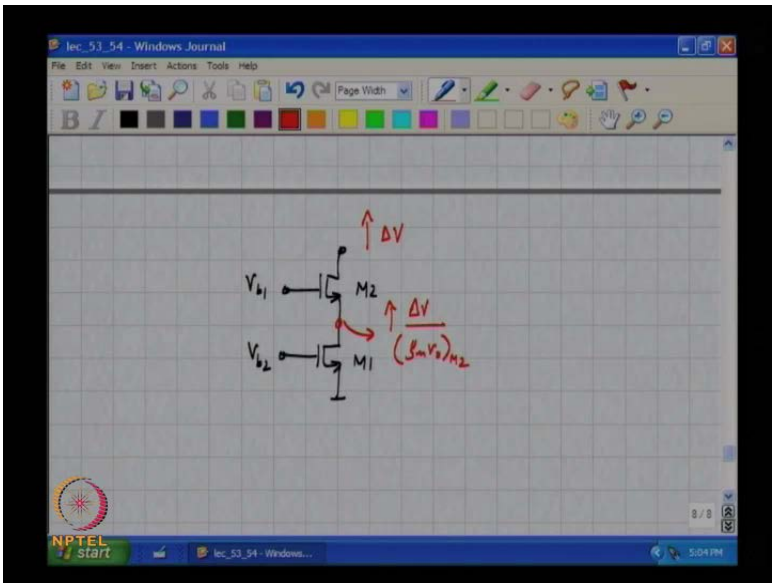

So, if let us say this is V b 1 V b 2 even if M 2 and M 1 are both in saturation if this changes by delta V or if this is yanked up by delta V what happens to this node this will go up approximately by delta V by g m r o of which resistor of m. So, e n is the transistor the switch transistors are in the saturation region that tail node will have components which are depend on V o p and V o m. So, you still you get only a respite of factor of g m times r o. So, in the next class we will get into this in more detail.