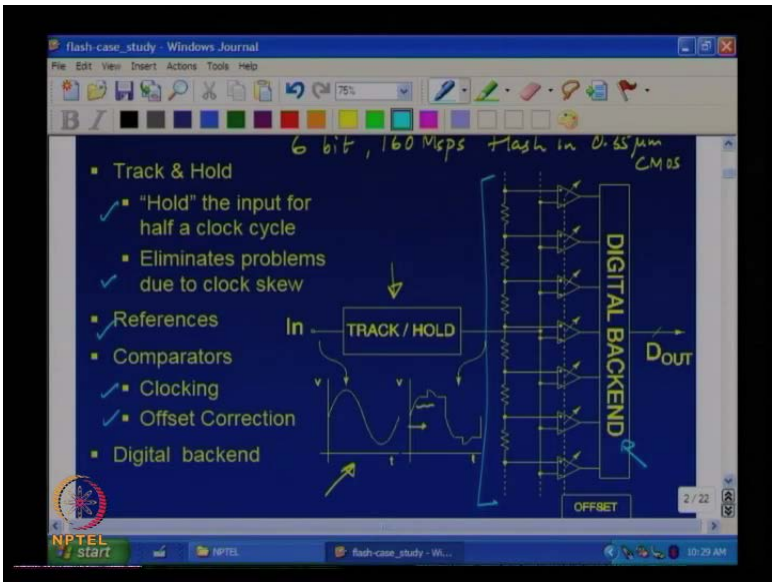
VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 48
Flash ADC Case Study

So, this is VLSI Data Conversion Circuits, lecture 48.

(Refer Slide Time: 00:15)



In this lecture I will give you a quick case study of 6 bit 160 MSPS flash ADC in 0.35 micron C MOS process, we did this in our group about will be 5 years ago, I may 6 years ago. It incorporates of whole lot of ideas that we have discussed in this course, and that is why I thought it is relevant to show you a practical design, which as all these ideas in place I will also introduce couple of new ideas, which we were not discussed in this course. But, they will be a motivation and the idea will be quite self explanatory, much of this is stuff that you already knows I will kind of base through the slides quickly.

As you know a flash A to D converter consist of a track and hold, that job of the track and hold is to take a continuous time input and generate a waveform, which tracks for some time, and holds for some other time. And the some of the track time plus the hold time is one full clock period, and as I mentioned earlier typically you make both of them, equal. So, you hold the output of the track and hold it is actual held for half a clock cycle, the motivation to have

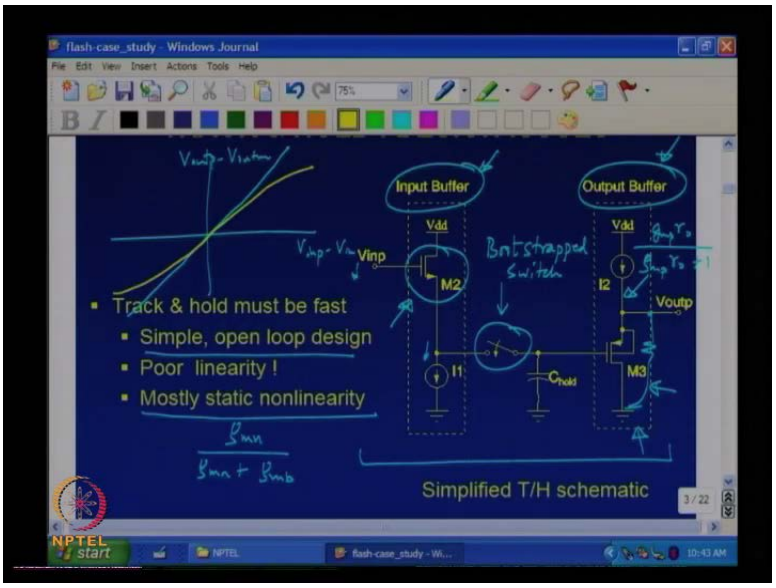
a track and hold in the first place, again is to eliminate problems due to clocks skew, which are bound to occur.

Because, this is distributed in space and routing a clock to these comparators which are separated in space, means that there will a time lag between. When the clock reaches comparator one through comparator n, which will then mean, that there will be a hit in the high frequency performance, because all the comparators are not sampling the same input. Now, so you understand this and you understand this, you also need to have references which go to the each of these comparators, and as we discussed earlier, the reference generation is easily done through a resistor string, which goes between full scale in ground.

So, the taps of the resistor ladder will give you the references to the various comparators, the comparators themselves are not really continuous time comparators, they are clocked and they will also incorporate offset correction. Simply because, the latches are called dynamic offset, and the preamps which are there to fix the dynamic offset problem of the latch right, have their own offsets which need to be estimated and corrected. And there is a digital backend, which includes bubble correction thermometer to binary conversion and so on.

So, this is the generic block diagram of a flash converter, there is some kind of offset correction engine, which may either be distributed in every comparator, which is what the very first version we discussed was. So, we have an auto0 phase every clock cycle, or you can do something where the offset is corrected, the auto zero is done once in a very long while, that can be done either in the port ground or in the background. And either case you need to have some kind of engine, which tells the comparators what to do.

(Refer Slide Time: 04:39)



Now, let us look at some design issues in a flash converter, the track and hold in a simplest form must have a buffer at the input, and why is that...

Student: ((Refer Time: 05:06))

So, the previous circuit block that drives the flash converter should see high impedance, you cannot I mean, alternately one could say I am going to simply connect the switch. And the capacitor to the to the previous block directly, in which case the designer of that block will go crazy because the switching load, is very difficult for him to dry. And then it may turn out that, because of this interface there is a lot of distortion, because it is not been carefully design.

So, it is mandatory that the flash itself present a very high impedance to the previous block that is driving, please note that there is a difference between having the switching capacitive load, and pure capacitive load. A pure capacitive load is very easy to drive, whereas a switching capacitor load actually draws spikes of current every time use switch, which means that the previous circuit must be able to provide those spikes of current.

Those impulses of current which means that, that circuit must have a very low output impedance, so it is common to have an input buffer, why do you need the output buffer, why cannot a simply connect this to the comparator array.

Student: ((Refer Time: 06:49))

So, the voltage which is been held on the capacitor must remain held, now if I connect a whole bunches preamps to this, even though there inputs are capacitive, depending on what they are doing there will be charge sharing and it becomes very messy. And basically modifies the very voltage that you are trying to digitize, so the output buffer is needed to drive the comparator array. And of course, this whole circuit is suppose to be linear, to the extent of the linearity of the flash converter.

So, if you want things to fairly linear, the standard approaches is to use negative feedback, you say if I want a very linear amplifier, the first thing I would do is say this is my opamp and then, let me work with it. Where if I assume a very good opamp I will get very good linearity, unfortunately the movement I use an opamp and negative feedback, it means that you take a hit with respect to bandwidth. Because, all this linearity is coming with only with loop gain, loop gain means that there are several stages of gain.

If you have several stages of gain, it means that the whole process becomes slow and a flash converter typically operates at the cutting edge of that process. So, if you are want a very very fast track and hold, which is a what you would need if you are designing a flash converter, the usual op amp based sample and hold type solutions, simply go out the door, because you cannot make them sufficiently fast. Which means that, you are stuck with simple circuits for the input and output buffers, which are basically opened.

So, we have the simplest, so I mean input buffer and output buffer you can think of are common range stages and therefore, this shows an example of a common drain input amplifier, which behaves like the buffer. And the output buffer is also a common drain amplifier, but it must be...

Student: P MOS

A P MOS type, why P MOS why cannot it be N MOS?

Student: ((Refer Time: 09:45))

Why do you think I cannot make this N MOS?

Student: Already voltage would be much much

Please also realize that, this is only the 1 half of a fully differences structure, there is two identical all the diagrams will be shown single ended, in reality it means that there are there is one more clone of this, which is processing the V and M. Now, the common mode voltage here will be the input minus V t minus the over drive of the N MOS transistor. If this was an N MOS design the output common mode of the sample and hold will be one more threshold lower, at a one more gate source voltage lower, which means that if you want to make all the transistors work in the saturation region.

You will find that the amount of signal swing you can have is very very small, you understand, so now what happens you go down 1 V G S and you go up 1 V G S, so you have a fair amount of signal swing. Now, every time we use simple open loop designs, you are stuck with limited linearity, in this case where do you think the nonlinearities are coming, I mean what is the origin of the nonlinearities here.

Student: The switch

The switch is one source of nonlinearity, how do you think that can be fixed

Student: From by making the gate back the input signal we have

So, this is the bootstraps switch, which we have discussed at great lengths, where we make the gate voltage track the source voltage. So, that the over drive is constant and independent of the signal, what else are the sources of nonlinearity.

Student: Source follower g in the

See one important effect is that most of the C MOS technologies, one usually finds that the N MOS transistor does not have it is body terminal available to the design, the body terminals of all N MOS transistors are by default connected to the substrate. Because, these only a one well for all the, one common well for all the N MOS transistors, whereas for a P MOS transistors you have the freedom of being able to connect it is source to be bulk, which means that there will be something called the...

Student: Body effect

The body effect, where the threshold is modulated depending on the source potential. So, that turns out to be a non-linear effect it will cause, the body effect will cause two problems, what you think what are the two problems.

Student: ((Refer Time: 13:11))

What happens to the incremental gain from here to here

Student: ((Refer Time: 13:16))

So, the there two problems with the body effect, the gain of the first flopper will become g m by g m n by g m n plus g m b, and not only that there will be this is a non-linear phenomenon. So, there will be some nonlinearity associated with this gain, the P MOS source follower fortunately does not have that problem. However, there is still some residual nonlinearity, because the output impedance of the P MOS transistor or the N MOS transistor for that matter, is also a function of the source drain voltage. Which means that, if the source drain, I mean if the output impedance of this P MOS transistor is not a constant with respect to the source drain voltage.

It means that ideally this gain must be g m p into r o divided by g m p into r o plus 1, now if this r o keeps varying with the output voltage, it means that there is the gain keeps changing with the output level, which means that there is non-linearity. So, that to summarize each of these buffer is very very fast, which means or this is a fastest you can do in a process which means that, at the end of the hold phase, the output has settled quite nicely.

Unfortunately there is error, because non-linearity and since this nonlinearity does not depend on the speed, because you have settled comfortably this nonlinearity is static. In other words, whether you run this sample and hold at 1 Megahertz or 100 Megahertz, if I plot a graph with the output deferential output p out p minus V out m, and deferential input V in p minus V in m, you will get a characteristics which is the same. And what kind of characteristic will you get, ideally what would you like to get, ideally you would like to get a straight line with a slope of 1, what is happening in practice.

Student: Different

It will be different from the ideal, in what ways

Student: ((Refer Time: 16:14))

The gain will be smaller than 1, sure what else

Student: ((Refer Time: 16:20))

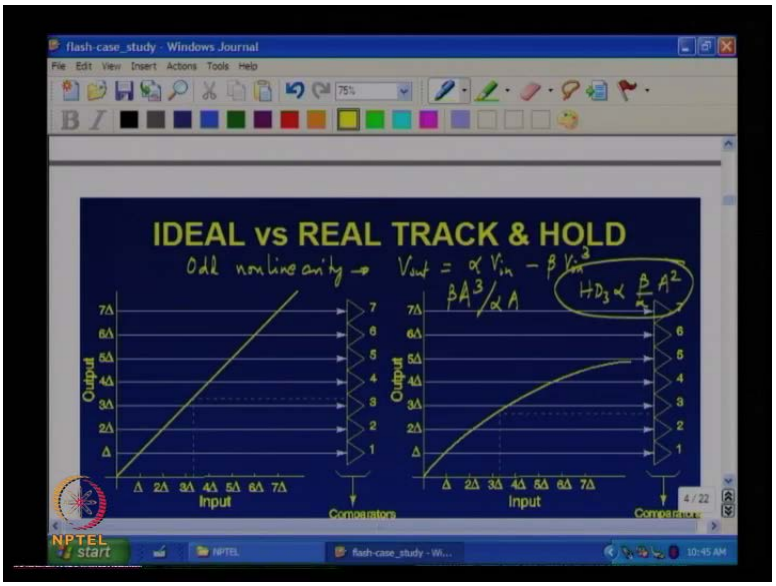
It will be non-linear and what kind of nonlinearity can we expect, if it is a differential system what kind of nonlinearity can you...

Student: Odd nonlinearity

You can only expect odd nonlinearity, so you will get you can expect to see something like this, now the fact that there is nonlinearity means that, if you go on increasing the signal swing what will happen to the distortion.

Student: ((Refer Time: 17:06))

(Refer Slide Time: 17:08)



So, in nonlinearity is odd, let us say it means that

Student: ((Refer Time: 17:30))

What is an odd function, ((Refer Time: 17:50)) an odd function is one where f of minus x is minus f of f of x, so you can of the output V out deferential output, as being are the form some alpha times V in. Where V in is the deferential input minus beta times V in cube and all

other odd powers, and as an approximation you only consider the cube term. So, the distortion is proportional to

Student: V input time constant

Of course, I mean as you increase the input amplitude the harmonics will increase, what harmonics will you see

Student: Odd

You will see only odd harmonics, and can you comment on the strength of the odd harmonic tone, in relation to the fundamental. We have, let say you put in a sin wave of amplitude A, that we discuss this, when we are discussing the switches in the linearize switches way back.

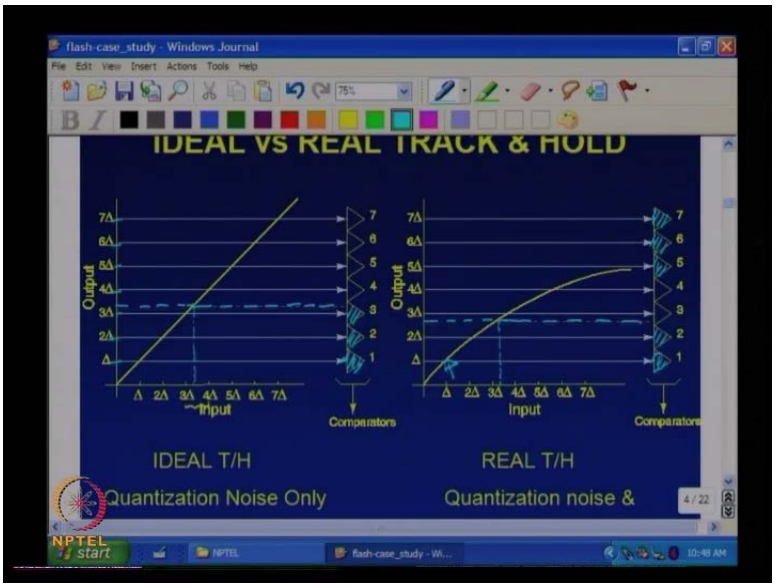
Student: ((Refer Time: 19:19))

The odd harmonic term will be proportional to A cube, the fundamental term it may proportional to beta times A cube, the fundamental will be proportional to

Student: Alpha times

Alpha times A, so the H D 3 of the third harmonic distortion will be proportional to beta by alpha times A square, there will be some constant which you can work out, but the key point is to observe that, the distortion is proportional to A square. So, it is the slit increase an amplitude will cause, a significant increase in distortion, so now if the track and hold distorts, let see what happens to the flash converter, in an ideal flash what happens, let us consider 3 bit flash converter.

(Refer Slide Time: 20:15)



If the input lies between say 3 and 4 delta as I shown here, what must happen, let us say the input lies between 3 and 4 delta, where delta is the LSB, then what happens which of the comparators will fire the output of the flash....

Student: ((Refer Time: 20:47))

Is like this, this output shown as the horizontal dotted line blue is compared against these references, and which of the comparators will fire 1, 2 and 3 will have an output of 1, these rather 4 will have an output of 0. And you can see that you are estimating the input to within 1 LSB, now if the if the characteristic of the track and hold is non-linear I shown here, if I put in an input between 3, 4 delta, what happens the output of the track and hold is this.

And what happens only 1 and 2 will fire and all these will not which means that, there is first of all you making an error and not only that the error keeps increasing with...

Student: Input

Increasing input amplitude and you will see that in this particular grossly exaggerated case 6 and 7 will never, in fact even 5 will never fire at all. So, since the magnitude of the error depends on the input amplitude, it means that this is not simply a static error, this will lead to distortion. So, apart from quantization noise your will also see distortion, so how do you think you can handle this problem.

Student: ((Refer Time: 22:49))

You have an amplifier if you drive it with a large swing, we get a lot of distortion, so what is the common sense way of

Student: Reduces

May be, common thing do is say A, A either try and build a better amplifier which is more linear, and in this particular case that is not possible to do simply because...

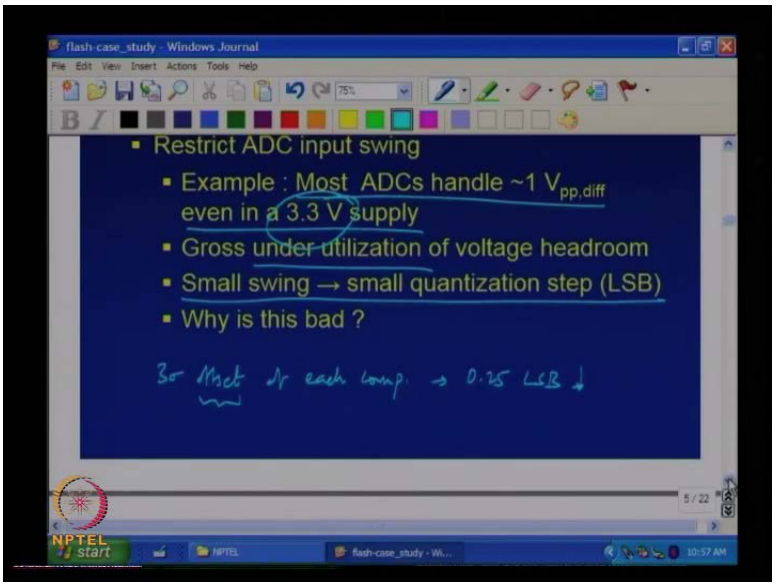
Student: It cannot give feedback

To increase the linearity at typically used negative feedback, I cannot use negative feedback, because negative feedback is only useful, when the loop gain is high, increasing the loop gain means that...

Student: ((Refer Time: 23:36))

Any successful stages which makes the whole process slow, so if I cannot increase the linearity then a common sense we have doing this, would be to say hey I am going to restrict the signal swing. Because, I know that distortion is proportion to A square, so if I reduce the signal swing or if I make the full scale of my flash converter low, then distortion will be small.

(Refer Slide Time: 24:12)



So, that is something worth, which is the commonly used approach again please note that this work is about 6 years old and therefore, all things are in 3.3 volt supplies, today one would be taking about 1.8, 1.2 volt supplies in correspondingly fast process. Anyway, so at that time most of the converter who are running off of 3.3 volt supplies, which meant that due to signal due to distortion of the track and hold, a common thing done was to restrict the signal swing.

And as a designer you would design a track and hold, you would put in some voltage should measure the distortion, if the distortion is too high I will reduce my signal swing, in order to bring the distortion, level it into speck. And then, that would then define the full scale of my A to D converter, the distortion will be worst when the signal is the largest, the larger signal by definition the full scale of the converter.

So, rather than define a full scale and then, say I am going to design a track and hold to a accommodate this full scale, I go the other way, I know that this is the best track and hold I can build. Now, if I want this level of distortion, then I am going to restrict my signal swing, so that it gives me this level of distortion in the worst case, this will then form my ADC full scale.

If this forms my ADC full scale, then I can be assured that the distortion is within speck, so you would find that even with the 3.3 volt supply, most converters would restrict their swing to about 1 volt peak to peak differential. And please note that in a 3.3 volt supply, what is the in principle maximum peak to peak differential swing you can get.

Student: ((Refer Time: 26:39))

So, in a 3.3 volt supply, in principle one should be able to get a 6.6 volt peak to peak differential swing, must be able to accommodate that in principle. Of course, there are lot of difference between in principles and in practice one thing that, it is a way directly into the 3.3 volt supply is that, you are often expected to work with plus minus 10 percent supplies. So, which means that your supply is down to 3 volts and then, you lose headroom here there and everywhere.

And one would say may be about 4 volts speak to speak differential is probably practical limit for operation, after accounting for headrooms and so on. But, you see that in spite of a practical limit of say about 4 or 3 and half volts, the actual swing limits chosen for many of these converter, which state of the art converters is only one volt peak to peak differential.

And the primary reason for is that, it becomes very difficult to design a track and hold, which can handle about 3 and half volts peak to peak differential with a linearity, which is good enough for a 6 bit performance.

Now, clearly in other words, we are not optimally utilizing the available voltage headroom, and one thing that you should always be aware of is that, if you underutilize the headroom you are always doing a power inefficient job. And why is that, in this particular case if the full scale is small what does it mean?

Student: ((Refer Time: 28:56))

The key point is the LSB size is small, the peak SNR is still the same, because you are taking small full scale you dividing it up into 64 steps, and the LSB is small, but the peak voltage, in relation to the LSB still remains the same. So, if the thresholds were ideal, there is no errors in the threshold, whether you have a full scale of 1 volt or whether you have a full scale of 10 volts the peak theoretical SQNR remains the same and is independent of the full scale voltage.

So, the only thing that happens as far as design is concerned, is that a small full scale voltage means, that you have a small quantization step. And the question is why is this bad, what you think this is a bad idea.

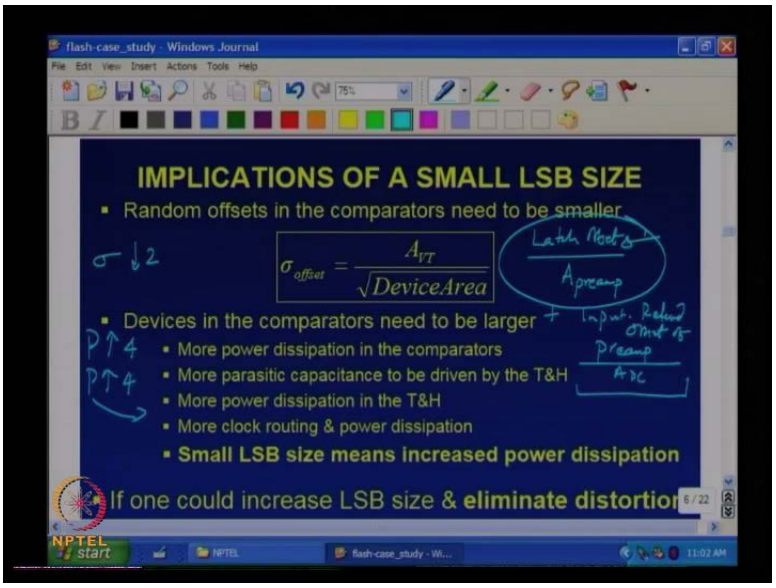
Student: ((Refer Time: 30:09))

[FL]

Student: Sir, offset requires you can most full

So, if the quantization step becomes smaller, you now need to speck the offset of each comparators slice, in a much tighter manner, as we just discuss in the last class. You typical try and restrict 3 sigma offset for instance, of each comparator to be say quarter LSB, now if the LSB size goes down, it means that the sigma of the offset in each slice must also go down, does it make sense.

(Refer Slide Time: 31:11)



Now, how can you how do you relate offset to power dissipation, what is the offset, offset is finally, dependent on device mismatch and preamp gain. So, input referred offset of each slice is latch offset divided by A preamp, please note A preamp cannot be very large, you are trying to run a flash converter at very high speed, your finite amount of time we have only so much dynamic gain.

So, it is not like I will say, let me go and increase A preamp by fact of 10, that is not possible, plus input referred offset of the preamp itself divided by the D C gain of the preamp. Please note that, there is a distinction between the D C gain of the preamp and the dynamic gain, the dynamic gain is always going to be smaller or larger than the D C gain, smaller than the D C gain.

So, you really one does not have to worry about the this part, you are stack with the latch offset divided by the preamp A, so if you have to reduce the offset of the preamp, what must one do.

Student: ((Refer Time: 32:45))

So, what one would do would be to, if I want to reduce the sigma offset by factor of 2 what should I do?

Student: It I will reduce latch

I have to reduce latch offset by the sigma the latch offset also by a factor of 2, which means that I have to increase the area by a factor of 4, please note that the sigma goes as 1 over square root device area. How would I increase area by a factor of 4, in principle it is like taking 4 identical latches and putting them in parallel, now if I have 4 identical latches and put them in parallel, the capacitor load offered by these 4 latches will be 4 time larger.

So, if I want the same dynamic gain, what should happen to the preamp

Student: ((Refer Time: 33:37))

I have to increase the size of the preamp also by a factor of 4, in other words I take 4 identical comparator slices and put them in parallel, then that will keep the preamp gain the same. It will reduce the sigma of the latch offset by a factor of 4, and it will make the area of the entire comparator slice 4 times larger, it will make the power dissipation of the slice 4 times larger. So, in other words reducing sigma by a factor of 2 means power goes up by a factor of 4.

Now, if the track and hold was just able to drive a comparator of size 1 multiplied by 63 to some require degree of precision, if you now increase the size of the comparator by factor of 4, what do you can you say about the power dissipation and the track and hold, you understand the question. I had initially a comparator array, where each comparator slice had a sigma offset some sigma of random offset. Now, the track and hold must be design to be able to drive this comparator array, but we found that because the LSB size is too small.

I need to reduce the sigma of the offset in the comparator array to that end I increased or scaled up the comparators by a factor of 4, there by resulting in a sigma offset which is lower by a factor of 2. Now, it is essentially like having 63 times 4 comparators, that have to driven by the track and hold, now what do you think I must do with the track and hold now, in order to make it drive, what is the easiest solution that you can think of which will definitely work.

Student: Again this 4 times

So, if I have track and hold which is 4 times larger, which is can be easily done by simply copying and pasting the same comparator multiple times, the power dissipation in the track and hold also goes up by a factor of 4. Now, you have a lot more comparators, and clocks have to go and drive all these comparators. So, what do you think will happen, who is going

to drive these comparators, you need to have a clock generator as I said earlier, you are not going to get all these mired clocks.

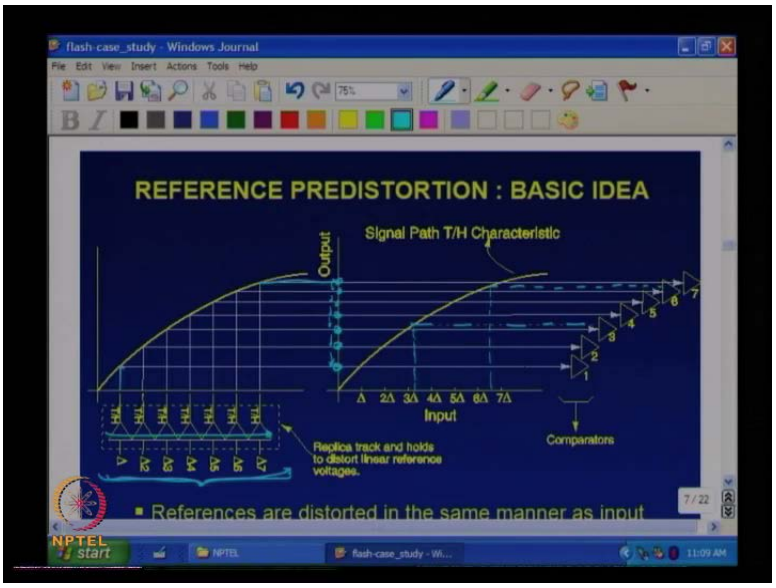
That you need to drive the flash from outer space, you are only going to get one master clock, from which you need to generate all these non over lapping clocks. And once you generates these clocks you have a clock drivers which go, and drive these large capacitive loads which are presented, because of the large number of comparators and the routing. So, now if you have a comparator which is 4 times larger, presumably when you put 64 of them, the whole array now becomes 64 times larger, which means that the amount of power needed to drive these comparators, also goes up by a factor of 4.

Probably more than that simply because, the routing also becomes much larger, but in principle at least you can say that it is 4 times more. So, what is the bottom line, a smaller LSB size which is stemming from the fact that, you have a small full scale range for the A to D which is stemming from the fact that... You cannot design a track and hold with a sufficiently small distortion, which is coming from the fact that, the track and hold cannot be very linear.

Because, you cannot use strong negative feedback is basically responsible for not only increase area of the entire converter, but also increased power dissipation. I can now turn this argument upside down and say, if I was somehow able to double the swing, from say 1 volt peak to peak to 2 volts peak to peak differential, then the LSB size goes up by a factor of 2. Which means that, my comparator offset standard deviation can go up by a factor of 2, which means that my comparator can become 4 time smaller which means that power dissipation can go down by a factor of 4.

So, things will become stronger, faster and smaller if the LSB size is made larger, the only thing that preventing us from making the LSB size larger is this done distortion of the track and hold. So, if we one could somehow increase the LSB size, and eliminate distortion, then one could reduce power dissipation significantly is the motivation clear, you cannot solve the problem unless what the problem is, and we now know what the problems.

(Refer Slide Time: 40:00)



So, one way of eliminating distortion is to design a better track and hold using negative feedback, but that is how to the question in this particular case, because we cannot effort the time. Another way of eliminating distortion is to understand the following principle, which is earlier why we were getting distortion with a non-linear track and hold was that. For instance if the input is between 3 and 4 delta, only the first two comparators are fire, if we ensure that the first three comparators are fire for all inputs between 3 and 4 delta, then we are doing ok. In other words in general if the input is between n delta and n plus 1 delta, if we make sure that the first n comparators fire, then in principle assuring distortion free operation. Of course, one way of doing that is to make this as straight line, which is not possible another way of doing that is to make the spacing of these references non uniform.

So, here what we have done is change the spacing of these references precisely in the same manner, that the track and hold distorts. And this way what happens if the input is between 3 and 4 LSB, please note that these references are derived by, how do you think you will derive by these non uniformly space references.

Student: ((Refer Time: 41:49))

You pass these uniform references through in principle, identical track and holds to the master track and hold which is processing the input. And the outputs of each of these track and holds will be distorted by that precise amount, by which the input itself is being distorted by the input track and hold. These levels have to be, I mean is it clear that these levels have to

be distorted in order for to get distortion free operation from the A to D convertor, the next question is how do we generate these levels.

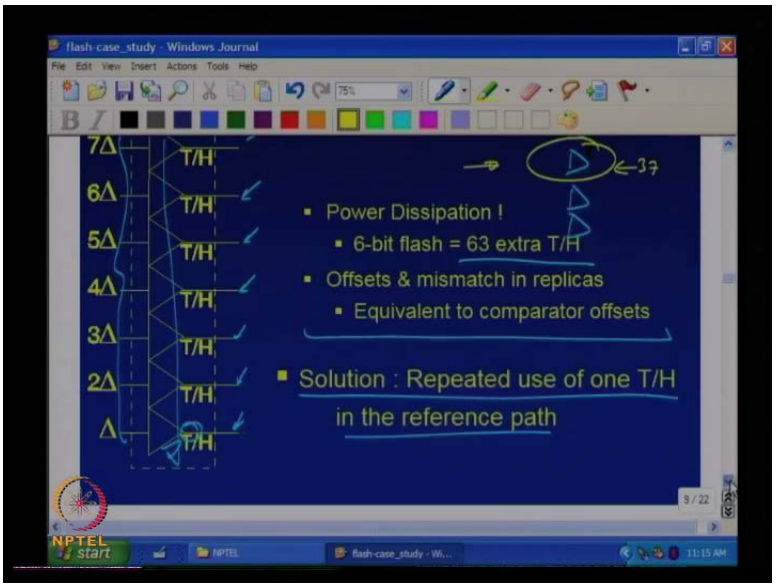
So, one way of doing that is to take the linear references, which are derived from the ladder, and pass them through array of track and holds, which are identical to the one that the input is being pass through. We know that on a I C at least you can build you know any number of track and holds, which are identical to each other, they all may be bad,, but there all just bad is each other.

So, this will ensure that the reference is pre-distorted by precisely the required amount, now you see that if the input is between 6 delta and 7 delta, because the references pre-distorted the first 6 comparators will fire and so on. So, this way you can use a non-linear track and hold and still get distortion free operation without any power penalty. Because, you are doing anything to the inherent track and hold, all we are doing is tweaking the references lightly, does it make sense.

(Refer Slide Time: 44:08)

And for this skeptics, who do not believe this I will would not work, here is stimulation results from transistor levels schematics with a non-linear track and hold, you can see that there is third harmonic. And the SNDR for a 6 bit convert is only about 30 d B, this is for the particular track and hold, that was used in the work later. The movement you go and pre-distort the references you see that, the distortion goes away completely and you get SNDR, which is what you would expect for a ideal 6 bit design, about 37 and half bit.

(Refer Slide Time: 45:06)



Now, what are the problems with the reference pre-distortion, the idea behind pre-distortion is to use linear references, and pass them through array of track and holds. So, that these output references, against which the comparators will compare their inputs are pre-distorted in precisely the right manner. Of course, if you want to have a 6 bit converter, you need to have 63 different track and holds, which means that the power dissipation will become very large.

Earlier had an one track and hold now you have one track and hold plus the 63 extra, in other problem is that all these track and holds will be nominally identical, but they will also have offsets in themselves. So, this means that an offset in the reference is the same as the offset in the comparator, because the comparator is comparing input minus reference. The reference is offset from its value by some random voltage, it is equivalent to having comparator offset. This therefore, does not seem like a practical idea I had to have 63 different comparators we generate, these 63 different values which is what would be required in a 6 bit flash design.

So, the solution to this is, what you think you could do to fix the problem, what do you think you can do, avoid this problem of 63 extra track and holds, and the mismatches between them...

Student: Because, these references are not outstanding signals they are not changing

Yes

Student: You can distort them and then, stored it some capacitors and

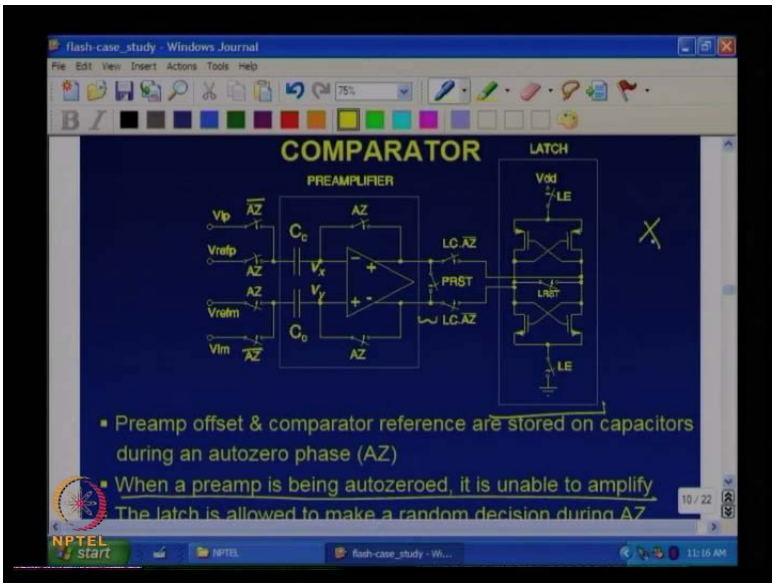
So, that in a comparators slice anyway, the references are stored on those auto zero capacitors, and if this auto zero is run in the background, then only one comparator is being auto zeroed at one time. And at any instant of time you are removing 1 comparator, and auto zeroing it during which phase you are also storing the reference. So, in other words, from reference generator you only need one particular reference at any instant in time, is this clear yes, no.

So, you have this array of comparators at any instant of time, let us say you are only auto zeroing, at any instant of time you are only auto zeroing one of them, during the auto zero, that particular comparators also storing the reference. So, in other words in principle the reference generator needs to generate only one reference at every point in time, you do not need all the references all the time.

So, in other words if you have the 37 comparator auto zeroing, the only reference needed from a reference generator, which is normally a resistor ladder is that 37 tap, you do not need excess to all the other taps, which means that if only one reference is needed you can use only one track and hold. And as you keep auto0ing various comparators, the track and hold can remain the same, the input to the track and hold keeps changing.

This way you have only one extra track and hold, and there is no mismatch between, this mismatch problem also goes away, because you are using the same track and hold all the time.

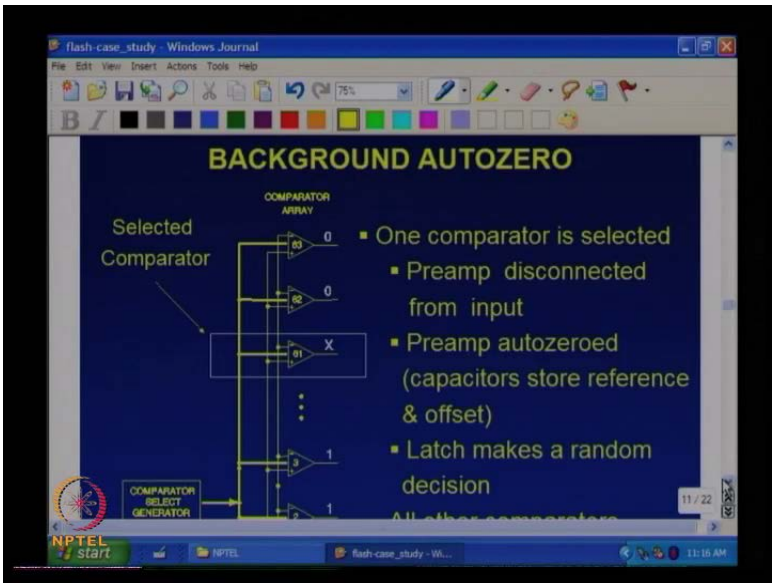
(Refer Slide Time: 49:43)



This is the rest of it is well known familiar territory, this is the preamplifier and the latch again these are the auto zero switches, so this is auto zero bar, this is also auto zero bar. So, during the auto zero period, the feedback loop around the preamp is closed and so on, this is the preamp reset we discuss this, this is the latch and beyond this it goes to the digital backend. The key point to note is that, when a preamp is being auto zero it is enable to amplify, but we run the latch anyway.

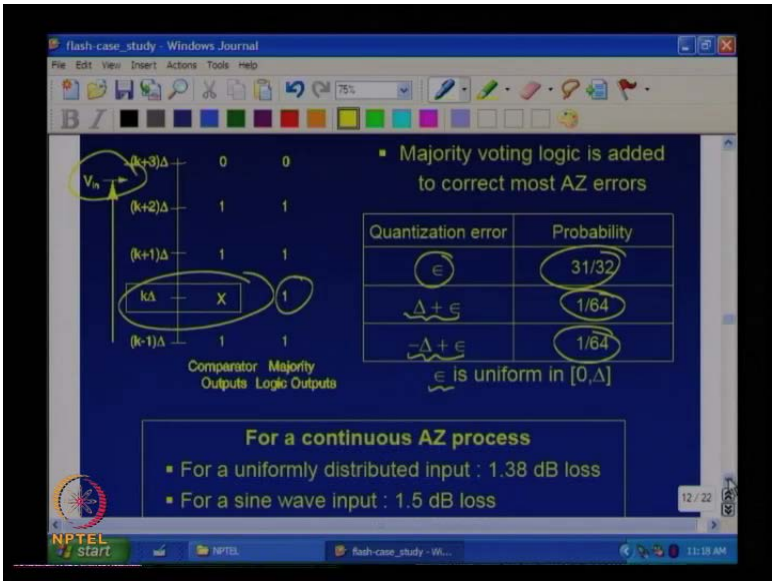
So, the output of the latch is some valid digital level, but it is got nothing to do with the input, so you basically denote that by some x.

(Refer Slide Time: 50:44)



And the auto zero is being run in the background, so what is the meaning of background auto zero, I mean you select some comparator and then, put it in the you disconnect the preamp from the input. And you put it into auto zero mode, the latch makes a random decision, all the others comparators function normally.

(Refer Slide Time: 51:15)



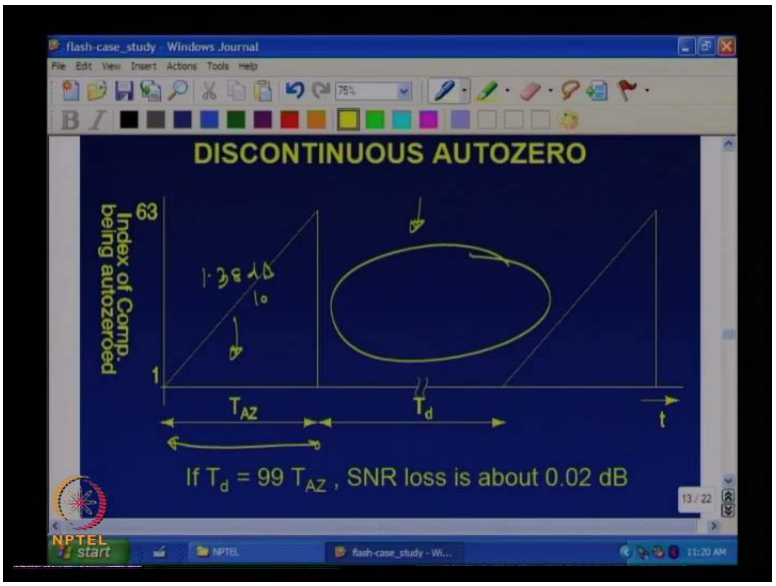
So, as we discussed in the last class, if a comparator is being auto zeroed, it gives you an x, but if that comparator is very far away from, the transition from the all ones to the all zeros, you have no problem at all, because this x will get corrected by the majority vouching voting

logic, which is use for bubble correction anywhere. So, to cut a long story short, you can do careful analysis, epsilon is the normal quantization error most of the time, the probability that the input is far away from the decision point is very high, because is only one decision point.

And but the input signal range is so large with the comparator that as being auto zeroed is not affected is very high, but with a probabilities of 1 and 64, we can show that the quantization error is either delta plus epsilon. Or minus delta plus epsilon with these probabilities, and epsilon is the normal quantization error, so from this you can go and estimate the mean square value of the quantization error, based on these probability distributions.

And the value of the error for each probability probable, so it turns out that for a uniform distribute input, you do the math and it turns out to be 1.38 d B loss in SNR. For a sine wave input it turns out to be a 1 and half d B loss, the reason is that the sine waves spends more time, at the peaks than at the zero crossings, and that slightly pushes up the error.

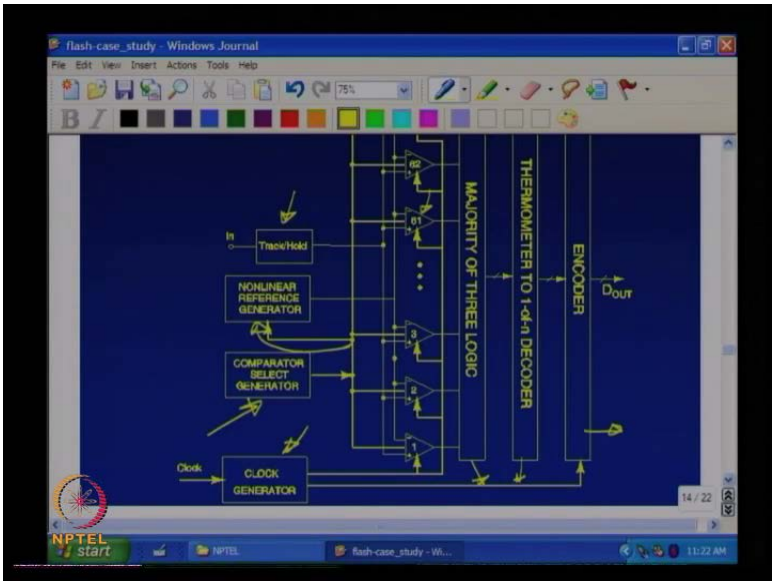
(Refer Slide Time: 53:28)



Now, as I was mentioning to you earlier, you can in principle hold, the reference and the offset for a long time, there is no need for you go through the array and come and start again. So, you run through one complete auto zero cycle wait for a long time, long enough to start losing charge on the auto zero capacitors, and start all over again, during this entire period it is like having an ideal array; it is only here that you hit you see a 1.38 d B loss in SNR.

So, when you amortize this over a large period, the effective loss in SNR becomes very very small, and you can see that, the hardware complexity is this pretty much the same as a regular flash array. There is none of these substitute going in and coming out all that stuff.

(Refer Slide Time: 54:36)



So, this is the top level the ADC, there is the comparator array, there is a track and hold this is the comparator array, you need some control with go to each of the comparators to tell them when to get into auto zero. The same thing must also go to the non-linear reference generators, please note that the what is the idea behind using the non-linear reference generator.

Student: ((Refer Time: 55:08))

[FL]

Student: Distortion is in reduces

What is the idea behind using the non-linear reference generator

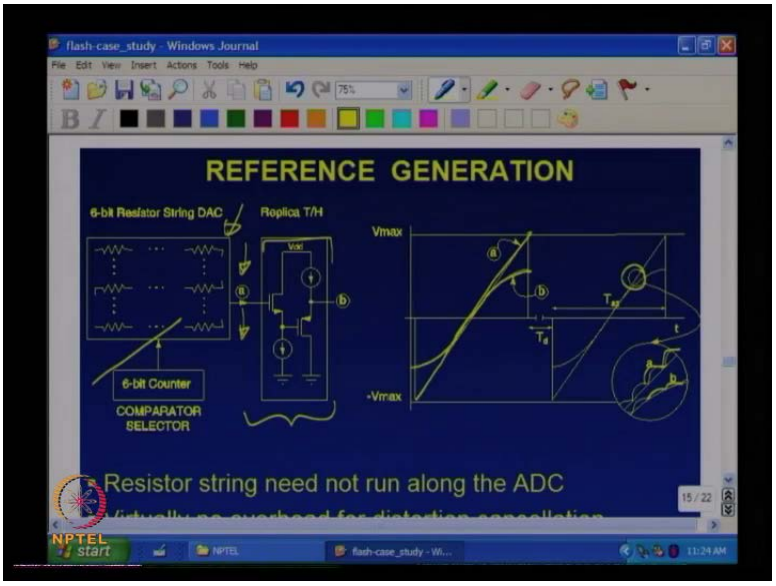
Student: Power dissipation

What is it trying, what you trying to do with it

Student: ((Refer Time: 55:26))

You are trying to pre-distort the reference to the comparator, precisely in the same way that the input would due to the, the input track and hold would due to the input signal. So, since you need to generate a non-linear reference for that particular comparator, which comparator you select for auto zero all that information also an use to go to this, non-linear reference generator. And of course, you need a clock generator to power the entire array, and the usual digital backend which consist of majority of three logic thermometer to one of an decoder and the encoder, which takes the one of encode and generates the binary code.

(Refer Slide Time: 56:10)



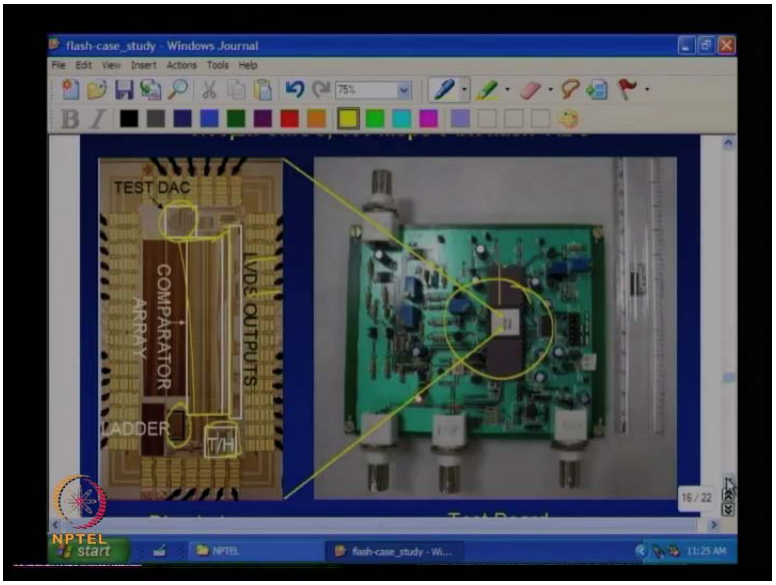
The reference generation is a is very straight forward, so you have the usual resister string, which you would need in a regular flash anyway. Now, this output which will be generate linear references, you need to select only one of those references, and pass them through the that one track and hold, which is the replica of the main track and hold in the signal path. Now, for the replica track and hold all you need is a P MOS source follower followed by an, N MOS source follower followed by a P MOS source follower, you do not need that switch in the capacitor and all that stuff.

Because, this is only static nonlinearity, so as the counter here, which is the 6 bit counter counts from all the way from 1 to 63, the output at this node will be a ramp which goes differentially from minus V max to plus V max, because it is deferential. The output of the differential track and hold will be something which looks like this, because of the distortion in the track and hold. And if you kind of zoom in here, the output of the resistor string will,

every time we change the count will change by one step, and the track and hold will also change in response.

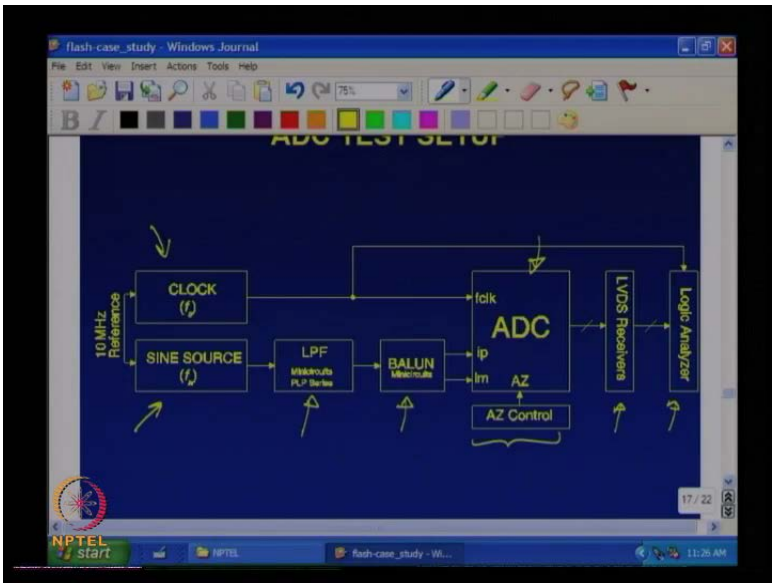
But, the change in the step size will be different for different input values for the track and hold, because it is non-linear. ((Refer Time: 58:09)) So, there is there is no over head for distortion cancelation apart from using a small replica track and hold, in the reference path, and the nominal ADV input voltage, can increase significantly over what was possible previously. Simply because, you are canceling distortion, in this case we were able to push it to 3.4 volts peak to peak deferential when compare to 1 volt.

(Refer Slide Time: 58:44)



And this is the chip, so this is the comparator array, this is a track and hold this is the ladder. And now the ladder can all be in one small place, it does not have to run along the comparator array, because only one comparator is being auto zeroed at one time, you do not need all the references all the time. And this is the digital backend and all that stuff, here is a small DAC, which will put out an analogue version of the digital code going out of the ADC. Just so at you can test the converter for functionality on a scope, these are the LVDS outputs, and this is the board which was used to design, which was design to use to test this chip.

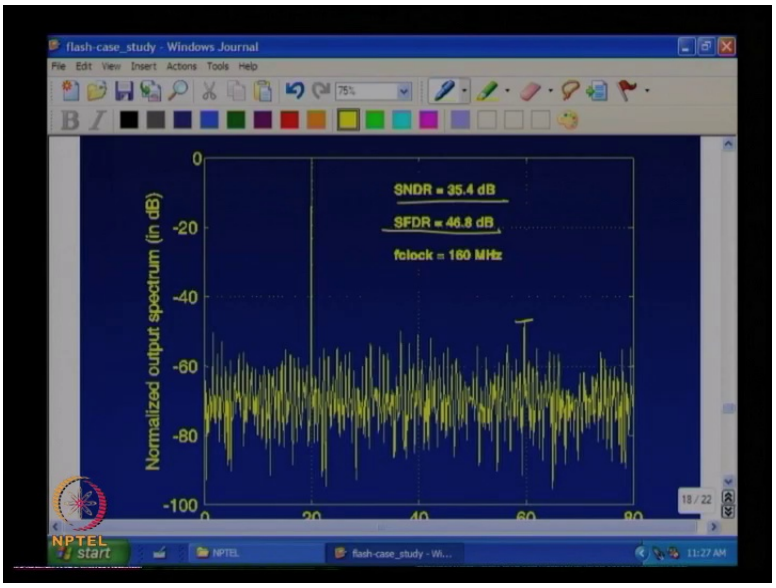
(Refer Slide Time: 59:47)



And this is a test setup which is pretty standard the source, and the sampling clock are slinked, the reason is that you can use then, a rectangular window estimate the SNR. There is a low pass filter for the sine wave source, to cleanup all harmonics there is a transformer to convert a single ended sine wave into a differential one. And this is the ADC test chip which has the clock and the two inputs, we also have a provision to either run the auto zeroing, either continuously or once in a while, this will help us see if that 1.38 d B is actually a, is what we are getting in the degradation in the SNR.

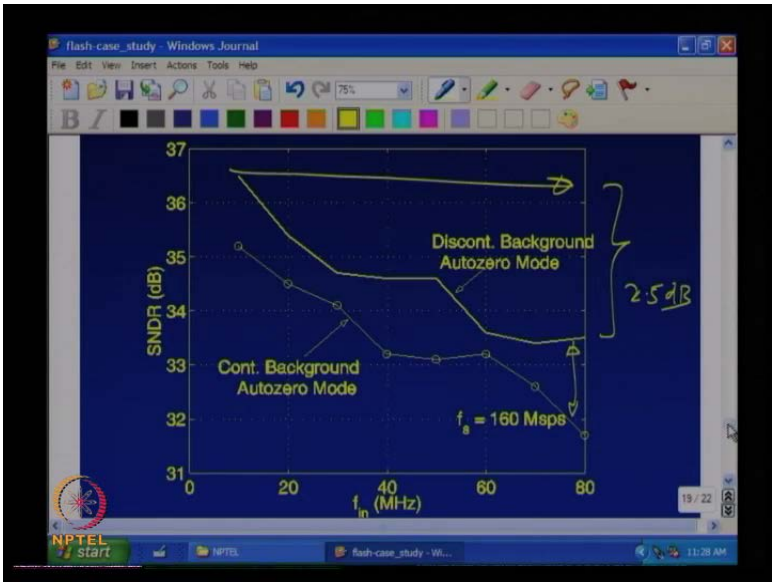
And finally, this goes through some LVDS receivers on the board and to a logic analyzer, which captures the digitize the data, to take the data into mat lab and do all your FFT.

(Refer Slide Time: 60:45)



So, this is the output spectrum measured, the SNDR at low frequency is about 35 and half d B, which is pretty close to what you should get for an ideal 6 bit flash converter. And the distortion in spite of using a very very large signal swing, is about 47 d B which is kind of what you would get for a 6 bit something, which is close to a 6 bit flash converter ((Refer Time: 61:18)).

(Refer Slide Time: 61:19)

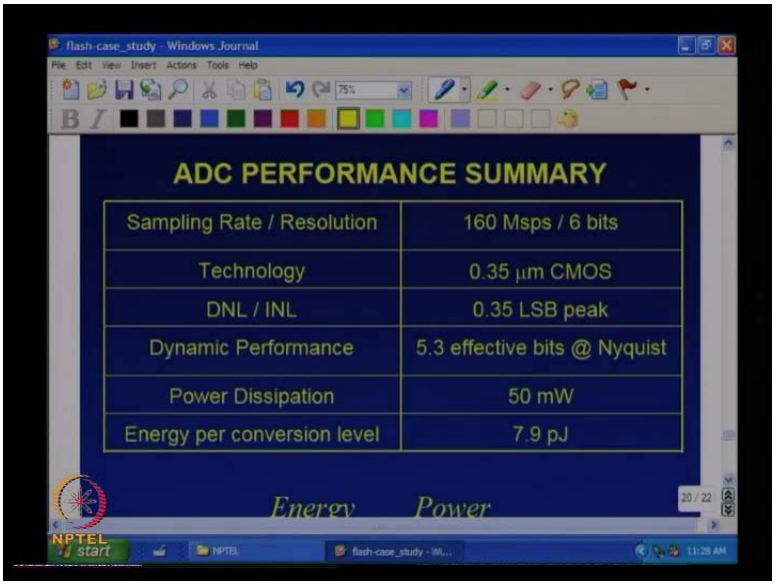


And like all circuits the performance will degrade slightly with input frequency, so as you increase the input sinusoidal frequency, as you go towards Nyquist you can see that the, SNDR actually reduces, however the degradation from DC to Nyquist is only about...

Student: 36

What is this 36 and half to about a 34, is about 2 and half d B also, and as you can see with discontinuous auto zero mode, you can see that the SNR is about 1 and half, on the average 1 and half d B higher than, if you do this continuously. That make sense, because whatever error you have is getting amortized over a smaller or a larger time.

(Refer Slide Time: 62:21)



So, when you go and compare it with state of the art, a figure of merit for a converter is basically the power you dissipate, divided by the effective number of levels, divided by the sampling rate.