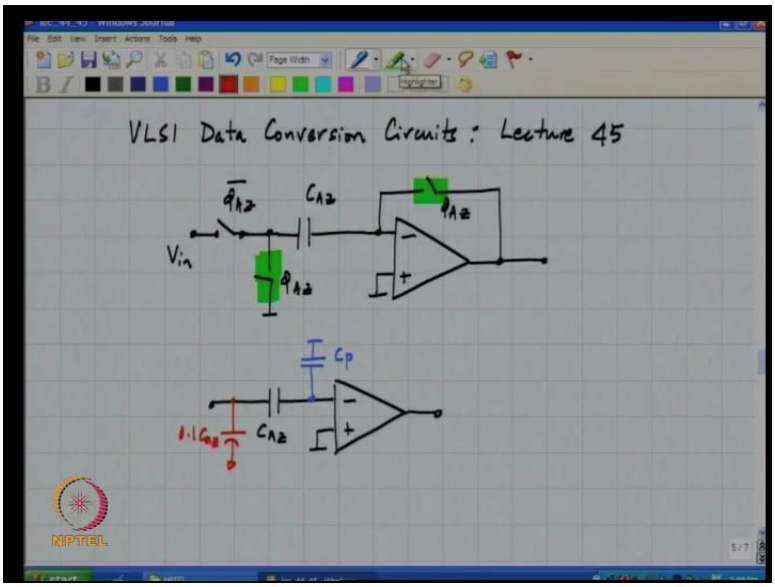
VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 45
Autozeroing – 3

(Refer Slide Time: 00:15)

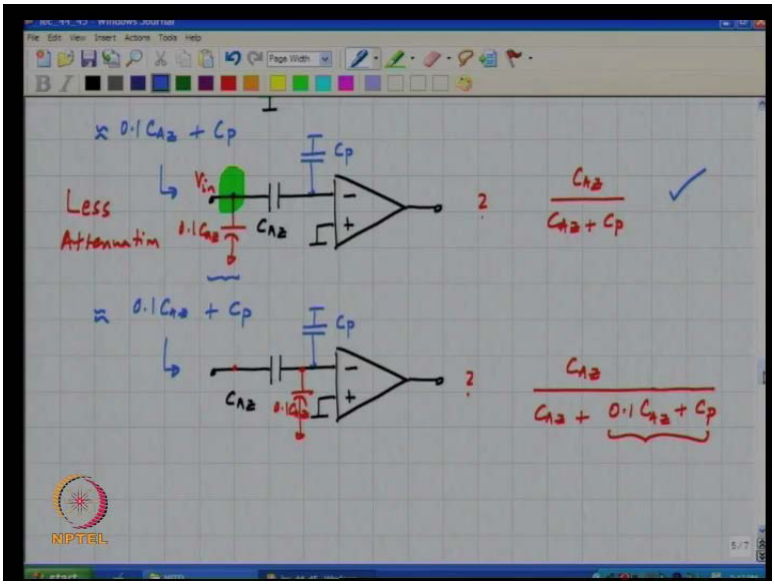


This is VLSI data conversion circuits lecture forty five; in the last class we were looking at the preamp and I wish to make one last minor point about it. This is the single and equivalent of the preamplifier with the auto zero capacitor in place during the auto zero phase these switches marked in green are closed, but during the amplifier phase the equivalent circuit looks like this with appropriate value of estimated offset stored on C A z. As we saw the last time around the input of the preamplifier itself has some parasitic capacitance C p and we saw that it makes sense to choose C A z to be not so small as to cause a big attenuation due to the series combination of C p and C A z.

On the other hand you do not want it to be very large either simply because making this capacitor C A z get charged to the estimated offset value it depends it becomes difficult. Because, the preamplifier has to drive this load capacitance and depending on the nature of the preamplifier the tradeoff's vary, but one thing can be said that if you want to charge a larger capacitor to the same voltage in the same time it means that a larger amount of charge must be deposited on this capacitor, which in turns means that current somewhere must be large.

So, it is appropriate to choose C p not to be so large as to make it difficult to charge nor so small so as to make the input signal smaller across C p because of this finite attenuation. In the last point that also precludes making C A z very, very large is that in practice it. So, turns out that C A z is accompanied by a bottom plate parasitic capacitance. So, one of the plates of C A z if not both have a capacitance from the bottom plate to ground. So, this capacitance is let us say about this capacitance is about ten percent of C A z.

(Refer Slide Time: 04:06)



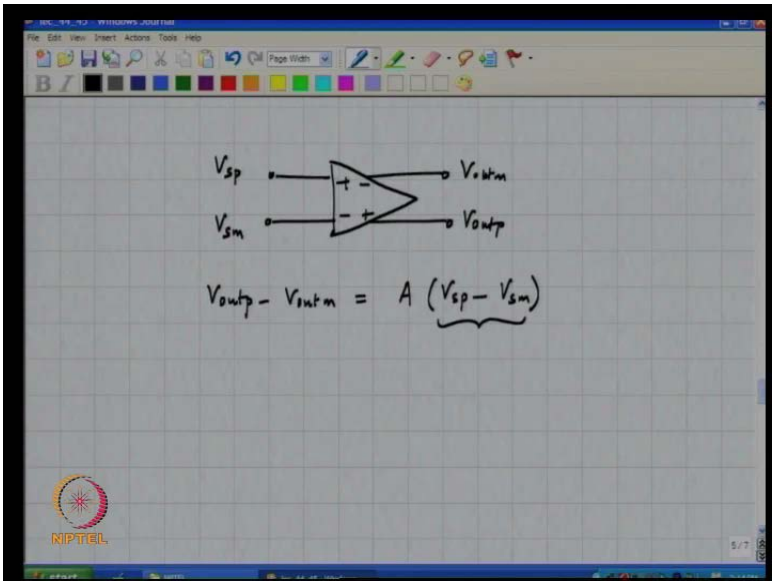
There are two ways of physically placing this capacitor. One could either place the bottom plate towards the input as shown here or take the opposite stand and place the bottom plate here. So, the question is which of these two strategies make sense? Clearly the attenuation from V in to the voltage across C p in the first case becomes C p why oh rather I am sorry C A z over C A z plus C p. In the second case it is C A z divided by C A z plus 0.1 C A z plus C p. Clearly this capacitance is larger therefore; it means that there is less attenuation here when compared to the case where you put the bottom plate to the right. Can you comment on the input capacitance looking in both cases?

Please recall that in a good design C A z will be much much larger than C p, because you want to make sure that the attenuation due to the series combination of these capacitors is small, which means that virtually all of Vin is appearing across C p which means that the input current is simply the current being drawn through the parasitic capacitance plus the

current which is being drawn through this point 0.1 C A z. So, the c in this case is approximately the bottom plate capacitance which is 0.1 C A z; as an example plus C p how about here now in the second case. Again if you assume that C A z is large which is what you would do in order to make the voltage at the input of the preamp roughly the same as the main input you will find that the input capacitance is approximately 0.1 C A z plus C p.

And this means that regardless of the orientation of this capacitor the input capacitance is the same, which means that the sample and hold has to drive the same amount of load capacitance; whichever way you choose the orientation of the auto zero capacitor. On the other hand the first choice namely putting the bottom plate on the sample and hold end prevents unnecessary attenuation of the sample and held voltage by this series combination of C p and C A z. So, this is the preferred approach; in other words you want to put the bottom plate parasitic towards the left side or the sample and hold side.

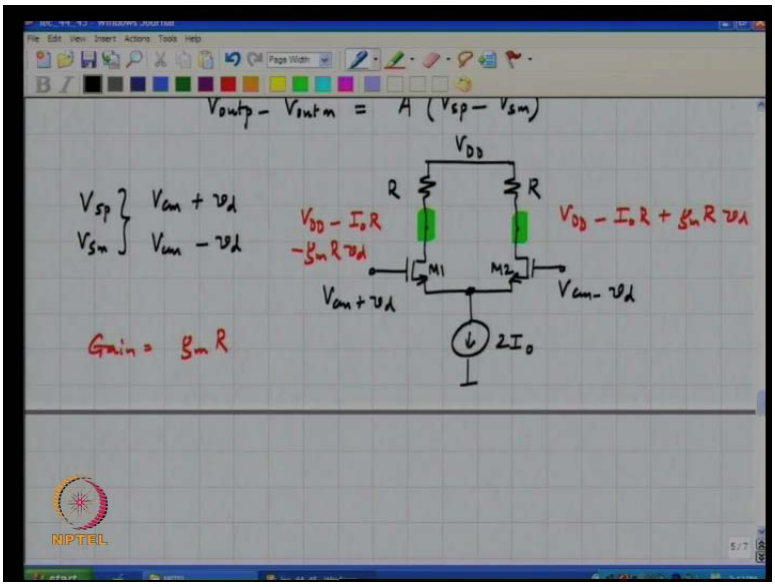
(Refer Slide Time: 08:11)



The next thing is to try and figure out how one might be able to design using transistors a preamplifier, where the basic idea is to take a differential voltage and generate another differential voltage. So, let me call this V s p and V s m, where s stands for sample and hold. So, the sample and hold output goes here and we want V out p minus V out m to be equal to some gain, hopefully as large as possible times V s p minus V s m. So, in other words we are interested in amplifying the difference between V s p and V s m. Now,

whenever you are asked to amplify the difference between two voltages, what is the first circuit that comes to mind the differential pair?

(Refer Slide Time: 09:16)



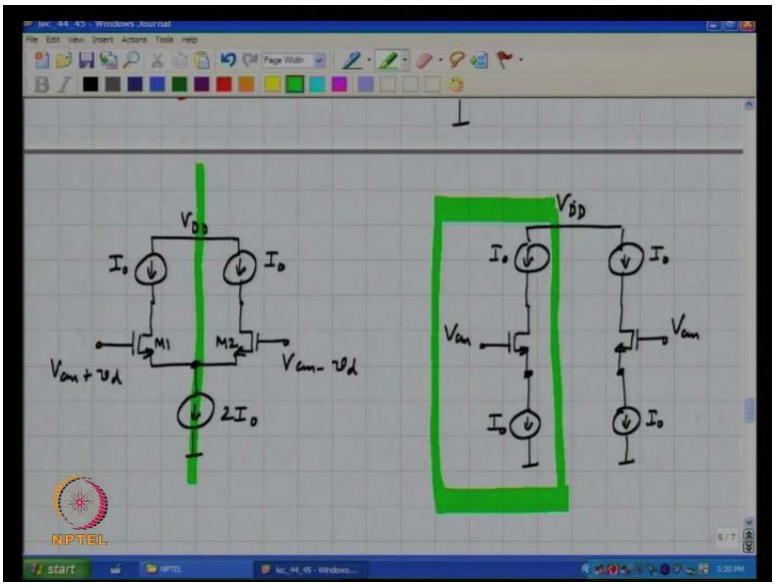
So, let us start from those lines the tail current is denoted by 2 I naught the 2 voltages V s p and V s m can always be written as the sum of a common mode component and a differential mode component and common mode component minus a differential mode component. So, I am going to denote this by V c m plus v d and this by V c M minus v d and as usual two load resistors to supply. Let us quickly review the quiescent operating point.

So, to determine the quiescent operating point, we assumed that the difference between the two inputs is zero, in which case the quiescent drain potential will be is simply V D D minus I naught R the incremental voltage on the right leg of the differential pair will be g m R into V d what about the left side minus g m R into V d. Now, in order to get a larger gain I mean clearly the incremental gain is g M times r. So, in order to increase the gain without increasing the quiescent current or the transistor size one seems it seems tempting to go on increasing R.

Unfortunately as R keeps increasing and if the supply remain the same the quiescent potential at the drain of the transistor which would normally be V D D minus I naught R would become lower and lower and eventually cause these transistors M 1 and M 2 to go into the triode region the only way this can be prevented is by raising the supply which is

not practical thing to do. From our experience with circuits earlier what do you think we should now do?

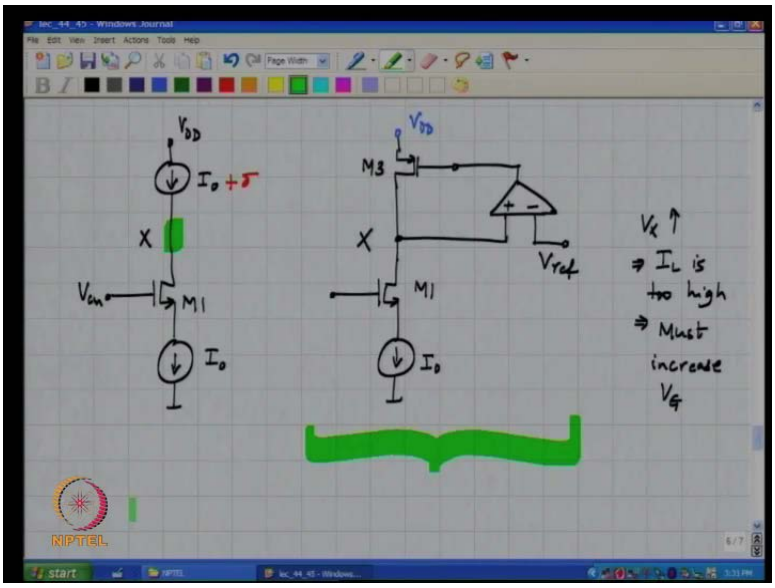
(Refer Slide Time: 12:40)



So, the solution to this problem is to not use a resistor, but employ an active load instead where the idea is to replace the load resistors with current sources and this enables a large incremental gain without increasing supply voltage. Now the circuit is symmetric around this axis shown in green; therefore, it should be possible to use half circuit analysis to understand the operation of the circuit. So, let us try and see first how this circuit looks for common mode inputs. Please realize that if we are interested in high gain at all one must make sure that all the transistors are operating in the saturation region.

So, when a purely common mode signal is applied in other words let us just say these two are the same potential. The first thing to do is to determine the quiescent operating point and because of symmetry one can split this tail current source into two identical ones. Strength is I naught and since no current flows through the leg in the middle one can get rid of it. So, as far as the operating point calculation is concerned all that one needs to worry about is one of these halves.

(Refer Slide Time: 15:12)



So, let us try and understand what the operating point will be with the aid of this half circuit this is V D D, this is I naught and this is I naught this is V c m and we are interested in the node potential at X. So, if the tail current here I naught and the current source in the load were exactly identical up to the two hundred decimal place, then one can say that the amount of charge flowing into node x is exactly the same as the charge which is being removed from node X in a particular interval of time therefore, no net charge is flowing into node X. So, the potential of node X will stay put at it is you know whatever value it was.

So, hoping that X was initially at such a potential that the transistor M 1 operated in saturation, we see that thing seem to be in practice I naught in the tail and I naught in the load are built with mean a transistors and these are by definition independent current sources, which means that they will not be exactly identical. It is impossible to make them exactly identical the only thing one can do is to make sure that you know they are only approximately the same. Now, let us assume that the two are off by a small delta where this delta can either be positive or negative. if delta is positive, it means that the current being pumped into this node X is larger than the current that is being withdrawn from X which means that net charge is going into node X, which in turn implies that the potential of node X will keep going up.

Now in the ideal world where the current sources are ideal this potential will go to infinity, but in practice we know that this current source which is in the load network is being implemented by a what kind of transistor? Is being implemented by a PMOS transistor, which will because I mean if the potential of node X keeps increasing it is only a matter of time before the source drain voltage of that PMOS transistor or that combination of PMOS transistor has become. So, the transistors enter into triode region and thereby this current source is no longer a current source, which means that you do not get the large gain that you are looking for is this clear.

By the same token if delta is negative, the current being pulled out of node X is larger than the current being pushed into the node X thereby causing potential of X to drop it will keep dropping the first casuality will be the transistor M 1 which will go into the triode region the moment M 1 goes into the triode region the potential at its source will track the potential at its drain, which should not happen if M 1 was in saturation. In saturation the potential at the drain and the source are isolated. The moment M 1 goes into the triode region the potential at the drain namely V x will also reflect at the source and eventually the tail current source will also go into the triode region. Since M 1 has gone into the triode region and its current is reduced the gain again will be very small.

Now the soul reason for this problem is that the potential of node X is being or two current sources which are independent are controlling or attempting to control the potential of this node and since the two of them are mismatched which will happen in practice the potential of node X either goes attempts to go towards infinity or ground or to minus infinity and we will get limited to voltages which are close to V D D or ground as the case may be. Since the problem is therefore, that the potential of x is not being we are not able to set the potential of X to you know stable value, because these two current sources are independent.

So, the potential of node X is being controlled by two independent current sources and for instance if you are in a company and one have two independent bosses who are telling you different things to do. Obviously, it is only a matter of time before you go insane; because each one of you wants each one of them wants you to do different things. In this particular case opposite things one wants to push you know you to go up the other one wants to you to go to go down. So, that is clearly a problem. So, the only a way to

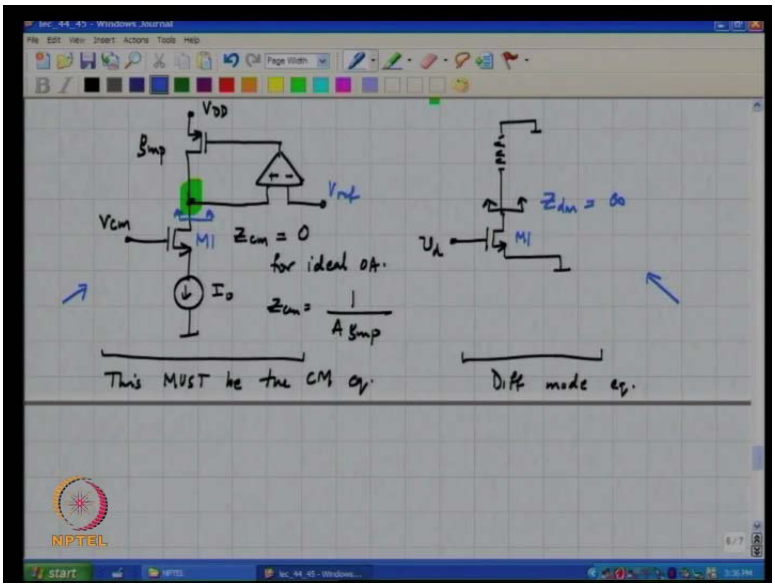
maintain sanity right or the potential of node X for that matter is to make sure that these two people who are trying to control the potential of X talk to each other.

So, that they are saying the same thing and the only way that can be done if both of them are talking to each other and agreeing with each other it means that both of them are not really independent. One of them has to be dependent on the other right and there is no harm in or loss of generality in making the tail current source independent right this is not necessary, but as an illustration I will just use that. In other words, I will assume that this tail current I naught is independent and the load current is dependent on I naught. So, in other words the load current is not some random I naught, but is chosen to be exactly equal to the strength of the tail current source.

So, basically what we need is a variable current source because it has to be dependent. So, what kind of what is the simplest variable current source you can think of which will push current down. No what is the simpler I mean you need a variable current source here and must push current down. So, what is the simplest way of doing this? A PMOS transistor and this is the control port and you want to make sure that this node potential is constant and making this node potential constant rather you want to make sure that this is the load current is exactly equal to the tail current and instead of comparing currents; one can as you well aware from prior experience, you can simply monitor the potential at node X if V x goes up it means that the load current is too high, which means that if this is V g I L is too high.

So, what must be done? One must increase V x. So, this is a standard negative feedback increase V g. This is a standard negative feedback process. So, if you assume the availability of some kind of forward amplifier in this case I have just assumed it to be an ideal opamp, if this goes up the output must go up and therefore, I will compare V x against a reference and kick V g upper down depending on whether V x attempts to go up or down. So, in steady state the potential of node X will be at V ref and V ref must be chosen to be high enough. So, as to keep M 1 and saturation and low enough that the load transistor M 3 does not get into the triode region. So, recall that this is the common mode half circuit and must only apply to common mode signals.

(Refer Slide Time: 26:30)



So, in other words we want our preamp to have a common mode equivalent which looks like this and at differential mode equivalent, which looks for small signals like this. I have drawn the resistor in dotted lines simply to indicate that that resistance is very, very very high and should ideally be a current source with I mean an incremental open circuit as the equivalent impedance. So, what do you suggest we do? So, in other words this must be the common mode equivalent and this must be the differential mode equivalent and another point that I wish to bring to your attention is that the incremental impedance looking in upwards from the drain of this transistor M 1.

If the opamp is ideal; please realize that the potential at this node which was the V x remains at V ref. V ref regardless of whether current is pumped into the node or pulled out of the node since the voltage at node X does not change in response to currents injected into that node it is behaves like an incremental short circuit, which means if the incremental impedance looking upwards from the drain of M 1 is 0. So, in other words since this is the common mode equivalent it implies that this feedback loop makes the common mode impedance. Simply, because it is appearing in the common mode equivalent circuit the common mode impedance looking in from the drain of M 1 is 0.

So, this let me just add that note here Z c m is ideally 0 in practice the gain of the amplifier will not be infinite; if you call it A then the in practice of course, Z c m will be one a times g m of the PMOS transistor. This is easy to establish you just apply voltage

measure the current. So, on the other hand let us observe what the impedance is looking in here. What is the differential mode impedance? It should I mean we want it to be the output impedance of that current source, which we ideally hope to get I mean ideally we would like it to be infinite, but in practice we will take whatever we get in the sense that if you maintain the transistors in saturation is Z d s is what we would like to get.

Now, our job is to find a circuit whose common mode equivalent looks like this and whose differential mode equivalent looks like this. So, one thing that one can think of I mean whenever you are given a half circuit and want to find the real or the full circuit what do we know the half circuit is basically is symmetric about some axis. So, what I would normally do would be to copy and paste about some axis of some symmetry. Let us see what we arrive. So, if this is V c m plus v d this is V c m minus V d correct the source; please recall that in the differential mode equivalent we want the source of this transistor to be grounded.

So, what should we do? Connect together the sources. We need to connect the sources together all right. The polarity of this is I made a mistake all right now in the differential mode equivalent without doubt this terminal is a short circuit for balanced inputs. Now what about the common mode? Only you can have resistance in as far as the common mode equivalent circuit is concerned we seem to be doing what about the differential mode impedance of the load.

If the op amps are ideal; So, if the op amps are ideal we see that regardless of whether you inject a common mode current or a differential mode current; the two voltages at these nodes. Let me call this x and y the potentials at node x and y remain put at V ref. V ref regardless of whether you push two currents in the same direction or two currents in the opposite direction through nodes x and y. That is because the op amp which is supposed to sense only the common mode potential at x is sensing the total potential at x. You understand let us get back to this circuit this is the common mode equivalent this is what we want the common mode equivalent to be and what is the op amp doing.

It is the sensing the potential at X and controlling the gate of the load transistor. So, in the in the context of the entire circuit it must be interpreted as the op amp is sensing the common mode voltage at node X, because after all we are talking about the common mode. Common mode half circuit we are sensing we are supposed to sense the common

mode potential at node X and go and tweak the gate of the load transistor. So, that the common mode voltage at node x is exactly equal to the reference. This is same this makes sense because this is what half circuit analysis is all about. Every impedance you measure is the common mode impedance right every gain you measure is a common mode gains every voltage you sense is a common mode voltage every current there is a common mode.

So, what we are supposed to be doing is to sense the common mode potential at node x and tweak the gate potential of the PMOS transistor appropriately. So, that the common mode of at node X is held constant at V ref. V ref, but the mistake we have made when we have simply copied and pasted this circuit as is common with this half circuit analysis is that instead of these this op amp is now not sensing the common mode potential at x it is sensing the total potential. The total potential at x which is the sum of the common mode, Differential mode does it make sense. So, in other words what we need is not this set of loads what we need is one op amp which senses the common mode potential at node x or y the by definition the common mode potential at x and y.

So, given two nodes x and y how will you sense what is the meaning of the common mode potential. The common mode potential of two nodes is simply the average of their two potentials. So, if you have nodes with potentials V x and V y what is one very simple way of measuring their average. You know one can say one way of computing their average potentials is to you simply use a resistive divider though this is not the only way one should do it let me call this R c m and R c m just remind ourselves that we are dealing with a network intended to measure the common mode values of these two potentials now what are you supposed to do.

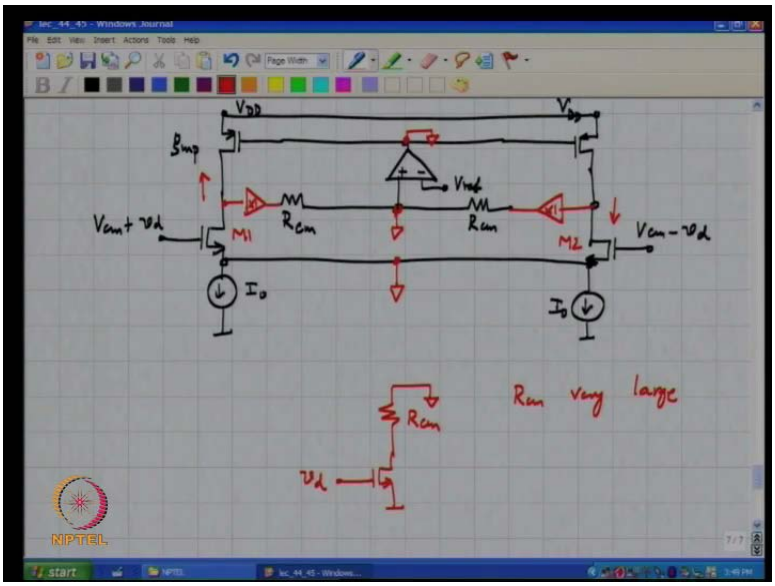
We compare this with some of the reference V ref and then do what. This must be connected to the gates and which must be the positive terminal of the op amp. The left side of the op amp must be the all right. So, in the common mode equivalent circuit what happens to R c m? No current flows through R c m in the common mode equivalent which means they can be replaced by short circuits, because the voltage drops across them only in the common mode equivalent. So, this now represents a circuit where the common mode equivalent is what we had put down all right what is the differential mode equivalent?

For differential mode signals what happens this node potential goes up this node potential goes down. So, what happens to this potential? It is firmly grounded. This node potential is grounded this node potential is. The source couple node is also grounded if this voltage is zero incrementally what is this voltage incrementally. That must also be zero, but because that is simply a multiple of the input voltage. So, for the differential mode signals what is happening is that we have an equivalent circuit which looks like this where the transistor M 1 is grounded at the source and in the drain what do we have?

We have R c M assuming the PMOS transistor has got infinite output impedance is this clear. So, if you want to get a lot of differential gain I mean can you comment on the size of R c m you need to choose. I mean you want to choose R c m to be very large and as I said I mean the reason why you want to choose R c m to be very large is because even though R c m does not appear in the common mode equivalent. It loads the differential mode part of the circuit causing the differential mode gain to become small.

One simple way of fixing this problem is to use buffers here, at least in principle this is one way of making sure that the R c m resistors do not load the differential output. Because, the current are beings the currents through R c m are being supplied by the voltage controlled voltage sources.

(Refer Slide Time: 43:22)

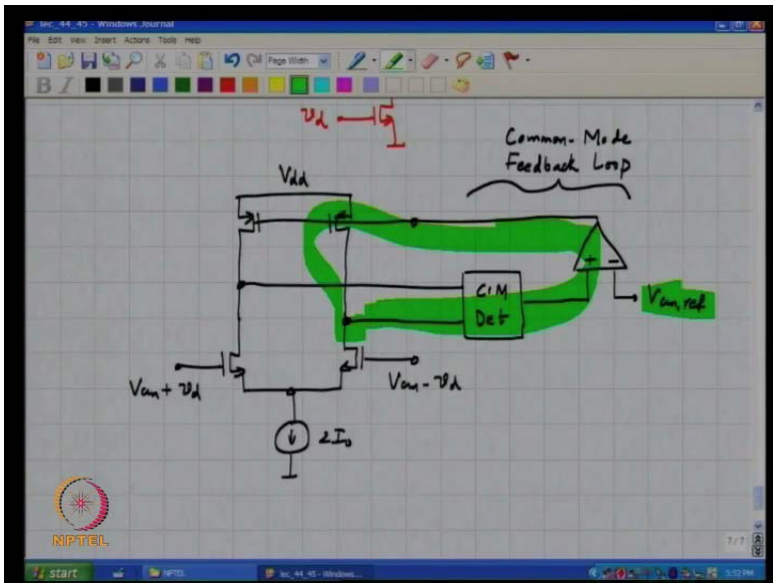


So, in general a differential amplifier with common mode feedback will look like this.. So, this is a common mode detector whose job is to generate the output or sense the

output common mode voltage. One simple way of doing it as we just saw is a resistive common mode detector, which simply is a potential divider unfortunately it loads the differential mode equivalent also. You compare this with some common mode reference and if some kind of amplifier not necessary in op amp; in order to tweak the gate potentials so as to make the output common mode reference I mean the output common mode voltage exactly equal to the common mode reference that you have set.

So, this is a block diagram form of a differential pair with common mode feedback. So, this network whose job is to monitor the output common mode voltage and apply corrective potentials at the gate of the load to make sure that the supply I mean the output common mode voltage is indeed at the desired reference is called the common mode feedback loop. The actual feedback loop runs through like this. There is any number of ways of implementing the common mode detector so called amplifier. So, you will have any number of ways of implementing a common mode feedback loop. But this is the basic idea in several implementations this V c m ref may not be an explicit one.

(Refer Slide Time: 47:43)



A good case in point is the following I think one of you had suggested this when I was discussing the common mode half circuit. All of you are aware that instead of using an op amp. One could I mean this node potential if this node potential is going up we need to make also go up. So, there is no need to use an amplifier in principle one could

actually connect these two. Now, if this is the common mode equivalent how you think the actual circuit will look like.

Can I do this? As usual what this is telling us is that the output common mode must be fed back to the gate not the absolute voltage itself. So, what one must do must be to sense the common mode someway the easiest way is to simply do this as I did not care it before and put this here. So, if I now call this R c m the incremental gain is it simply g m times R c m.

So, these resistors only appear in the differential mode equivalent and this is an example where there seems to be no explicit common mode reference. What is the final output common mode voltage? What will it settle to? It will simply the final common mode voltage that will occur is V d d minus V s g of the PMOS transistor which is of course, depends on V t p and square root of 2 I naught by mu p c ox w by l. There are also other conceivable ways where you do not need to load the outputs with resistors to measure the common mode. One way of another way of measuring the common mode for instance would be to convert these voltages into currents.

Add the two currents up which now has got information on the output common mode voltage in current form compare it with the reference current either explicitly or implicitly and use that information to go and tweak the gate voltage. And again the control as we discussed before we assumed that these two are independent and the load currents are dependent. One can reverse the situation and say the load currents are independent and I am going to go and tweak the tail current to make sure that the common mode at the drains of the two input transistors remains fixed.

So, there is any number of ways of making this work. In the next class we will figure out now that we have made a fully differential amplifier with some gain we need to add all the rest of the piece of the puzzle and most critically we need to interface the latch to the preamplifier in the right manner. Please recall that the preamplifier output is only relevant at the sampling instant of the latch. After the latch samples the preamp can be used for other things say out of zero say I mean whatever else because the output of the preamp is not relevant at that point in time you understand. So, we will look at timing and the complete comparator slice which is in this simple case a preamplifier followed by a latch in the next class.