VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 44
Autozeroing - 2

This is VLSI Data Conversion Circuits, lecture 44. In the last class we were looking at how one could reduce the offset of a latch.

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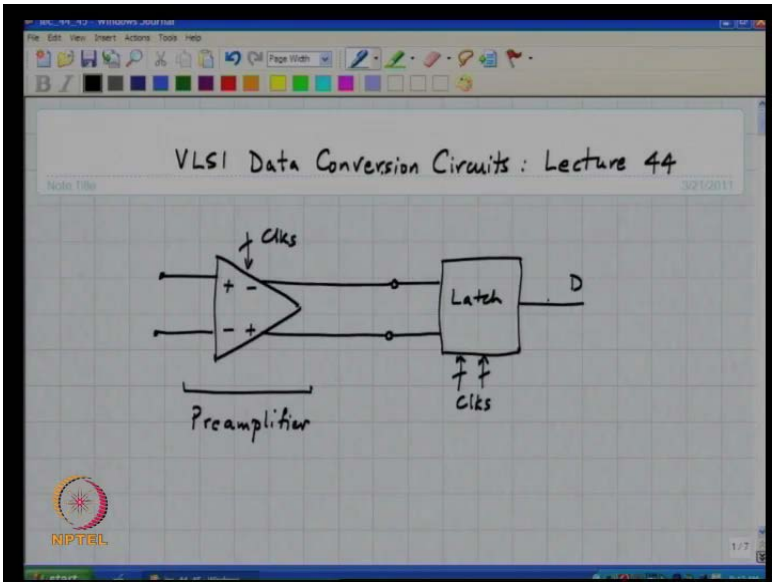

Please realize that the latch itself is some pretty complicated circuitry inside that box, which operates with a whole bunch of clock phases and so on, and finally gives out a decision D. And we also understand that the latch is working of or sample of the input, it is not a continuous time comparator, what it is doing is it is sampling the input implicitly, and figuring out of that differential input is greater than 0 or smaller than 0.

And due device mismatch, we have static and dynamic offsets, and the offset can only be minimized by increasing the size of the devices, which will in turn increase the power dissipation. So, what we then decided was to say, if the latch has an input referred offset that can be reduced by a factor A, if one puts in front of the latch an amplifier with a gain A. Unfortunately now, the amplifier with a gain A will have offset in itself, simply because it is also made with transistors, and these transistors are also likely to be mismatched.

And again one could reduce the input referred offset of the amplifier by making the device sizes larger and larger, and larger however, this carries the penalties of A power dissipation. And two I mean, while it is true that you indeed burn more power in this amplifier, the input capacitance of the amplifier will also increase, which means that the stage driving the comparator, which is basically the what is driving this array of comparators the sample and hold, which drives the array of comparators.

Now, has to drive a much larger load capacitance, which in turn will mean that it has to burn a lot more power, because a larger capacitance has to be charged to the same voltage, which means that there is a lot more current flowing through the capacitor. So, brute forcing it by deliberately making the offset low, does not seem like a very attractive solution. And understanding that this is a I mean we are working of a samples, one can say that during some part of time, the latch is actually amplifying the difference between it is inputs.

And at that time the output of the amplifier, before the latch is not really necessary, so the latch is reading or observing the output of the amplifier, which occurs before the latch, and which is why this is called a preamplifier. The preamplifier output is being observed by the latch only when during some part of the clock period, once the latch samples the output of the preamplifier, it regenerates the output.

And during that time what is happening, the preamplifiers output is not really necessary, which means that we indeed have time to do some housekeeping, so that time can be used to A estimate the offset of the preamp and subtracted off. So, that is the basic idea behind the whole thing and the last time around, we were trying to look at one way of cancelling offset, so this is called the preamplifier. And please note that, the timing of the preamplifier and the latch has to be carefully managed, because the output of the preamplifier must be sampled at the right time.

And then, the offset correction in the preamplifier must happen, precisely when the latch is busy, regenerating and making a decision and all that stuff.

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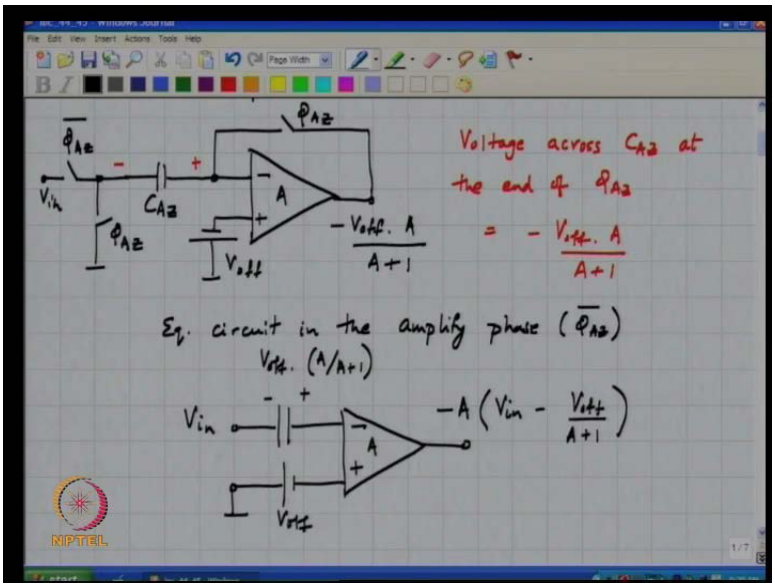

So, the basic idea behind the preamp as we saw the last time around, for a single ended example was to say, let us assume that we have an amplifier with an offset V off. And to estimate the offset of the amplifier, what one would be the following, measuring the output voltage of the amplifier when the input is set to 0, one would naively conclude that the output would be A times V offset. Unfortunately that is not true in practice, because if the gain A is large, the output of the amplifier will simply saturate, thereby giving us no information at all about the offset, except perhaps the sign.

So, the next idea was to say, we know that if we place the amplifier in a feedback loop, in this case specially chosen to be unity feedback. Then the output voltage of the amplifier will be approximately V offset, exactly what will it be, for this particular sign of offset chosen it I will be minus V offset times A by A plus 1. And as we see for A being a large number this voltage developed at the output of the preamplifier is virtually equal to minus V offset.

So, during this special phase called the auto zero phase, what we are doing is A creating a negative feedback loop around the preamplifier, estimating the offset which is now developed at the output, holding that on a that information must be stored for further use. And in analog if we want to store a quantity it must either be done with inductors or capacitors, and inductors are out of the picture, so must be done with capacitors. So, as

we saw the last time around capacitance C A Z is used to store the offset, so add the end of the autozero phase, what is the voltage across C A Z.

The voltage across C A Z at the end of phi A Z is nothing but, minus V offset times A by A plus 1, now if you open the auto 0 switches notice the following this voltage is approximately minus V offset. And this voltage is also minus V offset, thereby the same voltage is now apply to both the terminals, which means that in effect the difference is almost offset free. I mean the reason why it is almost offset free is that, the voltage across the capacitor is not exactly minus V offset but A by A plus 1 times V offset which is a number, which is very close to 1.

So, once the offset is being stored on this capacitor C A Z, the next job is to apply the input and that is straight forward, as we saw last time. So, the equivalent circuit in the amplify phase, which is phi A Z compliment, will be V in this is V offset, this voltage is V offset times A by A plus 1. And the output voltage will therefore, be A times V in minus V offset divided by A plus 1, so we can see that if A is sufficiently large, the input referred offset of the preamplifier has been reduced by a factor of A plus 1, which is approximately the d c gain of the amplifier.

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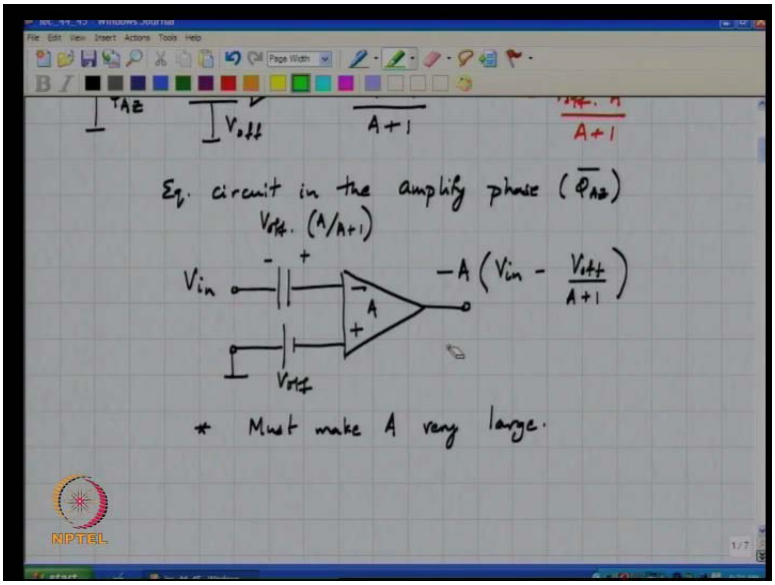

So, it is important to make A very large, while this is the basic idea you must, recall that we are now dealing with fully differential signals. And therefore, we must figure out a way of implementing a differential preamp, where the output of the preamplifier is a

difference between two node voltages, it is not referred to ground like the way we show here, you understand.

This output voltage by implication here, means that it is reference to ground, whereas the latch is receiving a differential set of inputs, which means that the output of the preamp must also be differential.

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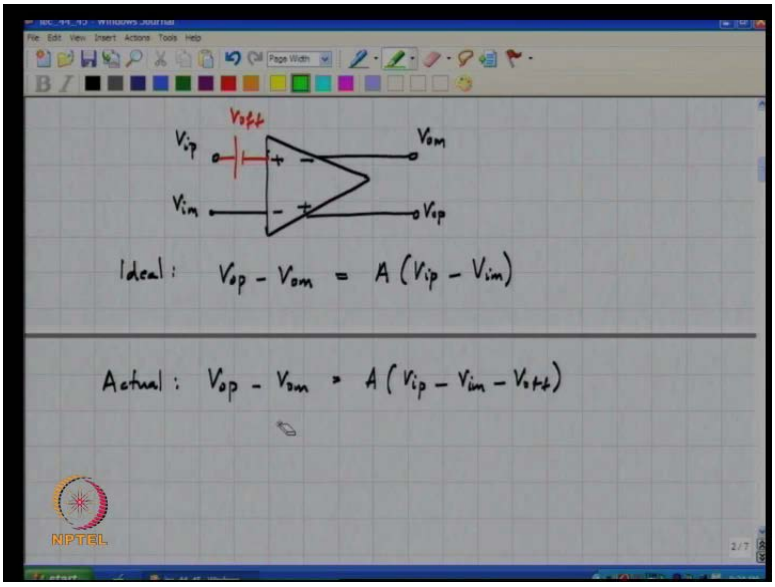

So, let us now see how one can realize something like that, so in other words what we are after is a preamp, whose differential output voltage is A times, if we call this V i p and V i m, V o m and V o p. Then V o p minus V o m is some A times V i p minus V i m, and again there will be offset and so on. And we can use a similar techniques that we have just discussed for the differential case, to illustrate that let us assume that this preamplifier is with offset of this nature.

In other words, V o p minus V o m is A times V i p minus V i m minus V offset, please note the departure from the earlier case, this is only saying that the difference between the two output voltages, is A times the difference between the inputs. There is no statement made as yet about the absolute voltage at the output, in relation to either the differential input or the absolute voltages at the input. Now, what do you think one can do to estimate offset.

Student: ((Refer Time: 15:54))

Again the same idea, so during the autozero phase we put this amplifier in a unity feedback loop, now what is the idea behind the unity feedback loop.

Student: The differential V o p minus V o m should be connect

The differential V o p minus V o m must be connected to the differential input, please note what was happening in the single ended case, let me redraw that ((Refer Time: 16:23)), so the negative input of the amplifier was being connected to the output. Now, the differential input must be connected in a inverted fashion to the differential output, so that means, that during the autozero phase, the amplifier is now placed in the unity gain feedback loop as shown here.

What will be the differential output now, let us just calculate how do you do this, what is the difference between these two nodes.

Student: ((Refer Time: 17:52)) V i p minus V i m

Just simply calculate this, so the positive terminal of the preamp input has a potential which is V o m minus V offset, this minus V o p times...

Student: A

A must be equal to V o p minus V o m, which means that V o p minus V o m must be equal to

Student: ((Refer Time: 18:54))

Minus V offset times A by A plus 1 just like in the single ended case, does it make sense. So, the difference between V o p and V o m during the auto 0 phase is minus V offset times A by A plus 1. And for a sufficiently large a this difference will be minus V offset, now the next job is to store this differential offset, again please note that the offset is not stored either as the absolute potential of the output p or output m. The offset information is stored as the difference between the two voltages, so which means that it is not enough to just hold V o p or V o m.

We need to hold both the output voltages, simply because the information the offset we are after is stored as the difference between the two. So, what do you think we can do...

Student: ((Refer Time: 20:23))

[FL]

Student: Capacitor at V i p and V i m

We need a capacitor at V i p and V i m, one way to do this is to say I am going to have, I am going to hold V o m on one capacitor, hold V o p on another capacitor, and I will explain the reasons for choosing this over what he suggested in a couple of minutes. So, this is phi A Z, phi A Z, C A Z, C A Z, let me call this V bias, so what is the voltage across C A Z at the end of the auto 0 phase.

Student: V bias

[FL]

The voltage across the auto 0 capacitor C A Z, at the end of the auto 0 phase is V o m, I mean as usual we define this to be the positive terminal, so V o m minus V bias and then, the other one will be V o p minus V bias. So, the absolute voltages across the two capacitors will have within quotes no meaning, the information we are after is what, V o p minus V o m and therefore, that is still available as the difference in the voltages across the two capacitors.

So, please note that the offset is stored as information on the difference between these two voltages, now we need to add the input, so what do you suggest I do...

Student: Two more situations

As usual based on our experience with the single ended example can it be here and what I have connected to the left side V i, to prevent abuse of notation I will say V, we sample and hold p, then we sample and hold m. Understanding is that, the inputs come from the sample and hold, as we can see the offset cancellation is not effected in any way by the absolute value of V bias we choose. Because, the voltage difference between the two capacitors remains equal to V offset into A by A plus 1, regardless of the value of V bias, because V bias is common to both sides.

Now, one feature of this fully differential preamp is that, it is a symmetric structure about this axis ((Refer Time: 25:39)), which means that the layout will be symmetric and the

parasitic will be symmetric at least in principle, on both sides of V s p and V s m. Once suggestion made was why do not you put one single autozero capacitor, across the two inputs and then, move it in series with, you understand.

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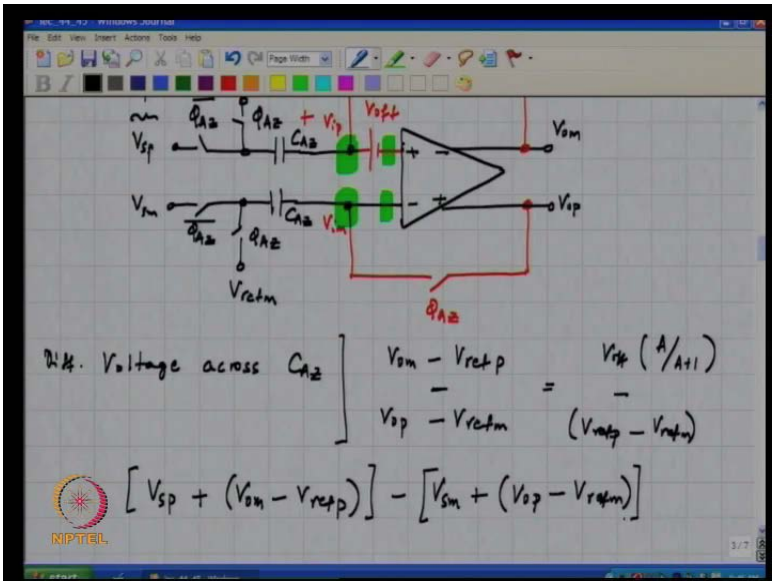

This is another conceivable approach, which is to say as usual this is phi A Z, and one could in principle store the offset on this capacitor C A Z and then, do what...

Student: ((Refer Time: 27:16))

Put this capacitor for instance, in series with one of the inputs, whereas V s m goes in to the other, in principle we should work, unfortunately there is several practical problems with this, there is the layout issue of both parts not being exactly symmetric. Another important point is that of charge injection, so we have dealt with charge injection in depth before, and the origin of charge injection is that every Mosfet conducts, when there is charge in the channel when you turn it off discharges to go out through the source and drain.

And is not exactly clear how much goes where, unless you carefully look at a various impendence at both know then, and calculate in stuff. So, here for instance consider this, what do you think is a good idea to avoid charge injection from these switches, do you think it particularly matters which is turned off first, do you follow my question. So, at the end of the autozero phase, we need to turn off these switches.

Now, you can either turn off the feedback path switches first, or the bias path switches first, which do you think is the better idea and why, I mean how many ways are there of doing this?

Student: ((Refer Time: 30:19))

You either turn of the bias switches first, or the feedback switches first, if we turn off the bias switches first, what happens?

Student: We turn on the bias switches first, there with charge injection and that current has a path through the capacitor.

Yes

Student: And then, the feedback switch and then to ground through the amplifier, so if we switch off the feedback switches first ((Refer Time: 31:04))

If we switch off the bias pass switches first, there will be charge injection, can you comment on the charge injection on both paths.

Student: ((Refer Time: 31:18))

They in the absence of mismatch in the switches, the same amount of charge will go on to both the capacitors, so there will be a change in the capacitor voltages. However, the change is the same in both the paths, which means that the differential voltage across the capacitors does not change. And why is this switch charge injection the same in both cases, because the gate source voltage of the switches is the same and that is equal to V d d minus V bias minus V t will be the gate over drive.

So, even though there is charge injection, that charge injection is a common mode affair, because it effects both paths to the same degree. So, if on the other hand one turned off the feedback path switches, what do you think will happen...

Student: ((Refer Time: 32:29))

The gate source voltage is mildly different, because one of them V o p and V o m are slightly different by approximately V offset. So, one could argue that there is nothing to choose you can either make one turn off earlier, or the other one turn off earlier or and

use the same clock for both, and you do not really care which turns off earlier. However, please recall that, ((Refer Time: 33:15)) we also need to subtract this preamplifier will only compare V s p and V s m, it will amplify the difference between V s p and V s m.

But, what are we after for the complete comparator, how will you build the flash is there something else we need to do or what, we need to subtract the references also. So, the last time around what did we do in the single ended case, how did we subtract the reference.

Student: ((Refer Time: 33:51))

We said instead of I mean out of the top plate of the capacitor was sampling the offset at the output of the amplifier, which was in the unity gain feedback loop. The lower plate was connected to a reference, so the true voltage stored across that autozero capacitor was the reference plus offset. So, the same thing can be done here also, now by analogy what do you think, how will you subtract the references.

Student: Replacing bias

Replace

Student: V bias

V bias by

Student: V ref p

V ref p and V ref m, so what is the differential voltage stored across the autozero capacitors...

Student: ((Refer Time: 35:06))

So, let us call this the capacitor on top has a voltage V o m minus V ref p, the lower capacitor has got a voltage V o p minus V ref m, which means that difference is nothing but...

Student: V o p minus V o m plus

V o m minus V o p minus V ref p minus V ref m, and V o m minus V o p is nothing but...

Student: V offset by

V offset by times A by A plus 1, so the differential voltages after the autozero phase is done, the difference between the two preamp inputs, is therefore V s p plus V o m minus V ref p minus V s m plus V o p minus V ref m.

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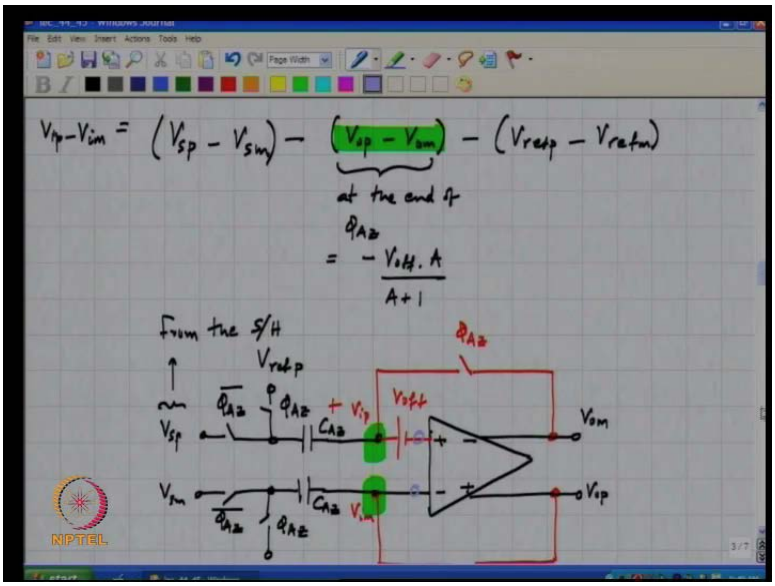


Which is given by V s p minus V s m minus V o p

Student: Minus V o m

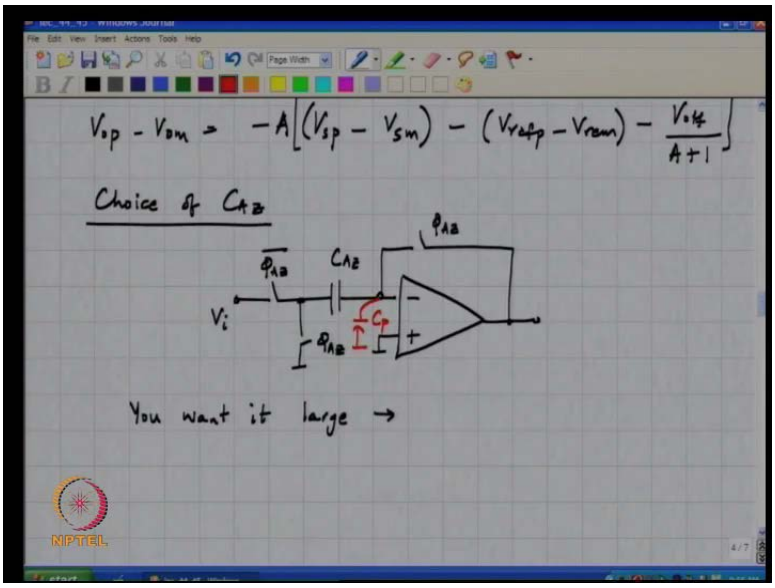
Minus V o m minus V ref p minus V ref m, so V o p minus V o m is nothing but...

Student: ((Refer Time: 38:17))

Please note that, this V o p minus V o m refers to the output of the preamp at the end of the auto zero phase, and is therefore equal to minus V offset times A by A plus 1, so this is V I p minus V I m ((Refer Time: 39:22)). So, the difference between those two nodes please note that the this node here, is a fictitious node it is not really available to us, so the difference between this node and this node, will therefore be...

Student: ((Refer Time: 40:16))

(Refer Slide Time: 40:27)



So, which means that the output of the preamplifier will be V o p minus V o m is nothing but, V s p minus V s m which is the differential input minus the differential reference minus V offset by A plus 1. Because, the difference between these two voltages was V s p minus V s m minus V ref p minus V ref m plus V offset times A by A plus 1, now you have minus V offset, so the residual offset is only V offset by A plus 1. This is exactly analogous to what was there in the single ended case, so the preamp has effectively made two contributions.

One the large gain has resulted in an effective reduction of the offset of the latch by this factor, then the capacitors which were used to hold the offset, can also be used to store the references. So, subtraction of the reference is also a very straight forward effect, you understand; now couple of things, now can you tell me which of these switches you will turn off first. So, there are switches in the reference path and there are switches in the feedback path based on the reasoning we had earlier, which do you think you want to turn off first now.

Student: Feedback

The

Student: Feedback

The feedback and why does that make sense

Student: ((Refer Time: 42:44))

So, if you go across the entire flats array clearly V ref p and V ref m are changing, all the way from negative full scale to positive full scale. Now, if we turn off the reference path switches first, the charge injection will not be the same, the difference in charge will be proportional to V ref p minus V ref m. So, as you go from the lowest comparator all the way to the top most comparator, since the charge injection is now dependent in some non-linear fashion on V ref p minus V ref m.

You will find that the references, which are stored on these auto zero capacitors are corrupted by some non-linear error. On the other hand, if you open the feedback path switches first, you will find that the charge injected is virtually the same, because we assume that V offset is a small quantity. And the charge injection is, therefore even though is different is very small and is not a problem, the next thing I want to bring you attention, is that...

Student: Sir

Yes

Student: ((Refer Time: 44:20))

So, this will be multiplied by minus a I believe, does it make sense, so the preamp is amplifying the difference between a differential input, and a differential reference causing the output to build up hopefully to a large voltage, which is enough to overcome the offset of the latch. The next thing I want to bring to your attention is the following, what do you think we should choose these capacitances to be should there be very large, can there be very small, and why do you think it must be by chosen to be large.

Student: It must be it has to be large, because any leakage or any charge, any leakage current at the input of the amplifier ((Refer Time: 46:58))

So, again let us go back to the single ended version just for convenience, to understand the principles involved, in order to be able to make an in form decision on the size of the auto zero capacitor. So, you want to make it large and why is that, what do the advantage of choosing a larger capacitance.

Student: Linear samplings are noise and it should be moving to

[FL]

Student: ((Refer Time: 46:59))

So, one thing that he mentions is the following, please note that the amplifier will have some input parasitic is it not, so let us call this C p, now what is the effect of C p.

Student: Because, there is a capacitance your signal will get attenuated, so

And during which phase is C p problematic

Student: Phi A Z bar

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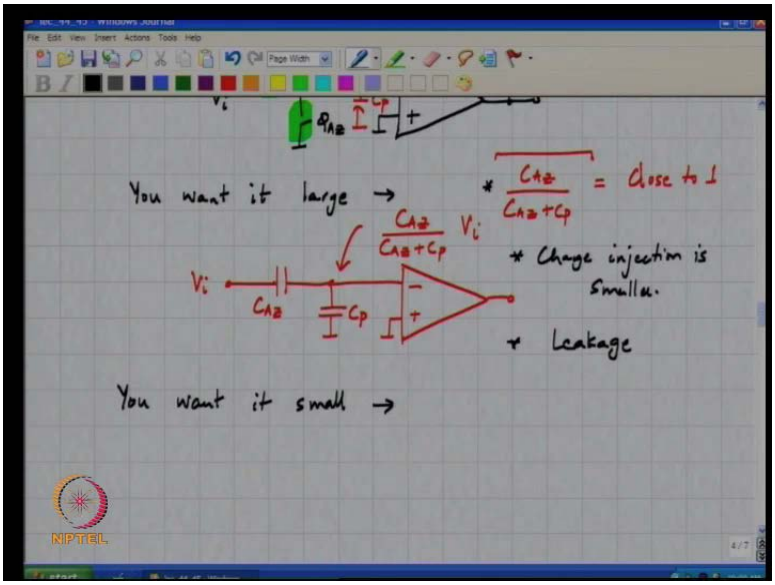

So, during the amplify phase the effective circuit looks like this, so this is C A Z, this is C p and this is the preamp, and this is V i, so what is this voltage, so this is nothing but, C A Z by C A Z plus C p times V i. And is therefore...

Student: C A Z should be much much greater than C p

In order to not attenuate the input signal, if you attenuate the input signal it is basically like having a smaller gain in the.

Student: Amplifier

Amplifier is it not, so you want it large, so that this factor C A Z by C A Z plus C p is close to 1, are there any other reasons why you would want C A Z to be large.

Student: ((Refer Time: 48:52))

Please note that all these switches are MOS switches, and all MOS devices have leakage due to A junction, the source bulk and the drain bulk junctions after all are reverse bias diodes. So, they will have small, but I mean finite leakage currents, so if you take very small capacitor stuff is likely to leak away, but do you think this is a real problem, I mean if this has to really effective. I mean what time scales are we interested in, sure what I am trying to say is that, if you take this capacitor charge it up and then, you come back tomorrow obviously, there is no not going to be any charge left on the capacitor. But, are you going to come back tomorrow or what?

Student: ((Refer Time: 50:00))

So, how long do you want this charge to be held on the capacitor accurately

Student: I mean it is down force to the clock period

Until the next time you do an auto zero, so if we decide to do an auto zero every cycle, then leakage is really not a big issue, so this is one reason why you would want to make C A Z large. Another reason least important reason is leakage, and just like leakage there is also charge injection, which is a lot more fundamental problem, and if you try to make these switches which will dump charge, so charge injection is smaller.

One could argue that in this particular case, that we have shown a single ended system charge injection is a problem, however fully differential system charge injection appears as a common mode error, so it is not likely to be a big problem either. So, the main reason for even attempting to have a large autozero capacitor, is simply the attenuation due to the input parasitic capacitance of the preamp. So, why would you want to have small is other any reasons, or are there any advantages to using a small autozero capacitor clearly making C p, C A Z too small, will result in the C A Z by C A Z plus C p to be much smaller than 1.

Therefore, there are I mean you do not want C A Z to be too small and of course, all charge injection effects will simply become lot more severe, when C A Z is small. And

leakage as he pointed out also becomes problem, but is there any advantage you think off using a small C A Z

Student: Speed

Speed of what

Student: No on the other phase charging V ref p V ref m, they have to charge these capacitors

V ref p and

Student: V ref m, they have to charge these capacitors

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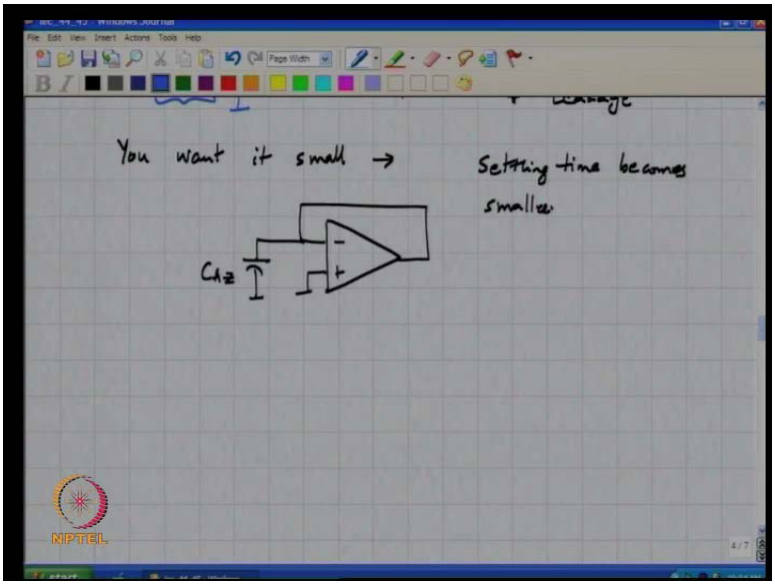

During the autozero phase, please note that the equivalent circuit is this, so the amplifier has to drive a load equal to C A Z, so if C A Z becomes too large, what happens?

Student: ((Refer Time: 53:14))

I mean to in order to be able to settled, please note that we only have a duration equal to phi A Z, during that time the voltage across the capacitor must settled to V offset times A by A plus 1 you understand. And that in any amplifier if you go and increase capacitance it will be slower, for the same voice and current if you want to drive a larger capacitance,

it means that it will take a longer time to drive it. So, settling time becomes larger and therefore, the only advantage you want it small, because settling time become smaller.

So, the only advantage to choosing a small capacitance is that, the autozero can happen quicker you understand, so like in everything else you neither want to make C A Z too small, which will cause significant attenuation of the input during the amplify phase. Now, do you want to make it too large, if you make it too large the attenuation problem goes away, however the time taken for the offset voltage to settle on to the capacitor becomes very very large.

And there is also a third effect which is not fundamental, it turns out that any capacitor you make will also have a parasitic capacitance called the bottom plate capacitance. So, one of these plates of the autozero capacitor will have a parasitic, which is say a percentage of C A Z. So, this is let me just take this is to be 10 percent of C A Z as an illustration, now if you go on increasing C A Z, with the hope that this attenuating factor C A Z by C A Z plus C p becomes closer and closer and closer to unity, we find that this will also increase.

And this parasitic capacitance directly comes as a load the sample, and hold you understand, so the trade off , therefore are you do not want C A Z to be so small that, the input is attenuated too much you do not want it to be so large that, it is bottom plate parasitic. And becomes a big burden on the previous stage, and because of the large C A Z the...

Student: Settling

Settling time in the autozero phase becomes very large, so will continue in the next class.