VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 43
Offset in a Latch - 2 Autozeroing

This is VLSI Data Conversion Circuits, lecture 43. In the last class, we were discussing various mechanisms by which the latch can give a wrong decision , of course systematic problems are once like hysteresis, which we have learnt to fix using a reset phase phi 3. Towards the end of last class, we saw that random mismatch between transistors, can also cause errors in the decision, because static mismatch in the transistors, which form the main regenerative pair as well as mismatches in the switches.

And the parasitic capacitances at x and y equivalently appear, as if you are not comparing V x and V y, but some V x minus, some delta v 1 and V y minus delta v 2, so it is an error in the threshold of the latch.

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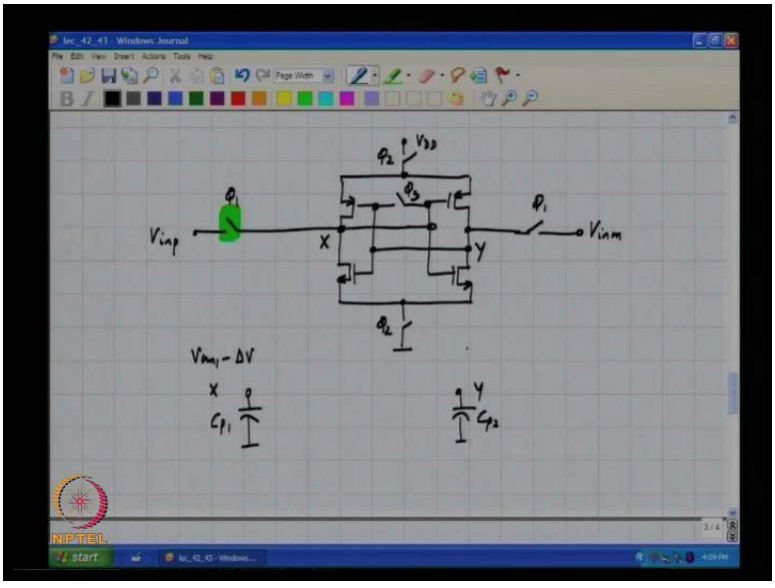

Another important mechanism is what is called dynamic offset, and the mechanism that causes it just follows, so this is our standard latch we have been discussing so far. And just at the end of phi 1. If the voltages on capacitors C p 1 and C p 2 at x and y were slightly different, for example let us say this is V c m 1 minus delta v and this is V c m 1 plus delta v.

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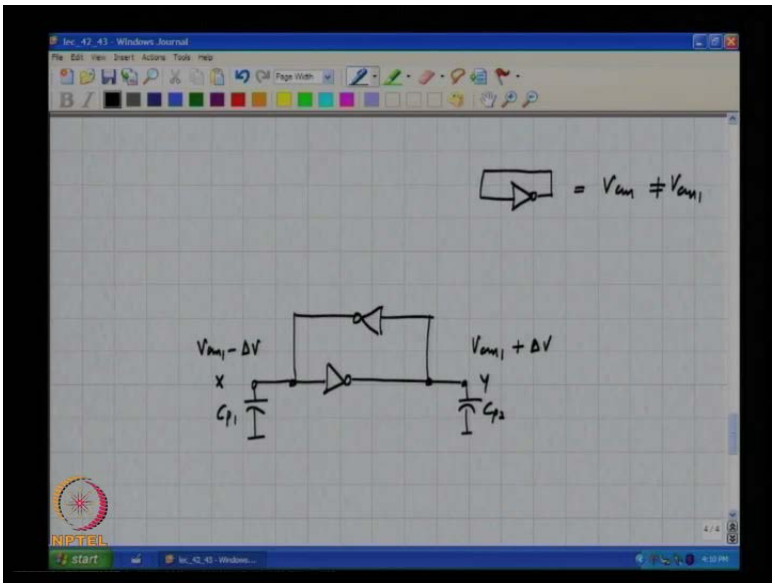

And let us say the inverters have a natural trip point, and what do you mean by the natural trip point of the inverter, it is that input voltage for which the n MOS and the p MOS currents are the same. Let us say the natural trip point of this inverter is V c m, which is not equal to V c m of 1, now what do you think will happen in the very beginning.

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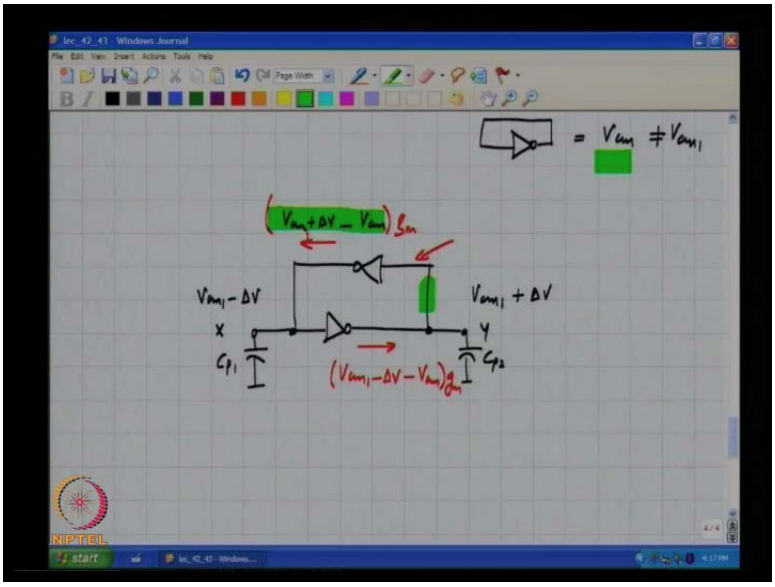

So, at the end of phi 1, these inverters circled in green are not yet turned on, so the initial conditions on C p 1 and C p 2 are V c m minus delta v and V c m plus delta v, the

moment the inverters turn on, what do you think happens, If V c m 1 was exactly equal to the trip point V c m what happens.

Student: ((Refer Time: 04:03))

The currents that each inverter would pump would be, I mean g m times delta v and g m times delta v in right directions. Now, what happens, if you apply let us think about it carefully, the initial voltage at this node as soon as the inverters are turned on is basically V c m 1 plus delta v, but the trip point of this inverter is V c m. So, to a first degree what does the current that is being supplied or pushed out by this inverter.

Student: ((Refer Time: 05:06))

It is V c m 1 plus delta V minus

Student: V c m

V c m times some trans conductance g m of the inverter is this clear, similarly this let us call this going this way, this current then will be V c m 1 minus delta v minus V c m times g m. So, for small delta v, which is what is of serious concern for us because the latch is most likely to make an error when the two inputs are very close to each other. So, what is the big departure from the previous situation, if V c m 1 was exactly the same as V c m, then if one inverter is pushing current in this direction, the other one is pushing current in the other direction.

Whereas, now in other words the current outputs of the two inverters was purely differential however, if the trip points of the inverter are different from the two initial voltages to which C p 1 and C p 2 would be charged, what do we see there is indeed a difference in the currents which is still equal to 2 g m into delta v however, there is also a...

Student: Common mode

Common mode component, and what is that common mode component trying to do

Student: ((Refer Time: 07:12))

It is trying to bring V c m 1 towards

Student: V c m

V c m and how do you see that

Student: ((Refer Time: 07:22))

To determine how this common mode potential is moving, what do we do, we draw the common mode equivalent circuit and what is the common mode equivalent circuit.

Student: ((Refer Time: 07:56))

So, we need to short to find the common mode response, in this is a common mode and all this only make sense when things are linear, in the very beginning of the degeneration phase we hope that things are still linear. Because, the input is very small and we are just looking at around the time, when the phase phi 2 goes high, so as far as common mode signals are concerned we see that, the common mode impedance at nodes x and y is a very small number.

In other words this back to back inverter chain is attempting to, of course regenerate the difference, but also at the same time trying to bring the common mode to V c m of the, which is the trip point of the inverters, does it make sense. And I mean, another way of seeing it is that, you can see that the current flowing here has got a common mode component, which is proportional to the difference between V c m 1. And is pulling it in a direction, so as to bring both of them close to each other.

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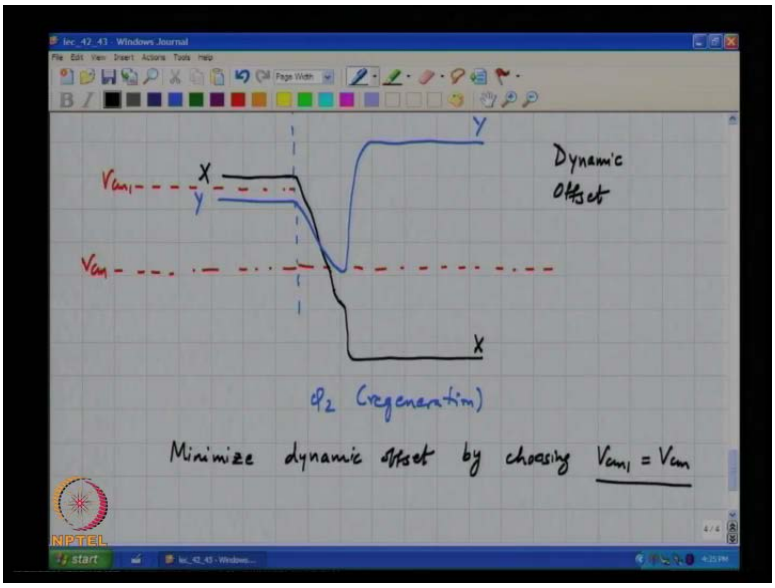

So, if you plot the wave forms at x and y these two were slightly different to begin with, and this is phi 2 or regeneration begins what do you think will happen in the, what do you expect to happen to the common mode, this was what is V c m, this is V c m 1, let us say this, on the other hand is V c m which is the trip point of the inverter. W hat do you think will happen.

Student: ((Refer Time: 10:35))

The common mode will attempt to go from

Student: V c m

V c m 1 to V c m in a very very

Student: Short

Short time corresponding to the time constant, which again depends on the g m of the inverters, and at the same time the differential mode degeneration is also attempting to happen. Now, the common mode going, so what you would think would happen would be that, this would attempt to do something like this, this on the other hand node x would attempt to do something like this ((Refer Time: 11:30)). This way you can see that the differential mode is increasing, the common mode is also moving towards V c m.

And beyond this the common mode does not change, because it is close to the trip point of the inverter and then, regeneration takes over, the regeneration becomes very strong and perhaps does something like this. Unfortunately in practice what happens is that, the two capacitors C p 1 and C p 2 are not only mismatched, they are also non-linear. So, it will turn out that during this time, if the input difference is sufficiently small, what will happen is that by the time the common mode moves to the natural common mode of the inverters, which is V c m.

An interaction between mismatch, and non-linear capacitance at V x and V y will cause the upper voltage to go below the lower voltage and then, regeneration takes over and you get n l. So, in one of your exercises you will actually be asked to plot all these wave forms, and see this for yourself, the mechanism actually is somewhat settle and difficult to rigorously analyze. But, it is possible to rigorously analyze mathematically, but you often end up with a messy more as of equations, but the key point is to understand that the problem is appearing, because of the difference between.

Student: V c m and V c m 1

V c m and V c m 1, the natural threshold of the inverters and the common mode of the differential input voltages stored on V x and V y, is what is responsible for this offset, which is called dynamic offset. All these diagrams of course, are grossly exaggerated and greatly simplified, when we actually look at real wave forms they will be a whole bunch of glitches and all these wave forms, corresponding to charge injection all this stuff. And every time a clock changes through the overlap capacitance of the switch transistors, you will find that they will be a component of the clock getting onto all these wave forms.

So, in order to understand this carefully, you need to take a very, very careful look at all the potentials, in that early part of phi 2, you understand. But, as I said I mean more than analyzing this, it is sufficient to recognize that this is a problem, and the solution is quite straight forward as you can see, what does the solution.

Student: ((Refer Time: 16:21))

So, the best bet to minimizing dynamic offset by choosing V c m 1 equal to V c m, so this should also tell you why, it make sense to short that to two nodes x and y together, during the reset phase phi 3, rather than connecting them up to a common potential

namely V D D. Connecting those regenerating nodes to V D D is something, which is done in a fair number of latches, and latches like this will be proven to a lot of dynamic offset. Simply because, during the initial part of the regeneration phase, the common mode of those two nodes will have to come down from.

Student: V D D

V D D all the way to V c m, which will can cause a the difference between nodes x and y to reverse sign and then, by the time regeneration takes over and stuff, it is too late because, the error has already been made. So, this is a good strategy to choose and often simulations of dynamic offset are done using Monte Carlo type analysis, where you put in device and process mismatch, and keep putting in signals which are straddling the threshold.

If you put too large in input difference, the output decision will indeed be correct, all these problems will only happen when the input is very small and that, therefore you need to run a whole bunch of simulations. Where you randomly vary the thresholds as well as the parasitic sizes to get a good estimate of what this random mismatch due to, whatever dynamic offset due to random mismatch, which will include both effects of you know nonlinearity of the capacitances, as well as mismatch between them are taken into account.

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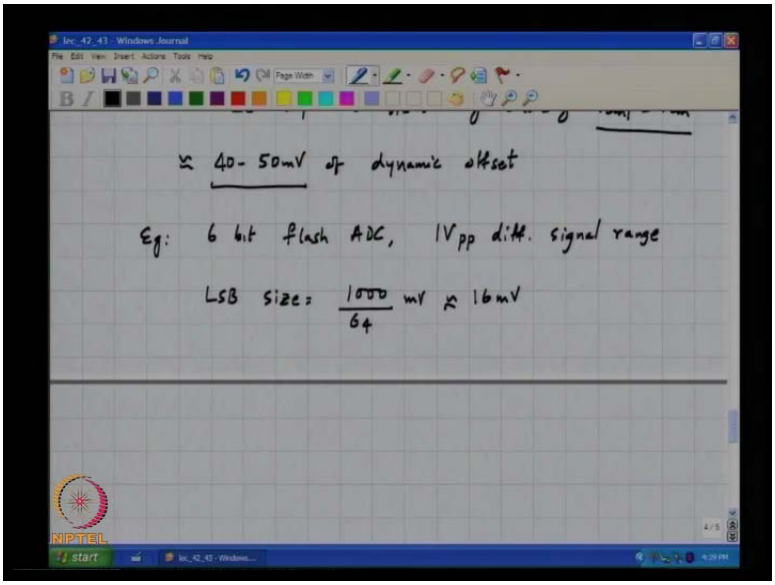

So, typical numbers to go by are about 40 to 50 millivolts of dynamic offset, a rough estimates and as I said Monte Carlo simulations are the best way to estimate, the true dynamic offset. Or rather true offset which will include contributions from both static, as well as dynamic paths, is this clear. Now, the question is what does one do, if one has such a large dynamic offset, let us say we trying to build a 6 bit flash ADC with a 1 volt peak to peak differential signal range, what is the LSB size?

Student: ((Refer Time: 20:50))

It is 1000 millivolts divided by 64 which is about 16 millivolts, so if the offset of the latch itself is 40 to 50 millivolts, that is almost like 3 to 3 and a half LSB of the converter that you are trying to build.

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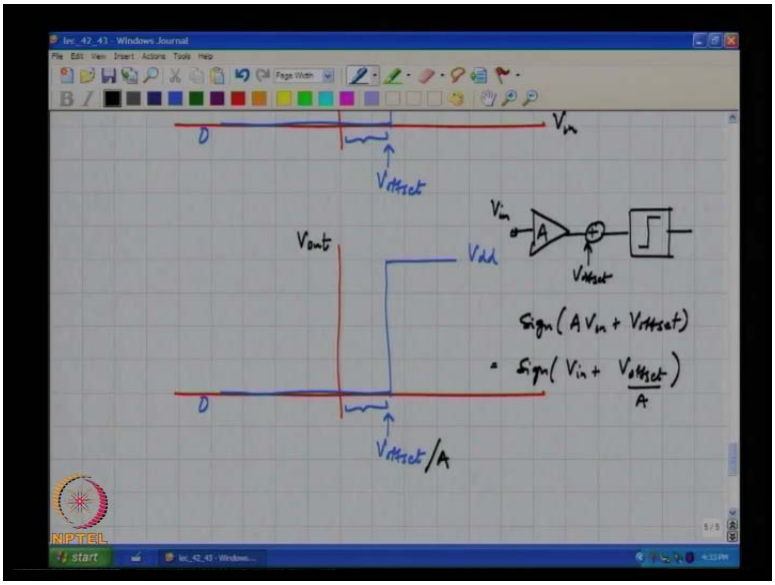

So, in other words the latch while it gives you, if you have sufficient time gives you gives you a characteristic which looks like, a signum function this is V d d, this is ground, this is V offset and this is a random quantity, which consists of static and dynamic components. And this offset as we can see from our discussion, can be much larger than LSB of the converter that we are trying to build.

Now, the question is what do we do about this, how do you think we can fix this problem, clearly the latch has such has a decision levels which are in error by too large in amount. So, what do you think you can do, ideally what do you want this signum to be.

Student: ((Refer Time: 22:56))

I mean you want this transition to be at 0, or if there is a variation in the threshold it must be centered around 0, and must be so small, that the DNL and INL of the converter are not drastically effected. So, what do you think you can do to reduce the effect of offset, in other words let us see this is V in, and this is V out correct this is the characteristic we have, what we want is something where this is much smaller. So, let us say we want this, where this offset is now being reduced by a large factor A, so what do you think you can do.

Student: ((Refer Time: 24:15))

[FL]

Student: ((Refer Time: 24:18))

If you want to take this characteristic and move the trip point from V offset to V offset by A, what do you think you can do?

Student: ((Refer Time: 24:38))

Yes, the input should be

Student: Amplify

So, in other words what you should do is, not use this latch as is this thing has got some offset, if you put an amplifier here with a gain A then, and the if this is V in what happens.

Student: ((Refer Time: 25:23))

So, the actual input going into the latch is A times V in plus V offset, so the latch is giving us sign of A times V in plus V offset, which is equivalent to sign of V in plus V offset by... So, this amplifier again I am just taking the liberty of drawing single handed diagrams.

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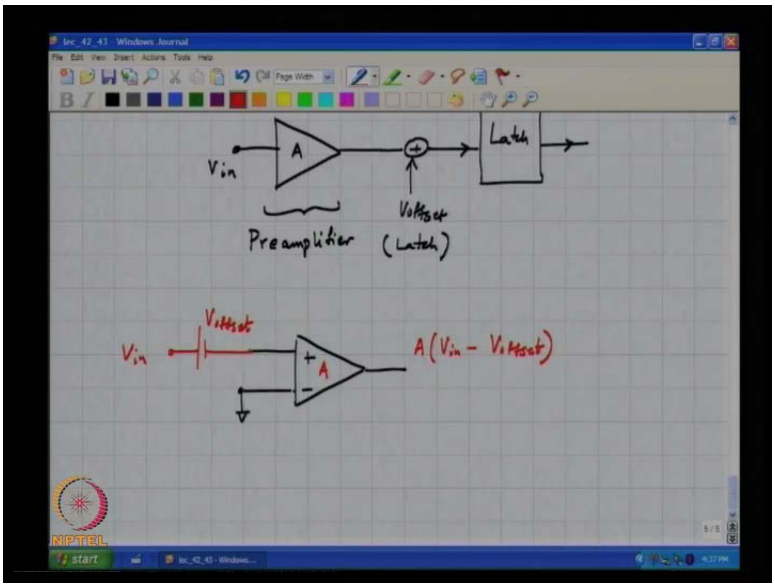

But, this is the latch offset, this is called the preamplifier and ideally what must be the gain of the preamplifier, ideally we would like to be like it to be infinite and thereby reduce the offset of the latch, when referred to the input of the preamp to 0. In practice of course, the preamp will have finite gain and the effective reduction in the latch offset will be only by this factor A. Now, what do you think is the problem with adding a preamp.

Student: ((Refer Time: 27:52))

So, it is not quite fair to assume that, there is mismatch in the latch and there is no mismatch in the preamp. So, if devices are mismatched they mismatched everywhere which means that, it is very likely that the preamp whose job is to take the input voltage and multiply it by a large factor, it does not just give you A times V in, it adds it is own offset. So, now you try to solve the problem of the latch by adding a preamp, now it does not help if the preamp itself has got offset, you understand.

So, in other words while this is a schematic a more for instance, this is the preamp and let us say this goes to the latch with all it is additional baggage, namely if the switches phi 1, phi 2, phi 3 and all that stuff. So, we do not worry about that for the time being, our job now is to try and figure out what to do with the offset of the preamp itself, in other words the preamp has got an offset, which is the output voltage, is actually A times V in minus V offset.

Now, the question is what do we do to fix this issue of preamp offset, and please note that ((Refer Time: 30:25)) this is your preamp, you cannot say why do not you apply the input here; it seems like the most obvious solution, but the bottom line is that offset is not accessible.

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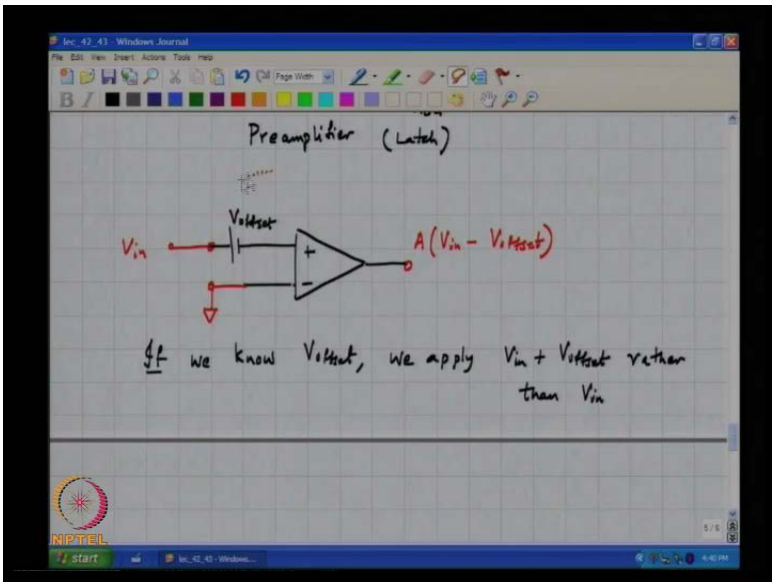

Now, let us see what we can do, I just to make sure that there is no confusion let me draw the offset also in black, so the accessible terminals are all drawn in red. And the unaccessible part is drawn in black, what whoever can be think about, and what ideas can we come up with which will enable us to either eliminate or.

Student: Reduce

Reduce the offset

Student: ((Refer Time: 31:33))

[FL]

Student: Whatever the offset is there, ((Refer Time: 31:36))

There are you can think about in several ways, but the basic idea seems to be like, if we know V offset, then instead of applying V in to the preamp we will apply V in plus V offset to the preamp rather than V in, is it not. So, now the question is how do we know or how do we get to know what V offset is, any suggestions in principle what will we do.

Let me rephrase, let me draw this again, how will we know V offset, we have an amplifier with some offset in it, how will we figure it out.

Student: Apply the 0 input voltage

Apply 0 input voltage

Student: ((Refer Time: 33:21))

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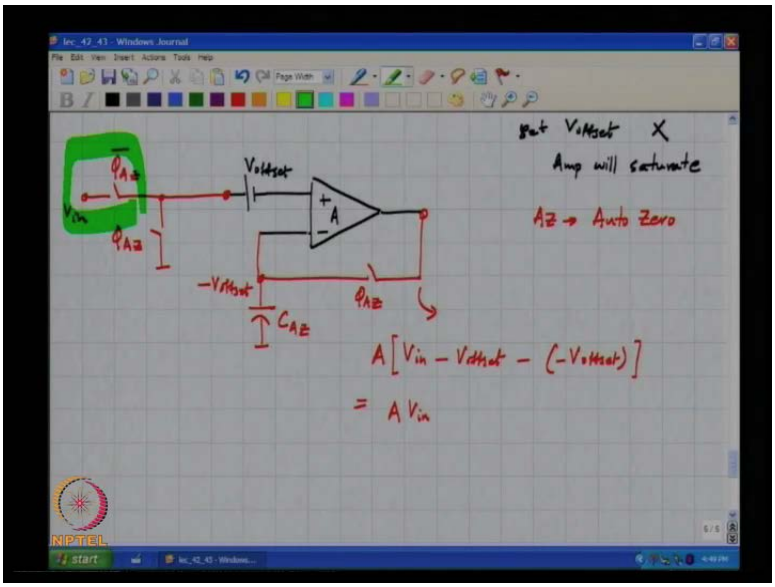

Let us say the first idea is to say, this has got a large gain A, why do not I apply V in equal to 0 and therefore, the output voltage must be minus A times V offset. And from this hopefully knowledge of A and knowledge of V offset, from the knowledge of A we should be able to get V offset, what do you think is the problem with this. A secondary concern is what it points out, which is getting knowing a properly is not an easy task, especially when A is very large, what is the more serious problem.

The more serious problem is that, if A is very large just imagine this triangle to be an opamp for instance, you seen that the output voltage of the opamp is always either going to be either ground or V d d. Because, the gain is so high, that it will saturate the internal nodes of the amplifier, so apply V in is 0 measure V out get V, from which you get V offset is not a good idea, because amp will saturate. I mean think about this as I have an op-amp with an input referred offset, and I want to find what that offset is, what will you do.

Student: ((Refer Time: 35:27))

So, from your basic opamp classes, you take the op-amp and you put it in

Student: Unity

Unity feedback and what will be the output

Student: ((Refer Time: 35:42))

This output will be, please check carefully it is minus V offset, does it make sense, but then if you put the opamp in unity gain feedback, you have minus V offset developed at the output of the opamp, then what you need to do.

Student: We need to subtract it accurately

We need to store this quantity and subtract it from

Student: ((Refer Time: 36:28))

Subtract it from the input voltage source, so how do you store an analog voltage

Student: Capacitor

On a capacitor, so I would say and please note, that it is not good enough to simply connect this to ground always, or to close this feedback loop always. Because, after we have done with estimating offset and hopefully fixing it, we want the amplifier to apply with a large gain, you understand. So, in other words these lines drawn in red must only be active during that period, during which we are estimating and storing the offset.

So, in other words let us call this phase phi A Z, the strange choice of clock name A Z stands for auto 0, and as the trade name given to any technique, which removes offset, offset cancellation is also called auto zeroing. Because, in the old days when there was an offset in the amplifier you have some kind of potential potentiometer control, you would look at the output and go and turn something, and the output would go to 0. This is called zeroing the output of the opamp or of the amplifier, now this all done automatically, so presumably this you can call this auto 0.

So, during when phi A Z goes high, the positive input terminal of the amplifier of the preamp should be connected to ground, you should enable the unity gain feedback path around the amplifier phi A Z. And what happens at the output of the amplifier, the voltage that is developed is.

Student: ((Refer Time: 38:55))

Can be stored on a capacitor, so where do you think you can put the capacitor, one way of doing this is to say I am going to have a capacitor here. And what happens to this voltage now, what is the voltage at the end of phi A Z, what is the voltage across C A Z minus V offset. And then, if you say during phi A Z bar the input is applied, what will be the output voltage V in minus V offset, minus of minus V offset times A, so this gives A into V in.

I mean another alternate way of doing this is to say, during it is not necessary as you can see to attach V in here one can also, what else do you think you can put V in and still get A times V in say for a sign.

Student: ((Refer Time: 41:19))

So, another alternate we are doing this, yet to say not I am going to short this to ground, and during phi A Z bar, and apply the input during phi A Z, I am going to connect this to ground. And during phi A Z bar I am going to connect this to V in, and one immediate thing that comes to mind is that, this node is connected to ground all the times, there is no need for the switches. You can connect this to ground all the time, and this will be this voltage will, therefore be V in.

Student: ((Refer Time: 42:43))

V in minus V offset, and the output voltage will be minus V offset minus V in minus V offset times A, which is A times minus V in, is this clear. So, one obvious question that comes is, I mean why would I want to do this, is there any special reason for doing this, rather than this ((Refer Time: 44:07)) any thoughts. Basically the offset cancellation is the same in both cases, the only difference is where the input is applied, so what topologically different thing do you notice here, versus here.

Student: ((Refer Time: 44:53))

I mean of course, this inverting, but can you see a fundamental difference between the two

Student: ((Refer Time: 45:20))

As far as offset cancellation is concerned, as far as estimating offset is concerned in fact, if I remove the input, one crucial difference between both these schematics is that, this node is always connected to ground, in the later case. Whereas, here that is not true, you understand, so it turns out then when we try and make this fully differential, why we interested in making it fully differential. The flash A to D converter we are going to build will be something which compares a differential input, against differential references, do you understand what I am saying.

The input as we discussed a few classes back on a analog mix signal chip, it always make sense for the input to be fully differential, because lot of common mode disturbances can be eliminated. Then the definition of a flash converter becomes, instead of comparing a single ended input with a single ended reference, a differential input is compared with differential reference. Which means that, the latches which have to be differential as we have already, I mean we have already discussed differential latches.

And it also means, therefore that the input to the preamp is not going to be single ended it is going to be differential. And it turns out as I will discuss in the next class, that it is very straight forward to convert a single ended schematic like this, where the positive terminal of the amplifier is grounded to a differential circuit configuration than a schematic like this ((Refer Time: 47:25)).

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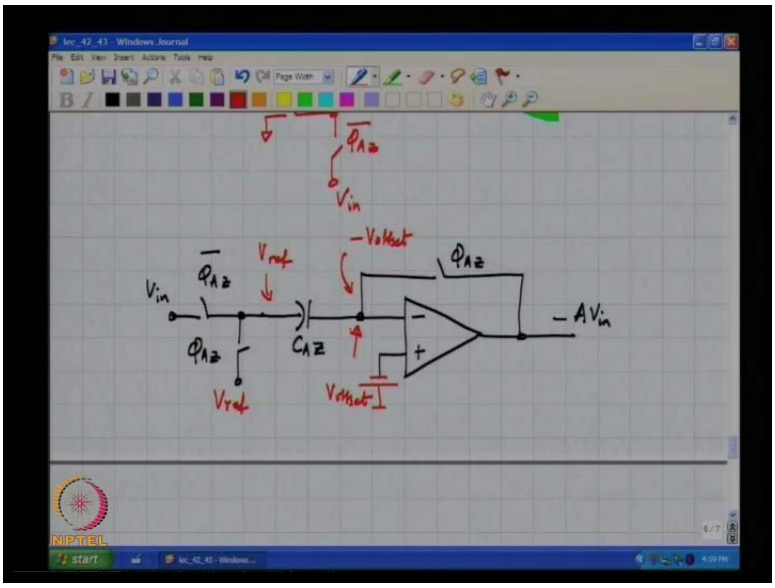

So, the way this schematic is the basic idea is drawn, can be redrawn in the following way, C A Z this is phi A Z, this is phi A Z, this is V this is ground, this is V in, this is phi A Z bar, this is just redrawing the whole schematic in a slightly different way, but it is indeed the same thing the gain is negative. So, this is an inverting amplifier and the output voltage will be minus a times V in, so notice that this capacitor C A Z is basically acting like a battery, which holds the offset.

We also need to subtract references, so what do you suggest we could do, please note that this is acting like a C A Z is simply acting like a battery, which stores the offset. If you want to subtract a reference, in principle what you must do is connect in series with V in another battery, which stores the reference. Now, the question is we already have one battery which stores the offset, can you use the same capacitor to also store the reference, so any suggestions.

Student: ((Refer Time: 50:14))

Very good, so the observation is that A, during the auto 0 phase this plate of the capacitor is getting charged to minus V offset, because what did we assume our offset was like this ((Refer Time: 50:40)). So, the observation is instead of simply grounding this plate of the capacitor, if this was connected to some reference V ref. Then the voltage across this capacitor will be V ref plus V offset V ref plus, so this plate will be at

V ref, the other plate will be at minus V offset. So, the effective voltage drop across the capacitor will be V ref plus V offset.

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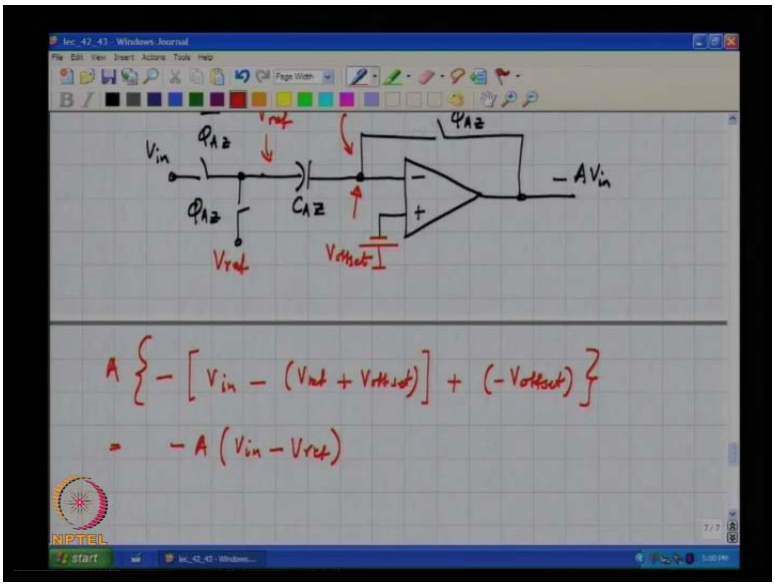

So, the voltage at the negative terminal of the amplifier will be V in minus

Student: ((Refer Time: 51:40))

V ref plus V offset, this is the negative terminal of the amplifier, the positive terminal is at minus V offset and this is getting multiplied by A, and this will be minus A times V in minus V ref. So, the offset storage capacitor can also be used to store the reference, of course, one thing that none of you caught is that, the output voltage will V equal to V offset. I mean during the auto 0 phase for instance here, this switch is shorted and this is grounded, this output is going to be minus V offset only if A is infinity.

In practice it is not quite infinity, so if the output voltage would be slightly smaller than minus V offset in magnitude, and so we will still be making an error in the, we are estimating V offset which is slightly in error. So, when you subtract also we will be not compensating for the entire offset, but only a large part of it. So, in the next class we will see what the error is and how one goes and designs the preamp; and more importantly how one makes the preamp differential.