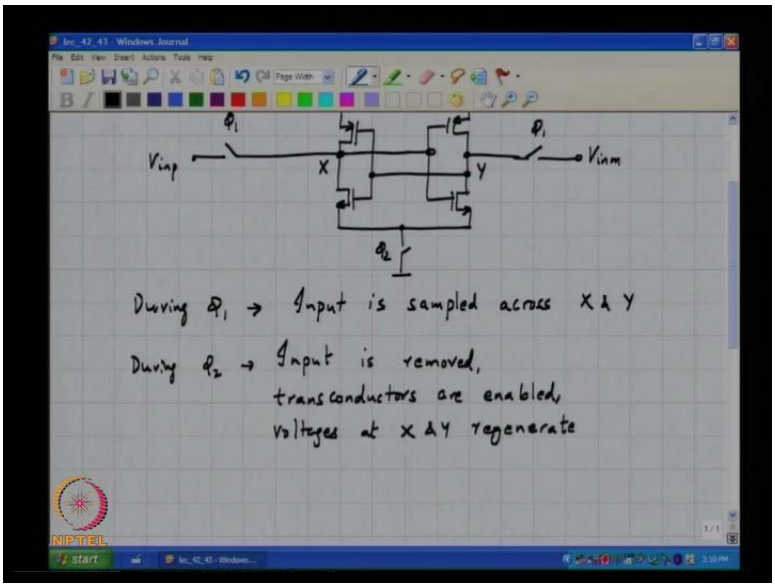
VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 42
Offset in a Latch – 1

This is VSLI data conversion circuits lecture 42, in the last class we were looking at, how one can build a comparator, namely a contraction which can take two input voltages and tell us, which one is larger. In principle, this is the basic build in block, if you want to compare something against the reference, what we need to do is, take the input subtract the reference and give that result to, whatever animal can take can tell us, which of the two inputs is larger.

(Refer Slide Time: 00:46)



And the basic idea behind a comparator was, as we saw last time, two trans conductors connected back to back and the trans conductors were implemented as C MOS inverters. So, during phi 1 what happens...

Student: Sampled

The input is sampled across X and Y and that basically means that, it is held on the parasitic capacitance at nodes X and Y. We did not want to put a deliberate capacitance there, because that will simply reduce the speed of the circuit. In the sense that, it will increase the regenerative time constant, there by making the output not sufficiently large

enough for the next levels of logic to be able to resolve it, as a logical 1 or a logical 0 within a given amount of time.

So, during phi 1, the input is sampled and held on the parasitic capacitance is at X and Y and during that time, it is important to make sure that, these trans conductors are not...

Student: attempted

Are not active, so phi 2 and phi 1 are non overlapping block phases and during phi 2, input is removed, trans conductors are enabled and voltages at X and Y regenerate. And if the input is sufficiently large at the end of phi 2, the voltages at X and Y are practically...

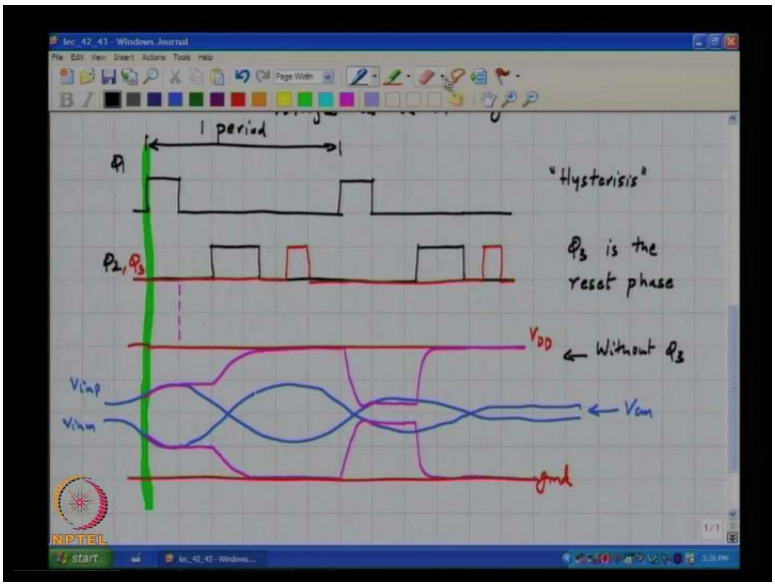
Student: Regenerate

The supply and...

Student: ground

Ground.

(Refer Slide Time: 04:27)



So, if we look at the timing diagram, let us say this is phi 1, I am just grossly exaggerating times here, especially the non overlap intervals. So that, the things are visible clearly, so this is phi 1, this is phi 2 and this is one period of the clock. So, if you

look at the nodes, let me call these rails V D D and ground, which is the sampling instant and at what instant are the inputs sampled.

Student: Falling edge of phi

Input sampled on the falling edge of phi 1, the way we have it and so, let us assume that the input is changing. So that, let us say this is the input, one input this is V in p and V in m is something like this, as you can see, both these wave forms are varying about a common mode V c m. Usually it is kind of advantageous to choose this common mode at V D D by 2, although this is not strictly necessary. So, we had like to plot the potentials at nodes X and Y,y let us start at the very beginning.

So, at this let us start plotting these waveforms at the rising edge of phi 1, so node X follows V in p until the following the falling edge of phi 1. Similarly, node Y follows V in m until the falling edge of phi 1, what happens when both phi 1 and phi 2 are low...

Student: Hold

The voltage is across I mean, on nodes X and node Y are in principle held, in practice of course, when the switch is open, there will be some charge injection and the voltages will be held, but they will not be the same as...

Student: ((Refer Time: 07:43))

Those held at I mean, just before the falling edge of phi 1, but this is just time to give you an initiative understanding of what one must expect. Then, phi 2 turns on and at this point, the inverters are or the trans conductors are active, because the inductors are turned on and what happens?

Student: ((Refer Time: 08:10))

Regeneration sets in and in principle, what are we expected to see at the output?

Student: ((Refer Time: 08:18))

What do you think will happen to the difference between the potentials at node X and Y?

Student: ((Refer Time: 08:22))

It will exponentially increase and beyond a certain point, the inverters will saturate and therefore, the potentials will go to?

Student: V D D...

V D D and ground and these are held all the way upto the next rising edge of phi 1, where again the inputs follow V in p and V in m are held and continued to be held at V D D and curve, does it make sense. So, the sampling instant is this and can you comment on, why this happens, why is there a finite rise time there?

Student: Measure over the memory.

So, the two parasitic capacitances on nodes X and Y, have just before phi 1 goes high are sitting at V D D and ground depending on, what the sign of the previous input was. Now, because of finite output impedance of the source and the resistance of the switches in series, the nodes are not able to track the input instantly. So, they need some time and during that time, what is happening, the prior memory of the nodes X and Y is being discharged through the equivalent series resistance looking back from these parasitic capacitances.

And at the same time, the sources is trying to charge these parasitic capacitances to the...

Student: Input

Input value, now as we were discussing the last time around, if the time phi 1 is not large enough and what is the meaning of large enough?

Student: It is the timing...

It is the timing, if the time constant of the series resistance and the parasitic capacitance is not sufficiently small compared to the width of phi 1 then, the discharge process of the previous decision is not complete. The fact that the present input voltage is not charged completely is only a minor issue, because if the input varying sufficiently slowly. And if the time is not enough all that it means is that, instead of the voltage across X and Y reaching V in p minus V in m times 1 minus e to the minus t by some time constant tau.

Instead of reaching V in p minus V in m, it will reach V in p minus V in m multiplied by some factor, which is smaller than unity, because it is 1 minus e to the minus t by tau.

But, the key point is to note that, the sign of the voltage across X and Y still correct right, however if the previous decision is not been discharged what will happen is that, that undischarged part of the previous decision acts like...

Student: ((Refer Time: 12:30))

An additional input apart from the actual input, whose sign we trying to determine, this can lead to errors if the previous decision is...

Student: ((Refer Time: 12:45))

Is different from the decision we would have correctly made during this clock cycle, however because of this memory from the past, it will appear as if the present input has the wrong sign or rather the sign of the present input is determine incorrectly and this is especially crucial when the differential input is very very...

Student: Small

Small, if the differential input is large, it does not matter because, that the previous decision would have decayed to some degree. And as long as the input is larger than that, you are still ok, but otherwise you end up making an error, so this is called hysteresis. And this is where, the latch remembers it is past decision and that can introduce error, now what do you think we can do to fix this problem?

Student: ((Refer Time: 14:11))

Pardon.

Student: ((Refer Time: 14:14))

One obvious thing to say is that, the problem is coming because of the finite time constant, if I reduce the time constant...

Student: ((Refer Time: 14:25))

I will be able to solve this problem, one way of reducing the time constant is to say, I will try and make the source impedance that is driving the latch have a very low output resistance. Now, do you think this is practical thing, now what is this cost?

Student: ((Refer Time: 14:47))

Basically if you want to reduce the Thevenin resistance looking back from the latch, if you want to reduce it by a factor of ((Refer time: 15:00)), it is it is like taking two identical circuits and putting them in...

Student: Parallel

Parallel and that simply means, double the participation, so while it is true that reducing the time constant is what you want to do, implementing it by actually making the time constant of the I mean, the Thevenin output resistance of the driving source smaller is not a practical idea. So, what do you think you can do...

Student: It seem to be curve like

Pardon.

Student: ((Refer Time: 15:29))

One other suggestion is try and increase the width of phi 1, not phi 2, increasing phi 2 is only make sure that, you regenerate better. So, that will only increase the gain, but it is during phi 1 that you made the error, so increasing phi 2 does not help as far as avoiding hysteresis course. So, increasing phi 1 is also a valid solution, however if you have only so much time to complete the whole process, if I try and increase phi 1 it means that, you decrease something else, most likely phi 2 which means that, now you have made no error. But, you do not have enough gain either and this lead to metastability problems, what else.

Student: Initiates to 0

Pardon.

Student: Initiates to it 0

Meaning what?

Student: ((Refer Time: 16:28))

So, the next suggestion is the key point to notice is that, what we are trying to get rid of

is the previous decision on...

Student: ((Refer Time: 16:43))

X and Y, and in other words, we need to clear whatever memory the parasitic nodes had from the previous decision and that must be done...

Student: ((Refer Time: 17:00))

When?

Student: ((Refer Time: 17:02))

This must be done before...

Student: Phi 1

Phi 1, so one way of doing it, again there are many ways to doing this, is to use an extra clock between...

Student: ((Refer Time: 17:20))

When should this extra phase be there?

Student: ((Refer Time: 17:25))

This is...

Student: ((Refer Time: 17:34))

This phase must be there after phi 2 is fallen and...

Student: Phi 1...

Before phi 1 goes high and let me draw that phase is, let me call this phi 3 and during this phase, what are we supposed to do?

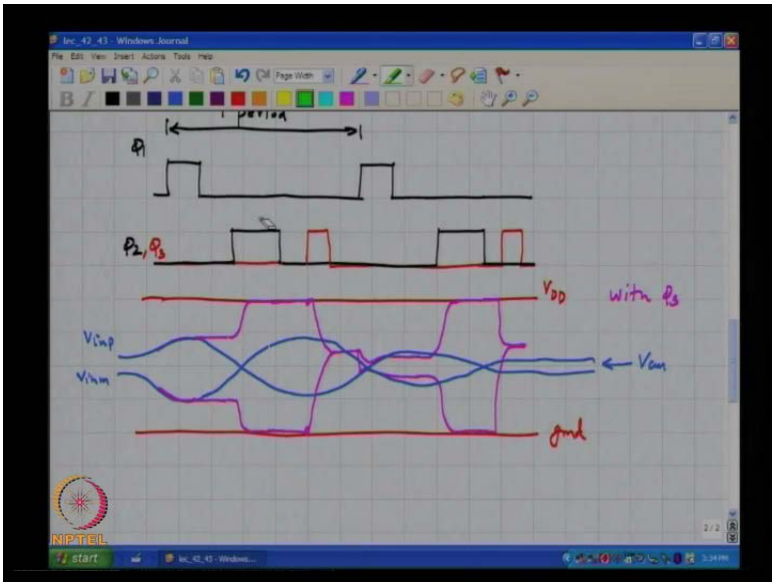
Student: ((Refer Time: 18:22))

We need to make X and Y forget their past which means that...

Student: ((Refer Time: 18:27))

One is simple way of doing it is to keep X and Y to the same potentials and rather than try and hook them up to a third potential, one way of doing this is to simply short X and Y using a third switch. So for example, a switch like this, so phi 3 is the so called reset phase, where in principle, what is being done is to clear the internal nodes of the latch of any remnants of the previous decision, now how will the wave forms look like.

(Refer Slide Time: 20:01)



Let me, so this is wave forms without phi 3, with phi 3 what we will do now, what is the difference. So, upto phi 2, things are the same, after phi 2 what happens, upto this point, that is, until phi 3 goes high things are ok, when phi 3 goes high what happens...

Student: ((Refer Time: 20:59))

Portal discharge to...

Student: Same potential

The same potential and what might that potential be...

Student: ((Refer Time: 21:10))

I mean, A good approximation is to say V D D by 2 is strictly not correct, because the two capacitances are, it is quite true that they are equal. But, on the other hand, they are non linear. So, if you take two non linear capacitors, one charge to V 1 and the other one charge to V 2 and you short them, it is not necessarily V 1 plus V 2 by...

Student: 2

2.

Student: No, on top of it, it would be the inverter, it will be of two invertors, which are connected back to back.

But, the inverters are the disabled.

So, all that you have is two parasitic capacitances, these are not linear, so it is not strictly correct to say that, the output voltage will go to the, that common voltage will be V V D D by 2, but it will be close. So, during phi 3, the waveform will look like this and during phi 1, again it will continue like this until it reaches the rising edge of phi 1, where then one of the wave forms will track phi 1. The other one will track phi V in p, the other one will track V in m and similarly...

Student: ((Refer Time: 23:41))

Yes.

Student: ((Refer Time: 23:43))

Yes, it is actually that is a good point, yes what I intended to show was, during phi 2, it is indeed rising exponential, I am going to correct this , here 2. So, this is with phi 3 and you can see that, resetting the latch is one way of eliminating hysteresis. So, you would ideally like to have as much time for phi 2 as possible, phi 2 is the phase during which regeneration takes place. So, if you want to be able to resolve the lowest possible input, the gain must be the largest which means that, of the clock period you have, you must try and allocate as much as possible to...

Student: Phi 2

Phi 2, the regenerative phase. And unfortunately, there are several considerations that prevent you from making phi 2 equal to almost the entire period. Because, as I said earlier, one issue that you need to worry about is the tracking of the, the input must be properly sampled on to...

Student: Phi 2

Onto...

Student: Phi

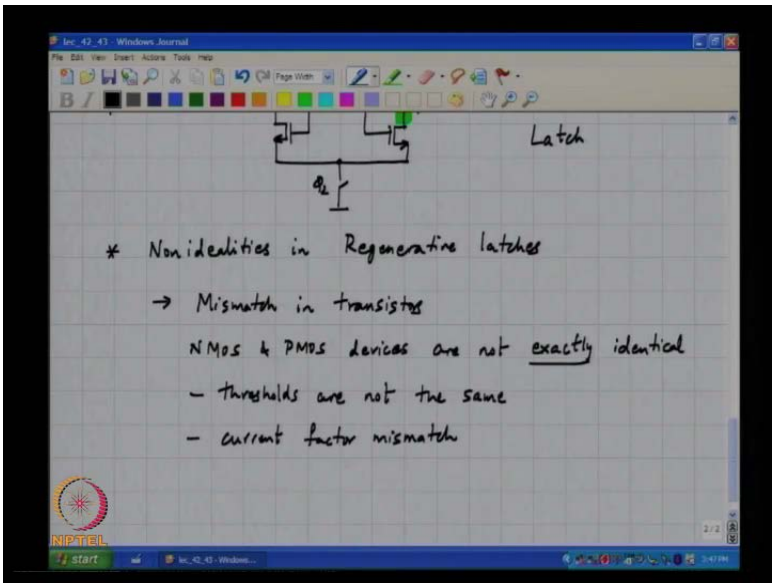
Nodes X and Y, there must be some safety margins for non overlap times and there must be some finite time for phi 3, you understand. So, typically phi 3 can be very small or just enough to make sure that, the previous decision has been removed to large degree and the over non overlaps must in a chosen. So that, across process variations and stuff, the wave forms phi 1, phi 2 and phi 3, still remain non overlapping and rest of it can be left for phi 2.

Now, the next thing to worry about is, the decision we are interested in is the logical value of nodes X and Y when...

Student: After regeneration takes place

So, what we need to do is, around this time, it is not just enough to regenerate and keep quite. We need to be able to capture that digital logic decision somewhere so that, the latch can get ready for the next set of inputs.

(Refer Slide Time: 27:52)



So, in other words, one needs to sample nodes X and Y and that is done for instance, there are many ways to doing this of course. But, this can be a waveform phi 2 delayed multiplied by phi 2 for instance, will give you a waveform phi 2 and phi 2 will be some

waveform, which looks like this. Again as I said, there are many ways of generating these wave forms, I am just giving you a, where you just want to generate a high, you want to capture the node voltages at X and Y after they have regenerated sufficiently so that, their outputs are valid logic levels.

And these outputs are captured on the parasitic capacitance of these inverters and this is also a storage element, however it is not a regenerative one. There is no harm in having a regenerative storage device following the basic latch, since we have put inverters, the outputs are out m and out p as I have shown. So, this is one way of doing a circuit or a designing a circuit, which will tell us, whether V in p is greater than V in m or vice versa. Now, we need to worry about, what all can go wrong here I mean, such a circuit is called a latch or a regenerative latch.

So, non idealities in regenerative and since there are any number of ways of realizing a trans conductor and there are any number of ways of disabling one, it does follows that, there are any number of latches out there in the literature, each one of them is got it is own pros and cons. This particular latch I have shown here, is something that we have used quite extensively and works quite nicely. The disadvantage with this is that, it requires a whole bunch of clock phases, which may or may not be easy to do.

If you are dealing with low frequency converters then, it is quite straight forward to partition a large clock period into a whole bunch of different phases and a portion different amounts of time to each of these phases at will. However, as speeds become higher and higher, generating these clocks and maintaining their integrity as far as queue is concerned, over when you propagate them across the chip, is not a trivial task. And many latches, which are out there in the literature, basically try and play around with different phases to try and accomplish the basic same objectives.

In one phase, you are tracking, the other phase you are regenerating, in some cases it may be possible to combine phi 3 and phi 1 or you may not be able to do separate phi 3. So, you just say, I am going to just have only phi 1 and take the hit that comes as far as hysteresis is concerned. I mean, that is the practical solution when you have absolutely no way of generating a third phase reliably so that, it goes an resets the two parasitic capacitances X and y.

But, otherwise the basic principle are the same I mean, one of you could argue for

instance that, differential trans conductor, why you use to C MOS inverters, one could have used a differential pair and how do you turn off a differential pair?

Student: By cutting of the tail current

You just cutoff the tail current that the pair is dead, so turning on and off the pair is one way of making the trans conductor come up or down. So, if you follow that line of thought, you will come up with a circuit topology, which looks very different from what we have shown here. So, the aim of this exercise is just to show you that, the reason why some of these transistors are there and the basic principles of operation. And the issue is that, one commonly comes across when your designing a latch.

The issues will be there, the basic issues we talked about are not circuit specific, finally we are trying to capture the input on two parasitic capacitors, we are trying to use to trans conductors to regenerate. At the end of the regeneration phase, those two parasitic capacitance will obviously contain voltages, which are one which is close to the upper rail or one which is a logical 1 and one which is logical 0. The next time around you need to able to, ideally you would like to be able to discharge or clear these parasitic nodes of memory from their previous decisions and move on.

So, if you go and dig through a whole bunch of latches, you will find that the basic principles are the same. One common way of clearing memory is to not, for instance use I mean, short the two nodes together, in some circuits it becomes convenient to actually connect those nodes to either V D D or...

Student: Ground

Ground, that is also an another way of resetting memory, both of them are now connected to the same potential. And usually, one also finds that, there is a trade of between, how what do you call, how easy is to generate these clocks and the performance of the circuit. I mean, this circuit for instance, in principal cleans up hysteresis and have, but unfortunately has three phases, the other circuits where the clock phasing is much simpler, there may be only one phase and it is complement, which may or may not be non overlapping with the other.

However, the internal nodes may be reset to V D D or ground rather than to mid rail and

as we will see going forward, that can be a problem in the latch, specially for very small inputs. So, latches which are very complicated from a clocking point of view, have some attractive properties, but by their very nature, you have to propagate many clocks or locally generate some clocks from the other, which of course messes up layout and makes a latch, little bigger than it needs to be.

On the other hand, the performance is usually quite nice, now let us take a look at non idealities in these regenerative latches. The things that can go wrong are the following I mean, what is the meaning of latch can go wrong I mean, what can be wrong about a latch.

Student: ((Refer Time: 38:02))

The voltages may not regenerate to logic levels, that is not really a non ideality in the sense that, the time constant is what it is given a certain technology. So, there is hardly any point is saying, I have this very slow technology and I want to regenerate in half a clock period, that is just not going to have happen. So, is not really a non ideality in that sense, we accept that fact even when the technology is given I mean, if there will an latch is making a mistake, what does it mean?

Student: wrong sign

It is giving you the wrong sign and that can happen, one of the main culprits behind that is mismatch. So, the N MOS and P MOS devices are not exactly identical and their two aspects, in which they are mismatched, one is thresholds are not the same. In other words, two identical MOS transistors place next to each other on the same ((Refer Time: 39:57)) are ideally supposed to have the same threshold, because they are gone through the same manufacturing process.

In practice however, random dopant fluctuations and random changes in oxide thickness and random everything causes the thresholds to...

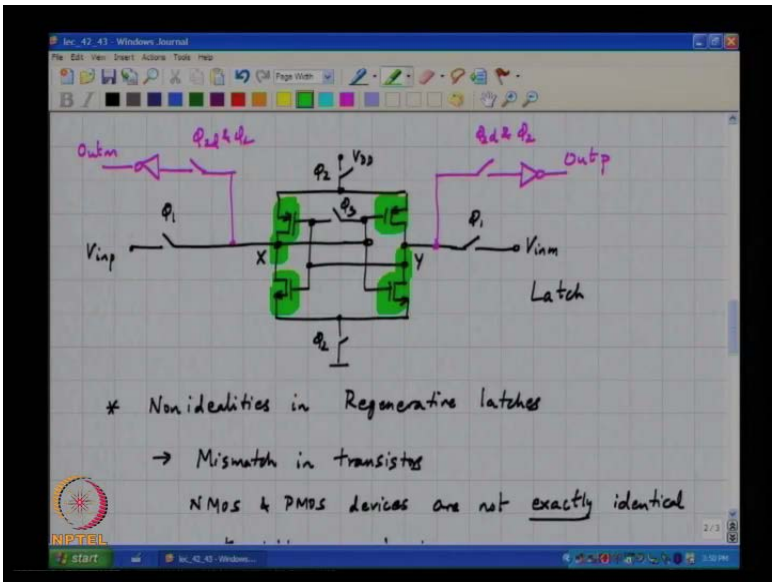
Student: ((Refer Time: 40:11))

Differ from...

Student: one another

One another, so yet another problem is current factor mismatch, this is where at mu N c ox or mu p c ox W by L s slightly different for different transistors lying on the same ((Refer Time: 40:39)). In your analog IC's class, I trust you have you understand the statistics of mismatch.

(Refer Slide Time: 40:52)



So, the V T mismatch is governed by some parameter called the sigma V T, which is given by...

Student: A V T...

A V T divided by...

Student: Square root W L

Square root of W L and beta mismatch, which is also the current factor mismatch is sigma beta or delta beta by beta is some sigma naught divided by square root of W L and this 1 by square root W L dependence make sense, why?

Student: ((Refer Time: 41:48))

Pardon.

Student: ((Refer Time: 41:52))

If very I mean, 1 by square root W L dependence means that, if there is more area, there is less mismatch, but I am asking why it make sense?

Student: ((Refer Time: 42:01))

So, let us say I take two identical transistors and put them in parallel, the threshold is basically, what is a threshold of this composite transistor?

Student: ((Refer Time: 42:22))

Yes, two identical devices with slightly different thresholds...

Student: ((Refer Time: 42:28))

It will be the...

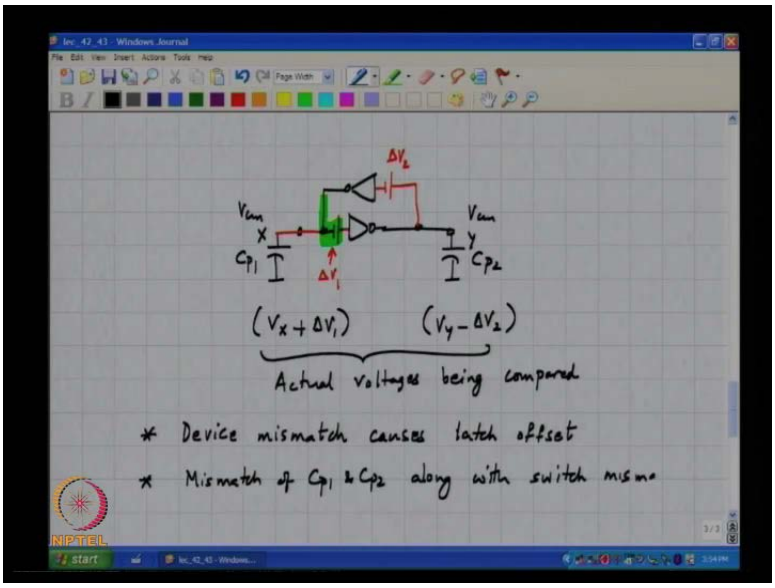
Student: Minimum

Average of the two, not the minimum, so that delta V T is very small then, you can model the changes in current as g m times delta V T 1 plus g m times delta V T 2 when you refer that back to the input, it is delta V T 1 by 2 plus delta V T 2 by 2. So, the standard deviation must go down by a factor of...

Student: ((Refer Time: 42:54))

By root 2, if you take two identical transistors and put them in parallel, the sigma V T must go down by a factor of root 2. So, these the statistic make sense, now if these transistors are mismatched, it appears like you have offset, even though there is none, you understand.

(Refer Slide Time: 43:37)



So, ideally let us kind of examine the behavior of the latch, when these two potentials are exactly equal to V c n, if these two potentials were exactly the same and there was absolutely no mismatch, what would you expect these two voltages to do...

Student: Remain at same

You would expect them to remain...

Student: same

At the same potential forever, but now and why is that happening, because the inverters are both, this V c m as we said, is exactly the trip point of the two inverters, in which case this inverter is producing no current and the other inverter it is brother, is also producing nothing. So, between the two of them, then make sure that, X nor Y N 1 of them move. Now, on the other hand, if there was a offset in the device thresholds, what does that mean, it is like having a battery in series with this inverter and an another battery in series with the input of this inverter.

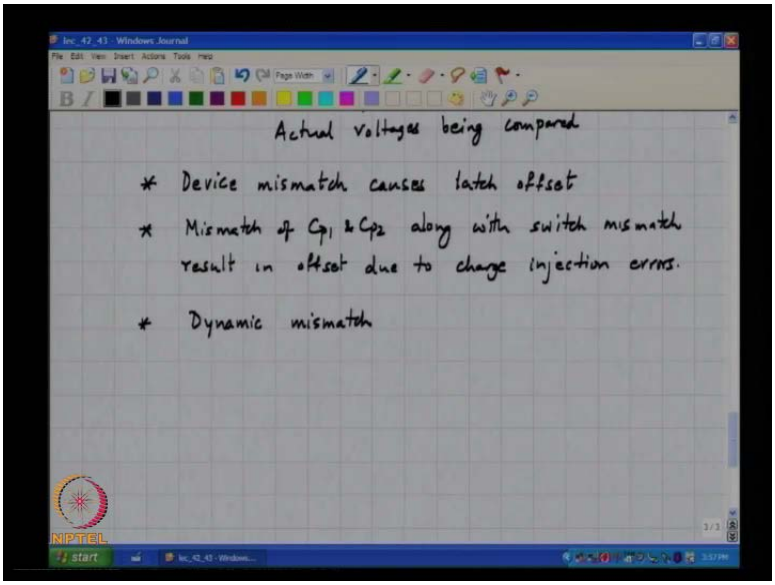
These are random voltages delta V 1 and delta V 2, which depend on the threshold mismatch between the N MOS and the P MOS transistors. So, what is this equivalent to, this is equivalent to, you can push the node, this voltage source through the nodes and it is like saying, instead of having sensing the difference between V x and V y, you sensing the difference between V x...

Student: ((Refer Time: 46:06))

Plus delta V 1 and V y minus delta V 2, so these are the actual voltages being compared, so what was the moral of the story, device mismatch causes latch offset. Another thing that we need to be aware of is that, the parasitic capacitances are also mismatched. So, this capacitance c p 1 and this capacitance c p 2, which are nominally supposed to be identical are not quite as identical as we had like them to be.

Now, this is got a couple of effects, please recall that, when you turn of the switches or turn switches on, charge is being either injected on to parasitic drained source nodes or taken from these parasitic nodes. So, in combination with the mismatch of c p 1 and c p 2 along with switch size mismatch, switch mismatch let us say, result in offset due to charge injection errors.

(Refer Slide Time: 48:19)



Ideally, at least when all the switches are identical and with both the capacitance are identical, the same amount of charge must be at dumped on both the capacitors, which will cause the common mode to jump up, but differential mode remains...

Student: The same.

The same, so it should not lead to any offset, in practice the switches will be slightly off due to device mismatch, threshold mismatch there will cause different amounts of charge to get injected then c p 1 and c p 2 will be different themselves. So, the voltages that are

developed across c p 1 and c p 2 due to these charges will also be different, so all these things cause offset. A third important mechanism, which causes offset is, what is called dynamic mismatch and has got to do with the way, the latch behaves at the time the regeneration turns on.

It is a not quite straight forward thing to see, but it turns out that, dynamic mismatch is often the dominant factor of the whole mismatch calculation. And usually, it is not straight forward to estimate simply from a hand calculation, one has to sit and do a fair amount of complicated math to figure this out. Fortunately, there is a solution to fix the problem and we will see, what this is and how to fix it in the next class.