VLSI Data Conversion Circuits
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Lecture - 41
Latches and Metastability

This is VLSI data conversion circuits lecture 41, in the last class we saw a top level view of how one would make a practical flash A to D converter, and the key building block in the converter is the comparator array, which means that we have to learn how to make a comparator. So, the basic idea behind a comparator as we saw was to detect, whether an input is greater than a reference or not, so let us try and explore some approaches, in a circuit approaches that will potentially make this possible to keep things simple.

We first start with the simplest possible reference mainly 0, in other words we would like to figure out, if some analog voltage.

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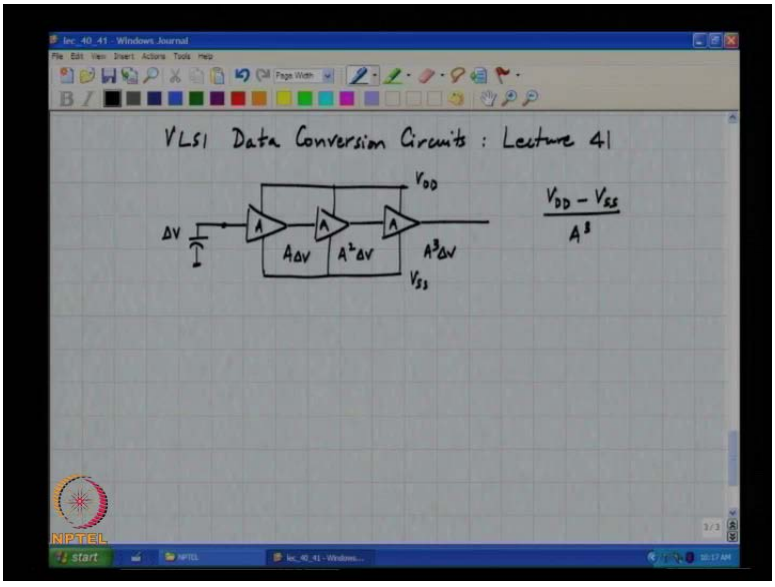

Say stored on a capacitor is greater than 0 or less than 0 aain we want to make a ((Refer Time: 01:12)) what we are interested in only, we are not really interested in the absolute value of the voltage, and we just want to figure out if it is greater than 0 or smaller than 0. So, what do you think one could do what is the simplest thing that you could.

Student: Op amp ((Refer Time: 01:29))

So, you know one of these one thing that suggest itself based on our experience, you say I am going to go on putting amplifiers in cascade like this, and as this delta v keeps going through this chain of amplifiers. You know here it will be a times delta v, a square times delta v, a cube times delta v and so on, eventually these amplifiers which are running of supply voltages, positive and negative will eventually saturate.

So, in this particular example if there are 3 amplifiers, the output voltage if delta v is sufficiently large will reach a logical level, which is either VDD or VSS. Because, these amplifies presume only cannot go on producing output voltages, which exceed the supply voltage, but clearly we see that there is definitely a range of inputs which will fail to produce a.

Student: A either ((Refer Time: 03:12))

Which will fail to produce

Student: VDD or VSS.

Either VDD or VSS, which are or you know voltages close to that which are recognised logic levels, so what is the minimum voltage you can resolve.

Student: Negative

Student: Negative

So, the if you assume that the logic levels you want are VDD and VSS, the resolvable input range consist of voltages which are beyond VDD minus VSS by.

Student: A cube

A cube, so this is the smallest resolvable input, and in order to increase the resolving capacity, what do you think one can do

Student: Increasing

Student: Increasing

You go on increasing put more and more and more amplifiers in cascade. So, please note that the linear range of these amplifiers are is hardly a concern, we are not interested in making these linear amplifiers at all. We are only interested in raw gain, and why we are only interested in raw gain, we are the characteristic we are trying to realise is very non-linear, it is a we are trying to realise an ideal signum function.

So, there is no point in trying to make each of these amplifiers linear, and of course as always you be interested in trying to do this with as efficient realisation is possible from both hardware and power point of view. Another way which is probably not very apparent at first sight is to say I have a capacitor with a voltage delta v.

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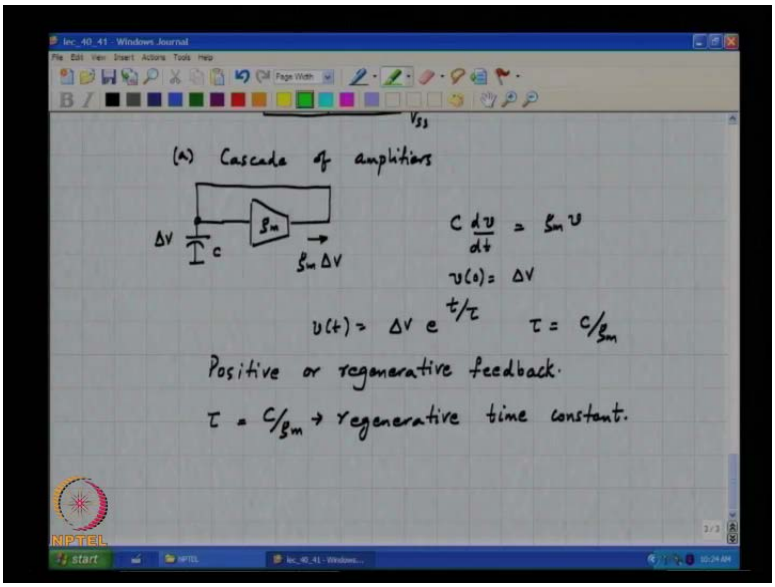

So, this earlier approach is the cascade of the amplifiers approach, and please note that even though we have said this is a cube b in practice, every amplifier will have finite bandwidth. So, this a cube b will appear after sometime, which corresponds to the delay, so to speak of this amplifier chain. Now, yet another way of trying to figure out, whether this delta v is greater than 0 or less than 0, is to you know is to say that following, if this voltage is greater than 0, I will attempt to make it, I will attempt to increase it.

If this voltage is less than 0, I will attempt to decrease it, so as time keeps going along, if it was greater than 0, it will keep going up and up and up. Hopefully, eventually hitting the rail, and similarly if delta v is smaller than 0 it will keep becoming more and more and more, negative eventually hitting the…

Student: Negative range

Negative range, so this way after sufficient amount of time is elapsed the output is either.

Student: V D D

Either V D D or

Student: V S S

V S S. So, it is like in India rich keep getting the richer and the poor keep getting poorer, so how do you, now push this node voltage up if delta v is greater than 0, what I mean if you want to push node voltage up what should you do.

Student: Put push current

You want to put push current in, but that current must be dependent on.

Student: Maximum delta v

On delta v

Student: Delta v

So, if delta v is positive you want to push current into the node if delta v is negative, you want to push current.

Student: Out of a node

Out of the node, so basically what you want to do, therefore is to have a current source, which is controlled by delta v, let us call this clearly a voltage control current source. So, if delta v is positive this current is g m times delta v this way, and what should I do.

Student: Feed it back.

I should go and feed it back like this, you understand, so what would be this voltage is a function of time if we started off with this v of T initially, let us call this C, C d v d T is nothing but, g m times.

Student: V

V with v of 0 being equal to delta v, so is the first order differential equation or if you think of this as a system it is a it is a single pole system, and where is the pole located.

Student: G m by c

Student: G m by c

G m by c, but where I mean where in the Laplace plane is this.

Student: Right

Student: Right half of

It is in the

Student: Right

Right half, so this is actually an

Student: Unstable

Student: Unstable

Unstable system, so v of t therefore, is delta v times e to the

Student: G in by c

Student: G in by c

Plus t by tau, where tau is nothing but, c by g in. So, what kind of to clearly there is a feedback here, what kind of feedback is this.

Student: Positive

Student: Positive

Positive feedback, because if we break the loop and come back, the I mean the response at the other end of the loop is in the same direction as the excitation. So, this is positive feedback or often called regenerative feedback, and tau is called the regenerative time constant is make sense. Now, what we will do is apart from figuring out how to realise

this with transistors, we will have to observe that again in practice this g m is going to be powered half of some supplies.

So, even though in principle the output voltage should go to infinity, in practice it will be limited either to the positive real of the negative real. So, a from hardware complexity point of view, this is a very simple structure where we use positive feedback to obtain gain. Whereas, the cascade of amplifiers would have required a whole bunch of amplifiers to do this, you understand and linearity etcetera, are not really important all that we need to do is figure out if the input is less than 0 or greater than 0. So, this is an ideal candidate for doing this, and if you want to have more gain, what does this mean how will you get more gain.

Student: ((refer time: 12:17))

Student: Gain

I mean the gain of this contraction

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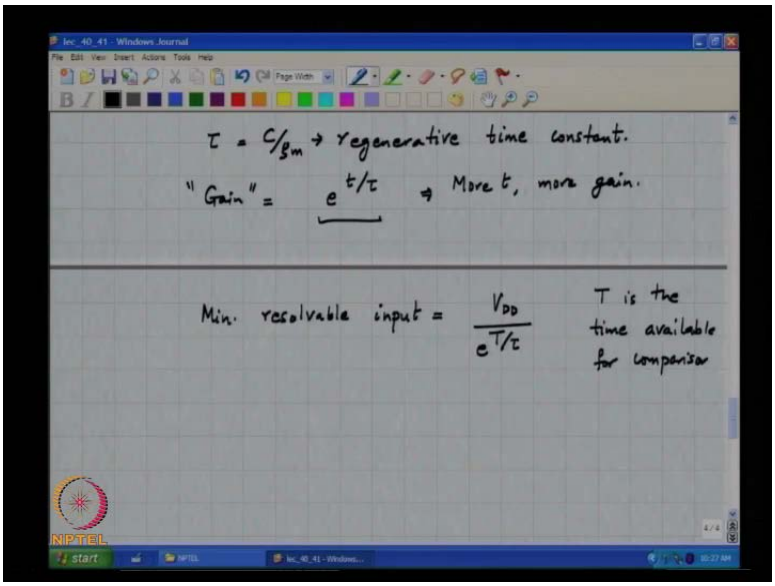

If you can call it that is basically e to the t by

Student: Tau

Student: Tau, the is the degenerative gain that you get in a period tau. So, one straight forward way of increasing the gain

Student: Is to wait

Student: Is to wait

Is to wait long enough

Student: ((Refer Time: 12:51))

That is all, so more t means more gain. Of course, most of the time you do not have the luxury of saying, I am going to wait for 2 days for this to give my decision. So, in practice what happens is that you are the amount of gain, you have is limited to the amount of time you can wait for. In a flash converter for instance the comparator array has to make a decision within a finite amount of time, that time cannot exceed one clock cycle, because the array has to get ready for the next input.

In the worst case therefore, or rather in the best case for the comparator array, one can say I am going to take the entire clock period to make a decision. And then in that you know that infinitesimally it is small time before the next input comes, I am going to do you know prepare myself for the next input, which is as you can see a stretch, but at least in principle, there you know that there is a finite amount of time before, which you need to make a decision. So, if that time is taken to be t the minimum resolvable input is the time taken to reach a logic level, divided by the gain as usual.

So, that is nothing but, say VDD divided by the gain which is e to the capital T by tau, where T is the time available for comparison does make sense, so let us say this is the time available capital T, and let us say this is VDD.

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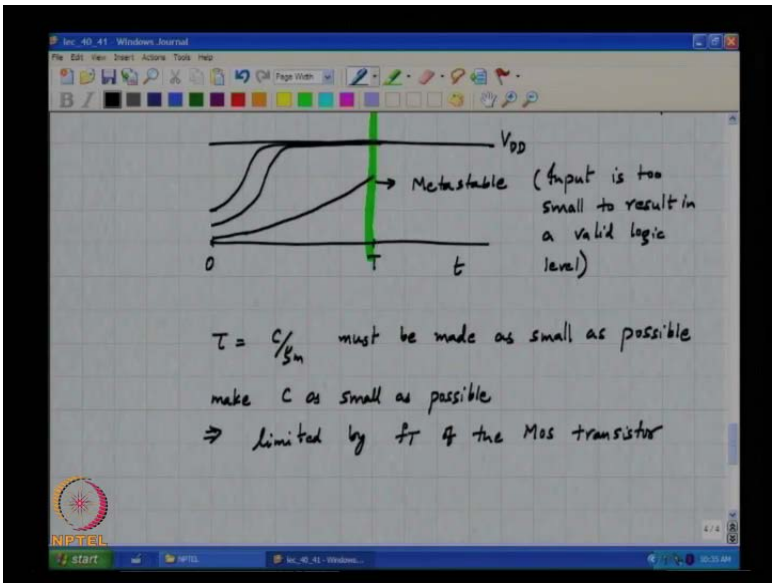

And let us say the input started out here, then what happens the input regenerates and the output is plus T, I mean at time equal to capital T is without ambiguity the full level that we want. Now, as the input keeps getting smaller and smaller, what happens, this happens, as you can see the delay of the comparator, therefore depends on.

Student: The input

How close the input use to the threshold. And if the input is very, very close to the threshold the output may not regenerate to a logic level, and in this case the comparator output is suppose is called metastable, where the input is too small to result in a valid logic level. Now, if the output is not a logic level, what do you think is a problem.

Student: ((Refer Time: 17:30))

Student: Thus

Student: Arrays

I mean clearly the output of the comparator arrays is going is being read by several levels of several stage of the logic, when you say the output of the comparator is not a valid logic level. It means that in digital parlance it is that x, where you know what the following stage of logic interprets the signal as is anybody gets. So, the same signal

could be interpreted by different logic blocks is being either a high or a low, in general this I will lead to errors in the flash output code.

So, in other words the delay or the time taken for a comparator to make a decision is dependent on the magnitude of the input, a large input in other words an input, which is large. When, compared to the threshold or far away from the threshold, will result in a decision which is very quick whereas, an input which is close to the threshold, will take a long time to regenerate.

Therefore, if you have only a finite time, it means that you will not get a valid logic decision in that finite amount of time, if the input is very close to the threshold. So, this is very similar to what happens, you know when you go for an interview for instance, what is the committee trying to do, it is trying to make a decision whether you are in or out. So, if you get kicked out of the room you know in a minute, you know definitely for sure that it is one of 2 things, either you are in or you are out presumably the committee does not want to waste its time you know too much.

So, if it is a sure shot candidate, then you are through or if you are sure reject also you are through, the moment you are on the border is when they would like to spend a lot more time and trying to figure out whether you are above threshold or below threshold. So, if you know you going into an interview, and then you spend lot of time in the with the you know guy who is interviewing, you then you know you should be worried. I mean of course, we come out very quickly, I am sure you know yourself there you know you are you are in or out.

So, that is what, this metastability is all about, and this will as I said will cause errors in the output of the flash converter, so the way of increasing the gain of the comparator or to reduce or make the minimum resolvable input smaller. What do you think, you can do I mean of course, capital T is fixed, so the only other variable you have is.

Student: Tau

You make sure tau is small as small as possible, so in other words tau is C by g m must be made as small as possible which means.

Student: ((refer time:21:27))

You mean, you know the g m finally, you know is going to implemented using.

Student: Mass transistors

Mass transistors and these transistors themselves have inherent capacitance, so there is no need to deliberately put another capacitance there, the input which you want to make a decision on can be stored on the parasitic capacitances of the.

Student: Mos

Mos itself. So, you make C as small as possible, and therefore which means that you do not put an explicit c at all, you are depending on the parasitic capacitance of the mosfet. So, basically you are limited by the f T of the mos transistor because g m by C, where c is some function of all the parasitic capacitances in the mosfet is proportional to the f T of the device. So, if you know if the technology improves by scaling down the length for instance, then to get the same g m, you need a much smaller capacitance.

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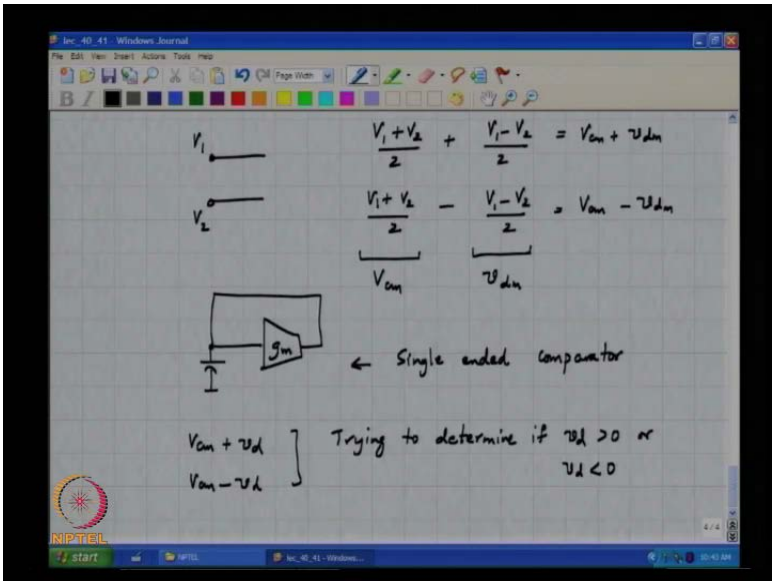

G m for a transistor is mu n C ox W by L v g s minus v T, where as c g s for instances C ox times W times L, which means g m by c g s is mu n c ox into v g s minus v T by L square.

Student: V g s plus((Refer Time: 23:49))

mu n into v g s minus v T by L square. Clearly, as mobility of the carriers increases you are expect you have a faster transistor, if v g s minus v T increases, you have a.

Student: ((Refer Time: 24:11))

You have a larger electric field pushing the carriers from the source to the drain, and if I mean, if L decreases, the f T goes up as L square and why does that make physical sense.

Student: This transistor n t

But why L square

Student: Because, it reduces the capacitance and increases the drain source is same as.

I mean in more physical terms, if you reduce L two things are happening, the field is the field strength is increased, because it is the field which is propelling the carriers is v g s minus v T by L, and the carriers have to travel.

Student: Shorter distance

A shorter distance, so it goes as L square. So, as you keep increasing the ((Refer Time: 25:00)) in the technology the comparators, I mean the regeneration time constant becomes smaller, which means that the minimum resolvable input for a given capital T. That given time you have for the decision becomes better, but unfortunately as technology keeps shrinking you are also expected to make.

Student: Capacitor

You know converters or circuits which are faster, so that I mean you will find that the design in a shorter channels mos technology, is just a challenging as one in a longer channel technology. Now, let us try and look at some circuits which allow us to do this, in a practice, therefore what one must do is to try and realise the trans conductor in principle. And it turns out that most circuits, these days on a chip are what are called fully differential circuits, as you might have seen in your analog I C design class.

So, information is not carried on one wire, but on

Student: 2 wires

Student: 2 wires

2 wires and the information is not the absolute potential on either of the wires, it is the difference between these 2 potentials. For example let us say you have to wires carrying voltages v 1 and v 2, the 2 wires voltages can be represented as v 1 plus v 2 by 2 plus v 1 minus v 2 minus v 2 by 2 and v 1 plus v 2 by 2 minus v 1 minus v 2 by 2. This is the, so called common mode voltage, and this is the differential mode voltage, so this is v c m plus v d m, and this is v c m minus v d m, any two voltages can be expressed in this fashion.

So, the advantage of having information being carried on two wires rather than one is that in a noisy environment, if both these wires go through the same environment, then all noise sources.

Student: ((Refer Time: 27:54))

Will add to both these wires in the same way. Therefore, only the common mode voltage of these 2 wires will be effected; however, the difference between these 2 potentials is still maintained in spite of adding.

Student: Noise

Noise to both these wires, that is the motivation behind going fully differential. And all state of the art signal chains are all are almost always fully differential, simply because I c's are expected to operate or analog sub blocks are expected to operate on the same chip with a lot of digital stuff. And the digital circuits are switching at, a lot of gate switching at the clock speed, so the supply and ground can be extremely noisy.

Now, if you have a fully differential analog system, then supply noise or any other noise source for that matter, which is common to both the paths can be rejected, because every time you are only measuring or you are only working half of the difference between the 2 wires. So, now, earlier I mean we were trying to resolve whether a single voltage was greater than 0 or less than 0, now if we take this a make this fully differential, what are we trying to do.

Student: Single ended

So, this is a single ended comparator as simple as it can get of course, this needs to be a lot more embellishment before this can be made a practical circuit, but at least the basic idea is this. Now, if you are now dealing with an input, which is differential, in other words the 2 wires are v c m plus v d, and v c m minus v d what are we trying to accomplish.

Student: Threshold is can create error

What we are trying to do is trying to figure out, if v d is greater than 0 or v d is less than 0, does it make sense, in other words we are trying to figure out whether v c m plus v d is larger or v c m minus v d is large. And please recall that I mean v d can be either positive or.

Student: Negative

Negative. So, going by our discussion on the single ended version, what do you think we would do for a differential version.

Student: ((Refer Time: 31:26))

Student: Single spaced differential

No, I mean what is the analogous schematic

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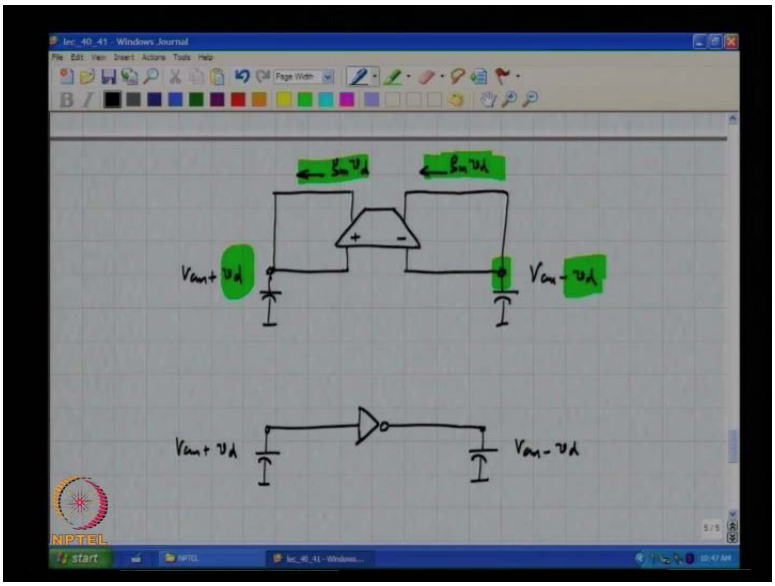

So, now you have 2 capacitors in principle, one carrying 1 holding v c m plus v d and the other holding v c m minus v d, and what do we need to do.

Student: ((Refer Time: 32:04))

We need to sense, what do we doing earlier in the single ended case, if we v d was greater than 0, we were pushing it.

Student: Current circuit to ((Refer Time: 32:20))

you are pushing it higher by you know using a voltage control current source, which only dependent on v d, now what should you do.

Student: If see the difference between

We look at the difference between these 2 nodes, and then pump currents such that, if v d is positive.

Student: From right to the left

So, let us say this must be g m times v d, and similarly if on the other side you must, you pull current out of the other node, does it make sense earlier we were looking at one voltage and pushing one current. Now, we are looking at the difference between 2 voltages and pumping, a current, which is the proportional to the difference between these 2 voltages, does it makes sense. So, please recall, therefore that this is plus v d, and current is being pulled out of this node this way.

Similarly, this voltage is minus v d, and current is being pushed out, so can you think of a simple circuit solution that I will do this, if this voltage goes up, current is being pulled in. Yeah, it is a trans conductor, but what is this, this simplest circuit that you can which will enable you to do this.

Student: C mos

A C mos inverter that is right, so let us say this is v c m plus v d, and this is v c m minus v d, if v c m was chosen to be the natural trip point of this inverter, what is the meaning of natural trip point of this inverter.

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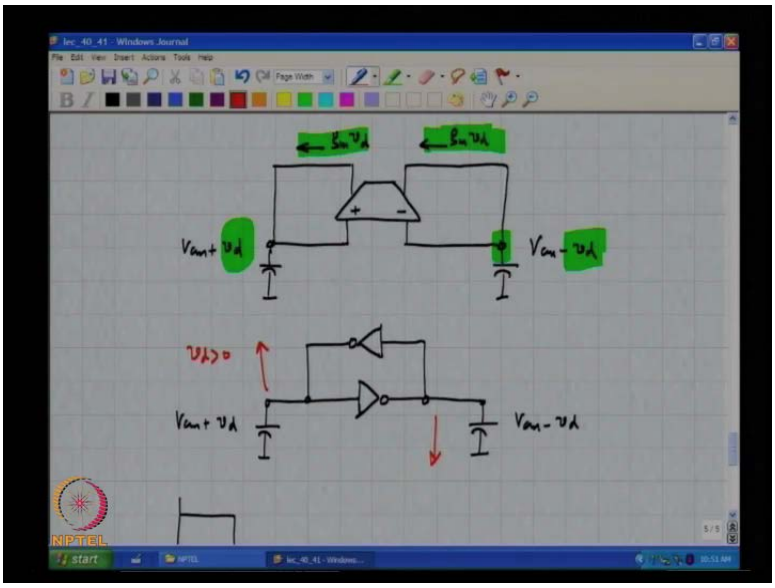

What are the characteristics how do the C mos inverter behave V i and v o, and this is you know that magic voltage v x, where there is high gain, so if you bias precisely at v x, what is the speciality of this v x.

Student: ((Refer Time: 34:04)) slope is very high

Slope is very high, but what can you say about the current through the n-mos and the p-mos transistor.

Student: Same equivalent.

It is the

Student: Same

Same, so this v c m is chosen to be the trip point of this inverter, then if v d is 0, this current is in other words for the inverter if we chose this to be the v c m. Then if v d was 0, what would this current be it would be 0 by definition, now if v d was positive what will happen, how much current will flow here.

Student: G m

G m times v d, does make sense, now what else should I do is that the whole story I need to do something else.

Student: One more inverter

Yes

Student: One more inverter

I need another inverter, which senses the other node, and therefore if v d is higher or rather if v d is greater than 0, what will happen is that this potential will eventually go to, this will keep going higher and higher. If v d is greater than 0, which means this node v c m minus v d will keep going, lower and lower and vice versa eventually the output, I will become, so high that the inverter will saturate giving you a valid logic level, does make sense.

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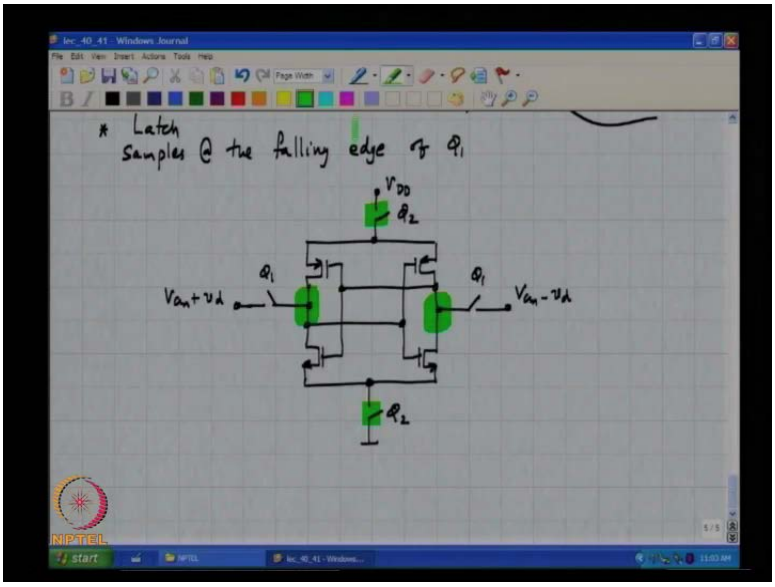

So, now let us get down to drawing circuits is 2 inverters connected back to back, and we know that we would not want to deliberately increase the parasitic capacitance at the input nodes for fear of increasing the regenerative time constant. And in any case so many devices, so there is bound to be a lot of parasitic capacitance, so you can simply use that parasitic capacitance to hold the analog inputs.

So, once this circuit has taken an input and made a decision, you must now get this guy ready for the next input, so there must be a way of we need 2 things, one once we have make sure that the correct input is written onto both these nodes. Further variations in the input must not go and disturb the decision making process, I mean just like if you have

an interview, I mean candidate goes in, and it is not like you know the other candidates are also walking in when this candidate is being interviewed, is not it.

So, you must have a mechanism by which you let in somebody and hold him in there, so you must need 2 switches, which will disable the connections to the input of the latch. So, let us call this phi 1, so the sampling instant of the latch this by other way is called a latch as you all know, the sampling instant of the latch is nothing but, the what instant is the input being sampled onto the 2 nodes of the latch.

Student: Depends up on ((Refer Time: 42:20))

Yeah, it depends on phi 1, and which edge of phi 1 is sampling instant of the latch.

Student: 3

These features are on when phi 1 is high, and off when phi 1 is low, so at what edge of phi 1 is the input what we are interested in, we are interested in, the voltage held on those 2 nodes to make a decision. So, what are those 2 voltages.

Student: ((Refer Time: 43:10))

No is the question clear or it is not clear. No, the input let us say is doing this, and this is phi 1, what is the voltage which is finally, held on that parasitic capacitance in the latch.

Student: Its phi 1

Student: Its phi 2

Student: Negative

On the falling edge of the phi 1 is when the

Student: Whatever

Input is sampled on to the latch, so that is something to bear in mind, the falling edge of phi 1. So, let us or let me ask you another thing, when the input is being sampled on to these 2 parasitic capacitances should the 2 trans conductors be active or not, let us see, so the input is being sampled onto these 2 nodes. Do you think it makes sense for these 2 guys to be active during that time, yes, no.

Student: No

Why no

Student: It will try and enforce there

Student: If I force it can consume a current out of it out of the input.

More fundamental reason why you do not want it, is the question, what we want to do is the following, we want to have v c m plus v d and v c m minus v d on these nodes, so to that end. What we do is we will attempt to write using 2 switches, which are clock with phi 1, so this is v c m plus v d, which is time varying, and this is v c m minus v d which is also time varying, does it make sense. So, during the time phi 1 is high, do you think it makes sense for these 2 people to be making a decision, I mean to help in the decision process, yes, no.

Student: Yes

Student: No

Student: Yes, first the this will be trying to write some values, but that inverter output will be pulling out

So, basically these guys will be pushing currents into these 2 nodes, which are dependent on v d of T which is not at

Student: Settle

You know settle to the right value that you want to make a decision on, so it does not make sense for these 2 guys to be active during the writing process, which means that during the writing process that is when phi 1 is high. These 2 inverters must be.

Student: ((Refer Time: 46:56))

What must be the they be doing

Student: Disable

They must be disabled, so what do you think I can do to a disable them.

Student: ((Refer Time: 47:09)) noting by cutting off the supply

So, once straight forward we are doing in this is to have switches in the between the supply and these inputs, these inverters as well as ground and the inverters ground. So, that when phi 1 is high, phi 2 is low, and as usual phi 1 and phi 2 are non overlapping clocks. So, when phi 1 is high the input is being return into the latch, when phi 1 goes low, I wait for a certain time, and then get phi 2 to go high, and what happens then, at the falling edge of phi 1.

The 2 parasitic capacitances have on them stored, the 2 inputs on which I want to make a decision, when phi 2 is enabled or when phi 2 goes high, these 2 switches are enabled causing the inverters to spring into action. And the voltage which is larger becomes larger, the voltage becomes smaller become smaller, and these 2 nodes which were at v c m minus v d and v c m plus v d depending on the sin of v d will either go to VDD order to.

Student: Ground

Ground, in this case we have chosen the negative real to be ground. Now, once a decision has been made, somebody else needs to store that decision, so you can always have a flip flop for instance, or you know another stage of memory which will hold what decision this latch is made. And then the latch must get ready for the next input, but couple of things one must observe, after a decision is been made what are the voltages at these 2 nodes.

Student: VDD

Student: VDD and

One will be VDD the other will be

Student: Ground

Ground, which one will be VDD, and which one will be ground depends on

Student: Input

The input difference v d, but the key point is if this latch has to be made ready for the next input, these 2 initial voltages are VDD and ground, so if I connect them directly to the input. What danger do I run.

Student: Sir, input was using them the ((Refer Time: 50:29)).

Student: No, whoever is driving this v c m plus v d mode he has to discharge a charger capacitor

So, these 2 parasitic capacitances are charged, these two

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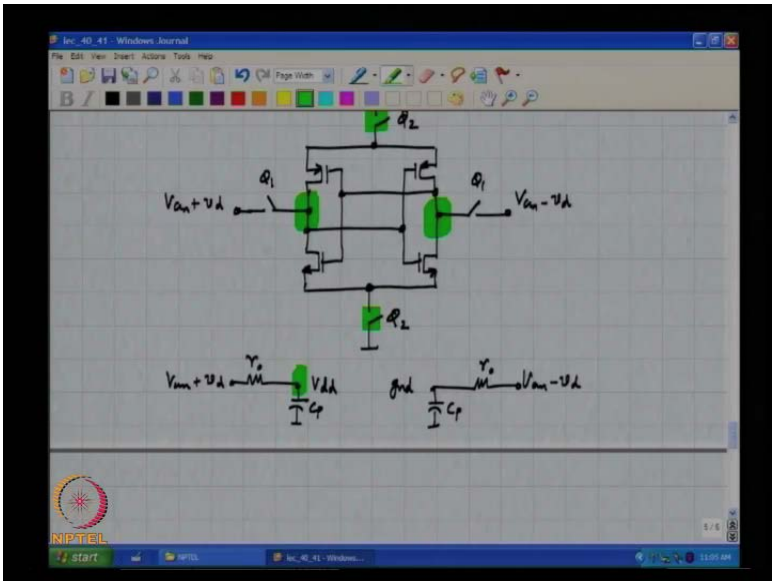


Let us assume that both of these are nominally identical, and one of them is initially charged to VDD the other one is charged to ground, the inverters are been disabled why.

Student: Because we are trying to

Because, we are trying to write the next input, so what we have is this scenario, where we are attempting to write v c m plus v d, and v c m minus v d. In principle if these voltages sources are ideal voltage sources, there is no issue, because is a ideal voltage sources the time taken to charge this capacitor is 0. In practice the voltage source that is trying to write into these nodes will have some finite output impedance, so let us call that output impedance r o, so what do you think will happen to this voltage for instance.

Student: Impendence variance

Student: It is impulse variance

No, no

Student: It should be variance minus exponential

There are 2 things happening, v c m plus v d is attempting to get onto c p with the time constant.

Student: R naught and c p

R naught c p, at the same time VDD is trying to get

Student: Discharged

Discharged again with the time constant

Student: R naught times.

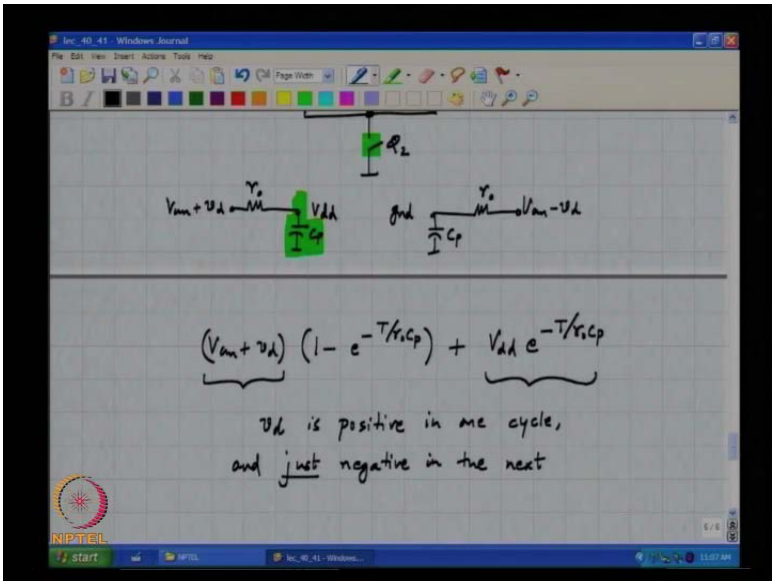
R naught times

Student: C p

C p. So, this r naught times c p is large then what will happen.

Student: ((Refer Time: 53:03))

(Refer Slide Time: 53:09)



The final voltage across c p will be some v c m plus v d into 1 minus.

Student: e to the minus

E to the minus

Student: Tau

Whatever T by

Student: Tau

Tau, T by r naught c not to get confuse with earlier time constant plus

Student: V D D

V D D times

Student: E power of tau

E to the minus tau by r naught

Student: C

C, so at the end of a time T, the voltage which will be on c p is not truly the

Student: Input voltage

The input voltage, but it also remembers

Student: Past

A past, this will be particularly problematic when the previous input cause the output voltage, this particular node to go to VDD and the next input will potentially cause this node to go to.

Student: It is ground

Student: It is ground

Ground, so in other words this is terrible when v d is positive in one cycle, and just negative in the next, because if v d was positive in the first, in one cycle the output is

regenerated to VDD. And in that extra time we need to I mean we for the next input we need to discharge this to.

Student: 0

Student: 0

We need to get rid of this VDD, but that takes time, so at the end of the time T a part of the previous decision has still remained on the parasitic capacitance. And this is clearly going to corrupt, the next input which is only let us say it is mildly negative, then this error will add to.

Student: Small negative value

Small negative value potentially making it positive, and cause the comparator or cause the latch to give you a.

Student: Incorrect

An incorrect decision. So, this is what is called hysteresis, where the latch remembers the past, so in the next class we will figure out what to do about this.