VLSI Data Conversion Circuits
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Lecture - 38
Integrator Design - I

This is VLSI Data Conversion Circuits lecture 38. In the last class we were looking at how to start implementing the loop filter of a continuous time delta sigma modulator. As we all know, the basic building block in the loop filter is the integrator.

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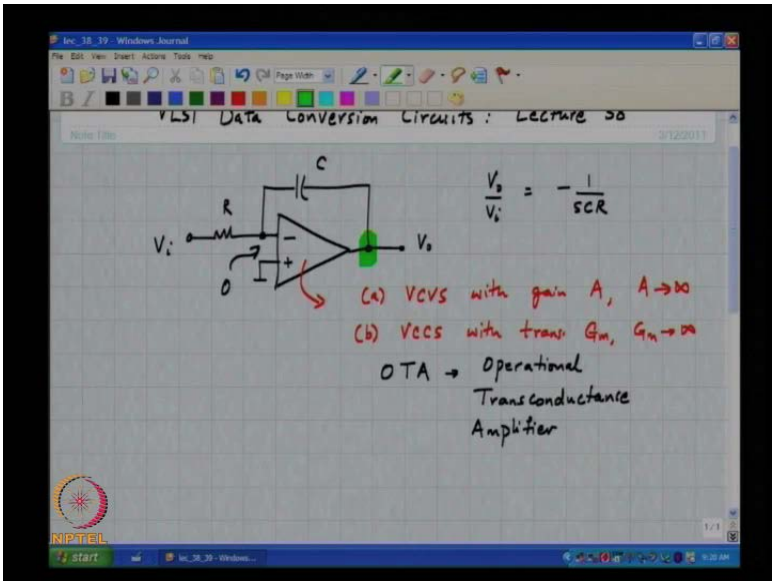

And one common way of implementing the integrator from your earlier classes is to use an op amp, and if the op amp is ideal, the input output relationship is minus 1 by SCR. So, this is an inverting integrator in reality of course, the op amp is never ideal and one common way to understand the operation of an op amp is to think of it as a voltage controlled, voltage source with again A and as A tends to infinity the op amp approaches ideal behavior.

Unfortunately with CMOS it turns out that it is difficult or rather it is not very advantageous to build an op amp is a Voltage Control Voltage Source, for the simple reason that the VCVS by definition means that the output impedance is low, which means that inside the op amp. One must have some stage at the output with a low output

impedance, and the simplest stage one can think of is a common drain amplifier or a source follower.

As we discussed in the last class and for you know using a source follower unfortunately constraints the maximum swing that one can obtain from the op amp because of the extra v t drop. So, instead of thinking of the op amp as a voltage control voltage source, it is better to think about it as a voltage controlled current source with a trans conductance of G m. And as G m tends to infinity the op amp or the, so called active element approaches ideality all right, and such an amplifier is called an OTA which stands for operational trans conductance amplifier.

And as usual if G m tends to infinity, the virtual ground voltage will be 0 and stuff, and of course, one should always be aware that, you should never operate an integrator open loop this integrator will be embedded inside the continuous time delta sigma loop. So, there is indeed negative feedback around the integrator through the other integrators, and through the quantizer and so on right. So, if you think about any isolated integrator for d c there is you know, there is definitely negative feedback through the rest of the loop.

Which is why, the output voltage the d c potential at the output of the integrator stays put right and does not you know drift off to either plus infinity or minus infinity. Which is what would happen in practice we just operated an integrator open loop, due to offsets the output voltage would either tend to plus infinity or minus infinity, in practice it would get limited to either the positive or the negative supply.

So, one does not have to worry about, how can I analyze all these integrators we seem to have no d c feedback loop around the integrator which forces the output voltage to be finite and the answer to that is we do not have to worry about it. Because, we know that eventually this is not going to be run stand alone, this is going to be an integral part of a delta sigma modulator which by definition is a negative feedback system. So, every integrator has indeed a very strong negative feedback loop around.

So, in practice of course, it is not possible to get an operational trans conductance amplifier with an infinite trans conductance, we have to make do with a finite trans conductance. In this course am not going to get into the details of the transistor level implementation of the op amps in the of the OTA's that will be covered in the analog

IC's, class what am going to do is discuss these at a at the level of macro models. So, that you get a feel of what is involved in the design.

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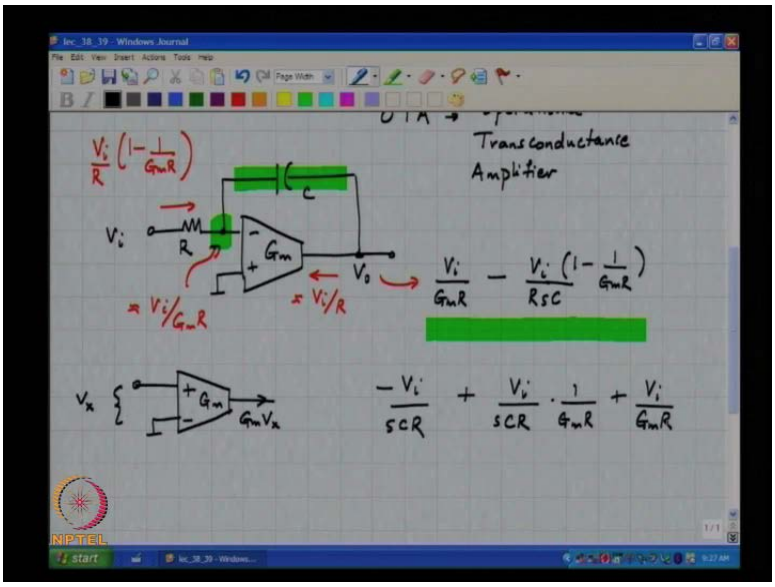

Now, this is the commonly used symbol for a trans conductor, so that you will like to understand, what the effect of finite G m is on the transfer function of the integrator right. So, if the G m is large, but finite this virtual ground node, which is ideally supposed to be 0 will be some small value, so if you say that this is approximately 0 what is this current, this current is approximately V i by R where does that current flow into the capacitor right and finally, into the trans conductor.

So, this is approximately V i by R, if a current V i by R has to be supported by the trans conductor, it is input voltage must be, so our initial estimate that this virtual ground voltage is 0 is not quite right it is actually plus V i by G m R all right this is a better approximation to the virtual ground voltage than simply say it is 0 correct. So, this current is actually, so if this voltage is not 0, but V i by G m R what is the input current flowing into the resistor it is simply V i to 1 minus 1 by G m R divided by R right.

So, if G m R is very large please note that this voltage will be very small right, and this current will almost be equal to V i by R, but not quite. So, what would be the output voltage, what is the output voltage.

STUDENT: ((Refer Time: 08:58)) by s current multiplied by 1 by s.

No not quite, the output voltage is please note this node potential minus the drop across the capacitor. So, the output voltage is approximately given by the virtual ground voltage which is V i by G m minus V I by R s c times 1 minus 1 by G m R.

STUDENT: Sir G m is prepared by current which is going outside or inside from the output.

Flowing which is the it is a good point.

If this is V x the current which flows out is G m times V x correct all right, which means that if current flows in the negative terminal must be at a positive voltage. Does it make sense of course, please note that this is also an approximate expression right, and this is telling us that the current flowing into the I mean this is based on the fact that the current flowing through the capacitor is this quantity that is not quite true. Because, our derivation for the virtual ground voltage assumed that the current flowing into the OTS V i by R right.

We know that that is slightly smaller than V i by R, so this virtual ground voltage will be slightly different from V i by G m R. But, that correction factor will be of the order of G m R the whole square, if G m R is large we can neglect G m R the whole square in relation to G m R. So, this is a quick way of obtaining the output voltage right, rather than sit and write k c l k v l, now can somebody look at this and compare it with the ideal transfer function one was expecting.

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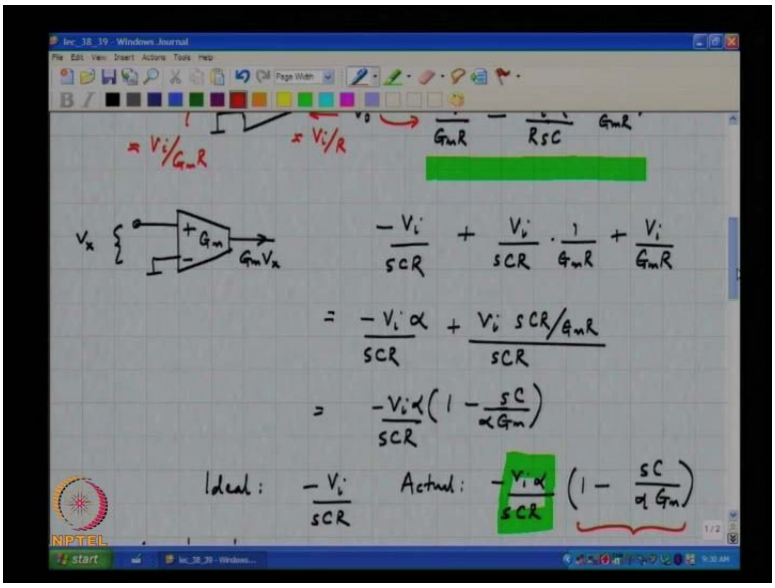

So, this is minus V i by SCR plus V i by SCR times 1 over G m R plus V i by G m R which can be I suppose written as into some factor alpha plus V i by SCR divided by G m R divided by SCR, which is minus V i by SCR times alpha minus s C by G m or now pulling alpha out. So, ideally the transfer function must be minus V i by SCR actually it is minus V i into alpha by SCR into 1 minus s C by alpha G m, so what do you see, and what is alpha by the way 1 minus 1 by G m R.

So, alpha is approximately one, but it is smaller, so the effect of having finite G m is twofold, first it appears as if the unity gain frequency of the integrator, which was ideally supposed to be 1 by R c is slightly.

STUDENT: ((Refer Time: 14:56)) less than 1.

Ideal unity gain frequency is 1 by R c it appears as if...

STUDENT: It is ((Refer Time: 15:05))

It is slightly less than 1 by R c, so for an ideal integrator you would have expected a ramp with a certain slope, now I mean for a step input. Now, you will get a ramp with a slightly smaller slope, the next thing is this and what is this factor I am sure you have seen this before in the context of circuits other circuits that you have seen this is 0 in the...

STUDENT: Right half s plane.

Right half s plane and intuitively why is this coming.

STUDENT: 2 parallel.

There are 2 parallel paths from the input to the output one is through the capacitor and one is through the trans conductor, both of them inject currents in the opposite signs which is why, the feed forward 0 appears in the right half s plane. And the trick rather or the circuit technique that is used to eliminate the right half plane 0 is to put a...

STUDENT: ((Refer Time: 16:20))

A small resistor in series with the integrating capacitor, the idea being that the voltage drop across the resistor must be the same as the virtual ground voltage right. So, what must be the value of that resistor 1 by G m right, so if you eliminate that and the 0 goes out all right. So, the bottom line therefore, is that the effect of finite G m is to make sure I mean what happens with the finite G m is that the unity gain frequency of the integrator is slightly smaller than what you had originally aimed for...

So, what do you think you can do to fix this problem of course, one thing is to say I can go on increasing G m right is there anything else that I can think of ((Refer Time: 17:37))

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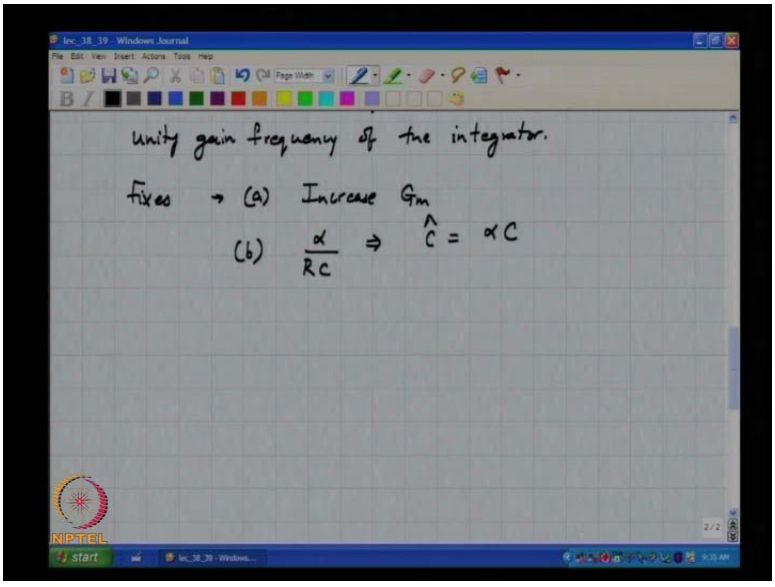

So, how do you fix this the obvious solution is to increase G m right, now what does this do to the power dissipation. Now, finally, the G m is going to be implemented using...

STUDENT: Transistors.

Transistors and to get a lot of G m you need to burn a lot of current or power in the transistor therefore, while this is a valid solution it increases power dissipation what else can you think of...

STUDENT: Amplify the signal.

You know that the actual unity gain frequency is alpha by R c correct, so which means that if we deliberately make choose C hat to be alpha times C right, you know that if we choose I mean a desired unity gain frequency of x you get alpha x right. So, I will deliberately choose x by alpha, so that I will get x you understand, so this is I mean this is what is called pre distortion right because, I know that am going to get only.

STUDENT: Alpha times.

Alpha times you know I mean you always only get alpha times what you ask for right therefore, you ask for more knowing well that, you will get only alpha times there and there is a very straight forward solution. So, the third solution is to say I am going to use a better G m, so if one does not want to increase power dissipation by a large factor by increasing G m pulse say in the sense that, increasing G m is like taking many small G m’s and putting them in parallel.

So, do you think of can you think of any other way of increasing the trans conductance.

STUDENT: Series connection.

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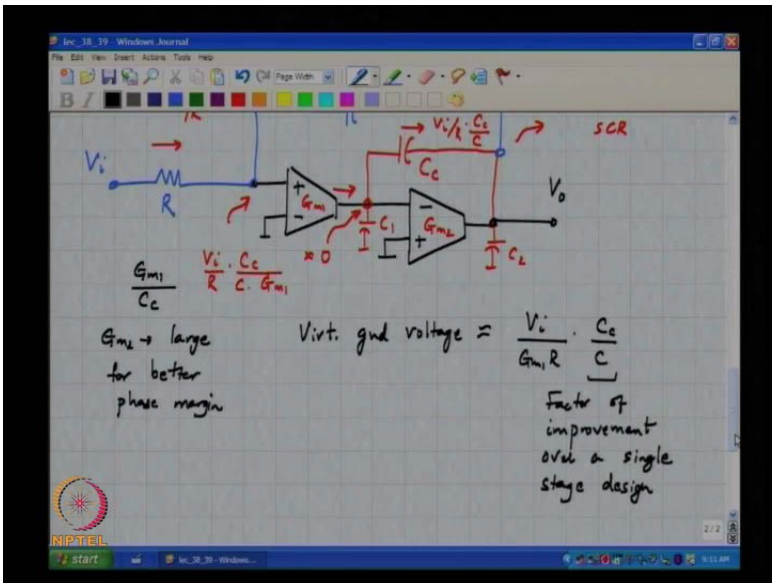

You cascade trans conductors, so in other words you attempt to make a two stage trans conductor G m 1 ((Refer Time: 21:07)) all right, at least in principle the trans conductance is at d c what is the current you get out if I apply a voltage here. Let us call this G m 1 and this G m 2, see finally, the what you must have must be dimensionally correct, the ratio of the output current to input voltage must be trans conductance if you say G m 1 times G m 2.

STUDENT: Consider a trans conductance capacitor.

If there was no load anywhere, then this voltage will be...

STUDENT: Infinite.

Infinite that times G m 2 will cause an infinite current, in practice of course, there will be non idealities say C 1 and C 2 will be parasitic capacitances. So, this voltage will be G m 1 by s C 1 that multiplied by G m 2 will give you the...

STUDENT: Output current.

Output current, so this is my, so called amplifier now this has to be embedded I mean you have to now create an integrator out of this thing what do you suggest I do what should we do next. So, we have the usual all right, so what is the problem with this structure now.

STUDENT: ((Refer Time: 23:53))

No that is not right.

STUDENT: Actual output is...

Yes. So, what is the problem.

STUDENT: I think stability.

The stability of this is a problem, as you have seen in your other classes, please note that for high frequencies the capacitor behaves like a short circuit. So, the feedback factor around the op amp I mean this is our composite op amp right, so the feedback factor around the op amp is 1 right. Which means that you want to make sure that this op amp that you have built is unity gain stable correct.

Now, from your discussions in both analog circuits as well as analog I c design, if you take two trans conductors and do not do anything, and if you attempt to close the loop around the two trans conductors what will be the what is the issue, do you understand the question. So, let us forget about the integrator for the time being this is an op amp right, if I now attempt to close the loop like this, what do you think will happen.

STUDENT: It will poles at...

So, there are two poles on the j omega axis, so the phase margin of the feedback loop is very small right. So, at least here technically it is 0. So, the two poles will be on the j omega axis, and if you want to think about neither way the loop gain function is G m 1 by s C 1 times G m 2 by s C 2 and as you can see, when the magnitude goes to unity the phases.

STUDENT: 180 degree.

180 degrees, so what do you need to do to make it stable for unity feedback one way of doing this is to use a compensating capacitor C c right, where the a idea is that the gain of the loop falls to unity much before the phase goes to...

STUDENT: 180 degree.

180 degrees all right, and this is the famous miller compensation and the unity gain frequency is approximately G m 1 by...

STUDENT: C c.

C c all right, and for a given C 1 and C 2 if you want to increase the phase margin what would you do...

STUDENT: ((Refer Time: 27:30))

If you want to keep the unity gain frequency the same ,and increase the phase margin what would you do...

STUDENT: Increase G m.

Increase G m 2, so G m 2 must be made large for better phase margin, so the second pole of the loop gain function is roughly at...

STUDENT: ((Refer Time: 28:09))

G m 2 by...

STUDENT: ((Refer Time: 28:20))

Which is approximately.

STUDENT: ((Refer Time: 28:31))

Which is approximately.

STUDENT: ((Refer Time: 28:35))

Which will be larger C 1 or C c.

STUDENT: ((Refer Time: 28:41))

It will be approximately G m 2 by C 2 plus C 1 right, the way of thinking about it is at high frequencies this capacitor becomes a short circuit. So, it is like having C 1 and C 2 in parallel, so the effective pole is at G m 2 over C 1 plus c 2, so without getting into too many details the only thing I would like to you to be aware of is that, the unity gain

frequency of this, so called op amp is G m 1 by C c approximately. And the phase margin is will be increased if you make G m 2 large all right.

Now, this op amp is to be embedded or is to be used to make an active R c integrator all right. So, let us try and understand, how we are pairing in terms of the input output transfer function here as compared to and what is the motivation for going for a two stage structure.

STUDENT: ((Refer Time: 30:19))

So, we are trying to you know avoid the problem of finite G m, and we thought that using two stages might be a better alternative than using a single stage. So, it make sense to now see how better we are doing compared to the single stage OTA right, of course, one can write the equation it is fairly messy, what I want to do here is just give intuition about why and under what conditions you will be doing better than a single stage design.

Again, let us take the same approach that we did at the last time around, this voltage is approximately 0, so this current is approximately.

STUDENT: V i by R.

V i by R, so this voltage the first order approximation is minus...

STUDENT: V i by SCR.

V i by SCR right what is this voltage approximately, I mean if you want a good phase margin what would you do.

STUDENT: Very high G m.

You would choose a large G m 2 which is equivalent to saying that.

STUDENT: 0 approximate.

This to first degree is approximately 0 correct, so what do you notice about this capacitor and this capacitor.

STUDENT: Parallel

They are not in parallel.

STUDENT: Virtually connected to ground.

So, both can you make any comment on the voltages across both of those capacitor.

STUDENT: Same.

They are the same right, so in other words since the voltages across these capacitors are the same, the current through the integrating capacitor is approximately V i by R. So, the current through the compensating capacitor will be both the capacitors have the same voltage, and that voltage is V i by SCR.

STUDENT: ((Refer Time: 32:58))

So, the current through the compensating capacitor is approximately.

STUDENT: ((Refer Time: 33:09))

V i by R times.

STUDENT: C c by c.

C c by C correct, now that current must be coming from where.

STUDENT: ((Refer Time: 33:25))

It must be either coming from the capacitor C 1 or from the trans conductor G m 1 where do you think it is coming from.

STUDENT: G m 1.

G m 1 because, we assume that the voltage across capacitor C 1 is 0 it must follow that this current must largely be coming from G m 1. So, what is the current that is being supplied by G m 1 it is V i by R into C c by C, now if this trans conductor is supplying a current of V i by R times C c by C what must this voltage be.

STUDENT: That by G m.

The input voltage of G m 1 must therefore, be V i by R times C c by C times 1 by G m R right. So, the virtual ground voltage therefore, is approximately V i by G m 1 times R times C c by C whereas, for the single stage design what did we have.

STUDENT: ((Refer Time: 34:49))

We I had only a single stage op amp, we would be able to do to generate only V i by G m 1 times R all right. So, now, you are doing better by a factor C c by C all right, so if you want to get any out of the two stage structure you must make sure that C c is...

STUDENT: Smaller.

Much smaller than...

STUDENT: C.

C you understand, so this is the factor of improvement over a single stage design, does it make sense. So, using a two stage op amp can make the unity gain frequency of the integrator closer to 1 by R c then using a single stage structure, so, the true current that will be flowing into the integrating resistor here, it will be V i minus 1 by G m 1 times R times C c by C times 1 by R. And that will flow through the integrating capacitor and the output voltage again is the sum of the virtual ground voltage plus the voltage drop across the capacitor.

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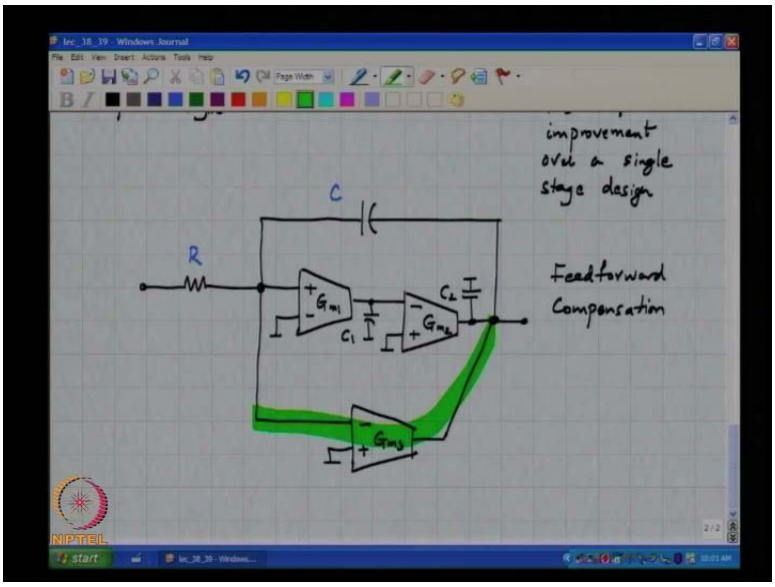

Yet another way of compensating a two stage op amp, please recall that this is the basic structure we had C p 1 and C 2 will be the parasitic capacitances of the outputs of the first and second trans conductors. With the miller approach what we did was put a capacitance across G m 2 all right, yet another way of compensating the two stage op amp is to use feed forward ((Refer Time: 38:27))

So, this is the G m 3 is the feed forward trans conductor, and this is called feed forward compensation, and this relies on the fact that because, you are adding an extra path between the input and the output, this introduces a 0 all right. And because, the sign of the current you pull out of the output node is in the same direction as the two stage path, the 0 is now in the left of s plane all right if there by increases the phase margin.

And you have seen this before anyways so, but you are familiar with adding a 0 to stabilize the modulator, I mean stabilizer two stage structure. And this is this is different from the miller compensating you know feed I mean feedback in the sense that, there the idea is to separate the two poles. Such that the magnitude falls off to unity before the phase can reach 180. Here the idea is to deliberately add a 0 or a high frequency path, which stabilize the feedback loop.

And intuitively it can be seen that, the larger the G m 3 the what can you say about the dependence of phase margin on G m 3, G m 3 is this trans conductor. If Gm 3 was not there what would be the phase margin, if G m 3 was 0 the phase margin would be.

STUDENT: 0.

0 it will reduce to the uncompensated two stage structure right, if G m 3 is very, very large what do you think the phase margin would be.

STUDENT: ((Refer Time: 41:53))

It should.

STUDENT: Continuous.

I mean if G m 3 is very, very large then the current that G m 3 supplies will be much more than the current supplied by the two stage path. So, for all practical purposes it is as if this path is not there correct, so this reduces to the.

STUDENT: Single stage.

Single stage structure, you understand which we know is neisson's table, so increasing G m 3 increases the phase margin of the loop you understand. So, the basic you now idea behind stabilizing a feedback loop is that you must have some fast path around the loop, unfortunately through the high gain path there are two poles. So, it takes a long while for the signal to get back whereas, if you have a single stage in parallel, this is the quick and dirty fast feedback path, which is not giving you enough gain.

But, it is it is doing things sufficiently fast whereas, the two stage path is the slow, but accurate path all right. And this is I mean since you looked at feedback loops in the context of a delta sigma modulator, you see here also that this is this is at the op amp level right. There we saw that, you know the high frequency path around the modulator loop is through the first integrator path, so if you have a third order noise transfer function.

The high frequency the fast path around the loop is that through the first order I mean first order path of the loop filter right. Because, that is what if you look at the quantization noise also the first order section that is the 1 by s path of the loop filter is what is producing the quantization noise at high frequencies, the higher order integrator paths are only producing is a varying degrees of the input and the quantization noise.

So, the first order path is always the fast path, and the moment the DAC pulse is delayed due to excess delay in the quantizer. The output of the first order path is producing is not enough, which is why we need to aid it by having a direct path, and that also as you seen is an example of adding a feed forward 0 into the loop filter transfer function all right this is doing a similar thing, but at the op amp level. So, you have two integrators in cascade, but you need a first order path to stabilize the loop all right.

So, I leave it as an exercise for you to work out the phase margin etcetera in relation to G m 1, G m 2 and G m 3 all right. But, these are some popular ways of compensating an op amp in the sense that, you would like to get a trans conductance which is much higher than what you can get with the single stage structure, without the power dissipation penalties associated with simply making the G m of the single stage structures very large right.

The price you need to pay for that is to have to compensate the...

STUDENT: Two stage structure.

The two stage structure one popular way of doing it is the miller compensation, where the effective trans conductance of the first stage is enhanced by a factor of C by C c. So, you came about, so you can think about this as having a single stage G m with a trans conductance.

STUDENT: ((Refer Time: 46:16))

C by C c times G m 1 and if we choose C by C c to be sufficiently large then it is like enhancing the G m 1 all right. Another way of stabilizing the two stage structure is to use a 0, and as per adding a feed forward trans conductor G m 3, and these are the basic macro model type you know in terms of the op amp. In practice of course, each of these trans conductors will have to be realized using transistors and that I will you know bank on your background from other classes on op amp design to be able to design this at a transistor level all right.

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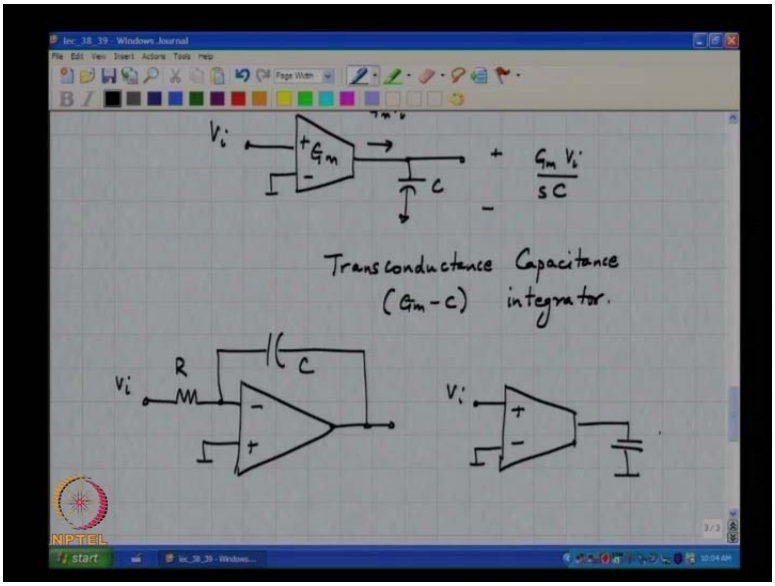

And other ways of realizing integrators exist, and one approach is to simply use not a large trans conductor, but a small trans conductor G m and directly pump this current into a capacitor right. So, if you have a voltage controlled current source like this current is G m times V i and the output voltage is G m by s C times V i all right, so this is what

is called a trans conductance or G m C integrator. And this is basically an open loop structure right unlike the active R c integrator which is a closed loop structure.

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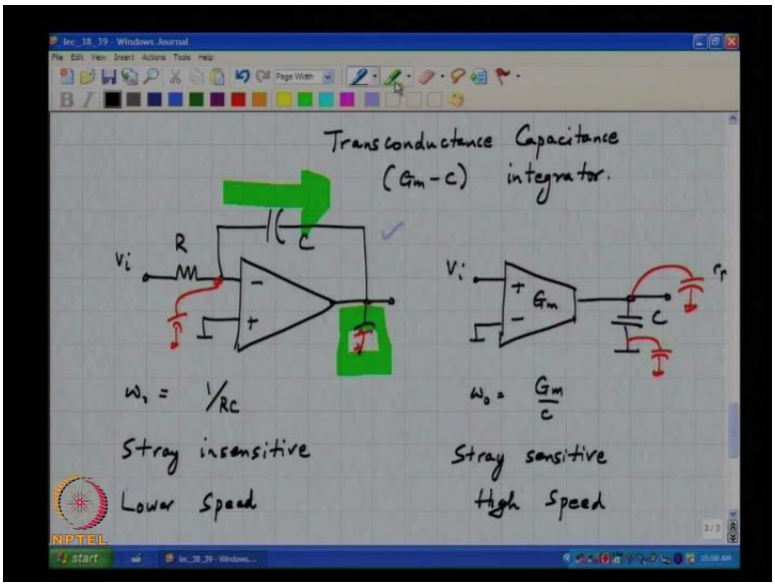

However, when you compare the two structures you need to be aware of some crucial differences, the unity gain frequency is 1 by R C here it is G m by c. So, if you want to have the same unity gain frequency in both cases you must choose G m equals 1 over R correct. Now, in reality no capacitor comes you know ideal as one had assumed every plate is associated with a parasitic capacitance all right.

So, can you comment on the unity gain frequency of this structure when there are parasitic capacitances assume the op amp is ideal for the time being.

STUDENT: ((Refer Time: 50:33))

First one you have.

STUDENT: No change.

No change at all and why.

STUDENT: ((Refer Time: 50:48))

For this capacitor.

STUDENT: ((Refer Time: 50:53))

The voltage across the capacitor is 0, so there is no current through the capacitor, so it does not do any harm, what about the capacitor the output of the op amp.

STUDENT: ((Refer Time: 51:08))

The op amp will supply the current needed by the parasitic capacitances there, the output voltage is not affected because, the output voltage is simply.

STUDENT: Quantizer.

The voltage across the integrating capacitor correct, so therefore, this structure is stray insensitive, but what about the G m C integrator.

STUDENT: It comes from...

Here you can see that, this parasitic capacitances appear in parallel with the integrating capacitance. So, the unity gain frequency is sensitive to all right, so it is fairly common to use this structure over this because of this problem, on the other hand because, this is a feedback based integrator, you can expect that speed wise it is not I mean anything based on feedback means that, you can only make it work at you know a lower speed when compared to an open loop structure right.

So, an active R C integrator is therefore, lower speed whereas, the G m C integrator being a high speed structure is a being an open loop structure is suitable for high speed operation. I mean in other words if you want to push speed in other words what you basically want is to increase the unity gain frequency of this integrator, which means 1 by R C must be higher and higher.

But, if you want to make it work like a proper integrator, the op amp must be it is gain band width product must be much, much higher than 1 by R C. So, these are the tradeoffs between a trans conductor capacitor and a active R C integrator; obviously, you know realize I mean the choice of integrators is a vast topic in itself. But, the intention here is to give you a rough idea of the flavor of the whole thing, rather than get into the details.

So, in next class we will quickly check out the effect of these integrators also add noise, so we will check out what effect the noise of the various elements in the integrator, how it affects the performance of the integrator, we will continue in the next class.