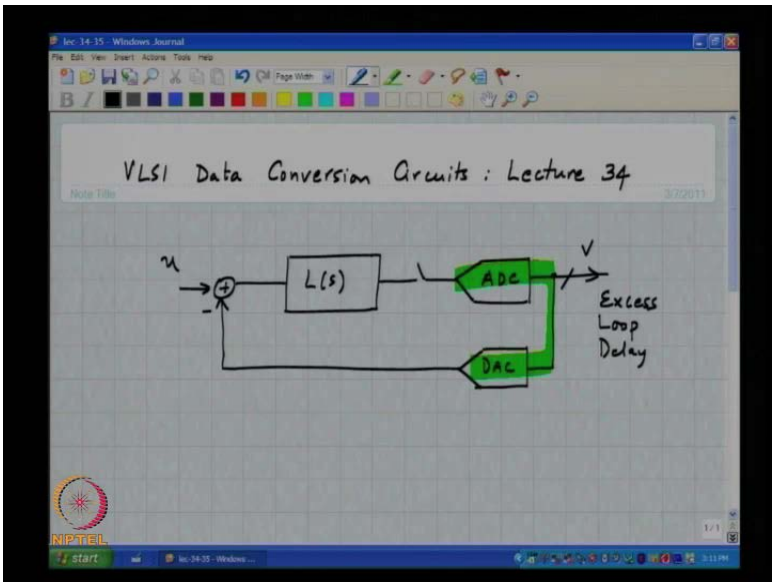
VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 33
Effect of Clock Jitter on CTDSMs - 1

This is VLSI Data Conversion Circuits lecture 34.

(Refer Slide Time: 00:17)



In the last class we looked at what the effect of one important non ideality, in continuous time delta sigma modulators, illustrated here with the shift type loop filter. We saw that in practice the ADC, DAC system will not be delay free, and this is delay that we did not anticipate during the design of the loop filter for a specific noise transfer function. And therefore, this extra delay that the ADC, DAC path adds is what is called excess loop delay. In the simplest of cases, we saw that it could affect the stability of the loop, this make sense, because every time we have feedback loop, if you deliberately introduce excess delay in the loop.

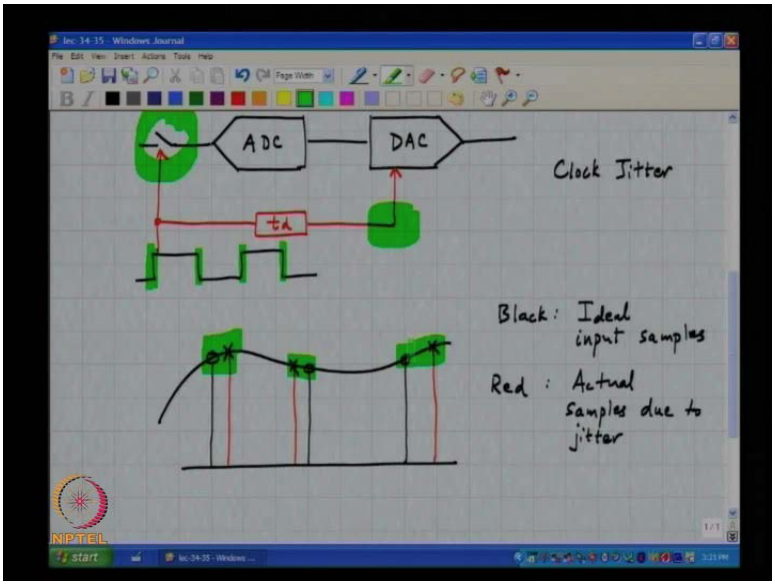
From experience we know that the loop will tend to become unstable, even if the loop does not become unstable, if because delay is very small, we saw that the performance of the loop can become altered. In the sense that even though the signal band noise transfer function remains the same, outside the signal band crazy things could happen, in the sense that the poles of the close loop system are not to originally intended them to be. In

the case of first order modulator, we saw that if we make tau the excess loop delay equal to 1, the poles are actually on the unit circle.

And you can only imagine, what happens when the order of the noise transfer function that needs to be realized is higher. We also saw, what one can do to fix this problem, and that involved adding a feed forward path across the loop filter, which can equivalently be interpreted as a direct path around the quantizer. We also saw how one could calculate the coefficients of this direct path and the values of the coefficients, which have to be modified in order to bring the noise transfer function back to the desired value, in spite of this excess loop delay.

Today we will take a look at couple of other non idealities, that occur in continuous time delta sigma modulator, the first one is what is called clock jitter.

(Refer Slide Time: 03:45)



So, if we kind of look at this path a little more carefully, ideally what we expect to happen is that, there is an A to D and DAC, the A to D basically samples, let us say at the raising edge of a clock. So, this clock is what is controlling the sampling instant of the A to D converter, ideally mind you the D to A converter would also be controlled by the same clock. And the output waveform of the D to A converter will occur exactly at the sampling instant of the A to D.

In other words, we assuming that the A to D converter looks at the input, figures out which of the bins of the input characteristics, in the incoming input lies in, generates a digital code representative of that input, that goes to a D to A. The D to A puts out a continuous time waveform, corresponding to this input code and all these happens in 0 time right clearly that is not possible. So, there is the first non ideality as we saw the last time around is excess delay, in other words one can interpret that as the A to D make some time to make a decision, and passes it on D to A.

The D to A takes it is own sweet time and generates the output pulse, all that can be modeled as if delay, the clock to the D to A converter is delayed by some t d. In other words, in this diagram both the A to D and the D to A are assume to have 0 delay, but we deliberately clock the D to A, A to D later in order to module the delay of the ADC, DAC path. Yet another non ideality that we going to talk about, now is what is called clock jitter, so when we set clock jitter what we mean is that, the edges of this clock that we use to sample the input which needs to be quantized.

As well as the delayed version of the same clock which goes and clocks the DAC, and the output of the DAC is synchronous with the edges of the input clock that it sees. It turns out unfortunately, that these edges are not occurring at the exact period that we think, that we want for example, if we say the input clock create say 1 Gigahertz, we would expect every raising edge of the clock to occur precisely at multiples of 1 nanoseconds.

What happens in practice is that the oscillators or the systems that are use to generate these clocks some noisy which means that, on the average every raising edge will be apart by a nanosecond. But, instantaneously there may be from edge to edge there may be, the delay may be off, in some cases neighboring edges may be, let us say the time interval between neighboring edges may be say 999 picoseconds.

And the next two set of edges, it will be say 1001 picoseconds, so in practice what happens is that, all that one can say is that the average delay between edges and raising edges or adjusting falling edges is 1 by f s. However, the instantaneous values that is from edge to edge may vary, according to some distribution, and that distribution and the variance of that process depends on how the clock is generated. We will not go into details of that in this course, all that we will say is that the clock edges are jittery, this the

fact that edges or not exactly periodic is called jitter; and is often refer to as clock jitter, because these edges are pertain to a clock.

So, if there is jitter there are two things which are happening, what all waves does the jitter in the clock effect the system we are looking at. If the edge is not at the right time at supposed occur, let us say before or after slightly, please note that this these are all very, very small deviations from the nominal time period. So, if the edge is slightly displaced from it is ideal value, what do you thing will happen here.

Student: ((Refer Time: 10:16))

All that happens is that the A to D converter instead of quantizing value at a certain time t, will quantize the input which is at t plus some delta t, in a similar way if this edge jitters the clock here, is simply a delayed version of the input clock. So, if the raising at jitters, it will also affect the D to A converter clock by the same amount, so what does that mean, what is the implication of that as far as the D to A converter output waveform is concerned.

Student: Sir, we can modal that as the delay in that loop.

No, see to the suggestion is that why do not you modal this as delay in the loop, I mean if this was the fix number, then we would say it is equivalent to delay in the loop, but this is varying from

Student: Edge to edge

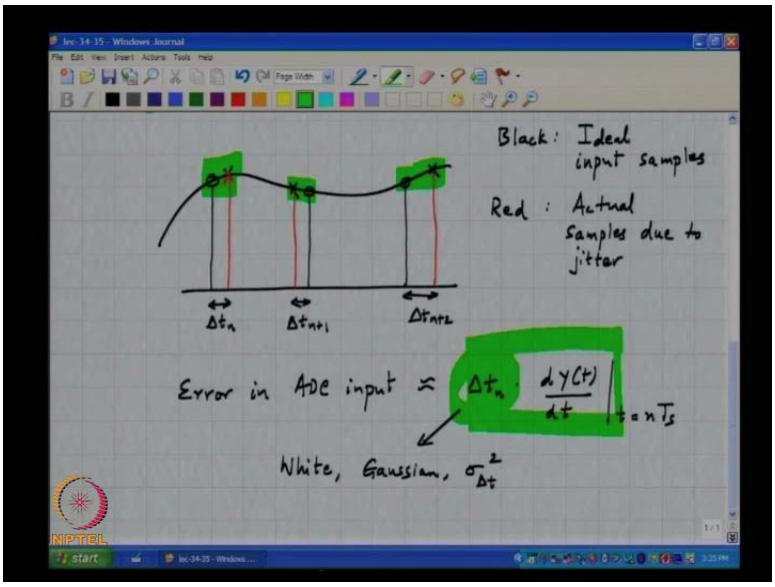
Edge to edge, so this cannot be modeled as a delay in the loop, is that clear; now if the edge to the DAC is jittered, what do you think the effect will be at the output of the DAC.

Student: Comes under different points

So, the output DAC, let say was suppose to raise at a certain time, will now raise either a little, just a little before or just a little later compare to the ideal raising time. So, let us try and understand what the effect of this is on the performance of the modulator, is this clear, so let us summaries the discussions so far, let us say this was the input to the ADC, the ideal sampling instants are these times. Now, the actual sampling instant because of

jitter is say this, please note that I am grossly exaggerating here, so that the displacement should be visible and as you can see the two of them are in error.

(Refer Slide Time: 13:50)



If I call this delta t, then the error in the sample is proportional to approximately, what is the difference between the ideal sample and the actual sample that you get.

Student: Delta T minus ((Refer Time: 14:27))

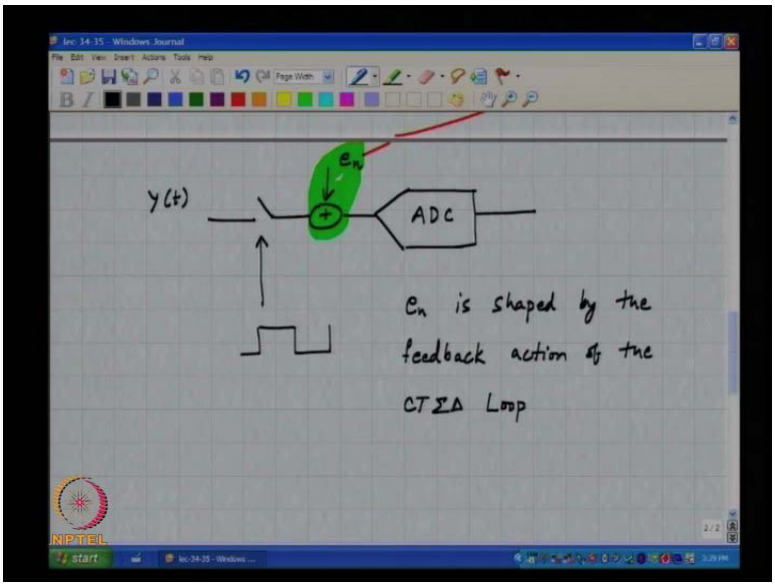
Is simply the error in the ADC input is simply delta t 7, which stands for the jitter in the n th clock edge, times d y of t by d t evaluated at t equal to n T s, equal to and T s bear in mind that the input to the ADC is y of t. For simplicity in this course, we will simply assume that the jitter sequence delta t sub n is white, Gaussian distributed. And let us say, it is bandwidth is such that, and it is very broad band and for all practical purposes can be thought of is white, and it is the a variance is sigma delta t square.

So, delta t sub n is simply a discrete time sequence, which is Gaussian distributed has variance and it is white which means that, the jitter in subsequent edges is completely uncorrelated, you understand. Now, if the delta t sub n is uncorrelated from edge to edge, can you comment on this error.

Student: Again white

It will again be white does it make sense, because each of these numbers is uncorrelated with each other which means that, if you find the average of two numbers which are like this by virtue of these being uncorrelated. The delta t is being uncorrelated, the average value of this sequence will also be 0 which means that, the errors are also uncorrelated.

(Refer Slide Time: 17:47)



Now, so therefore, you can modal the effect of sampling jitter in the A to D converter by adding a sequence e sub n, where e sub n is nothing but, ((Refer Time: 18:00)) delta t sub n multiplied by the slope of y at the n th clock. So, in other words, an A to D converter or ADC sampling the input y of t with a jittery clock can be modeled by the same A to D, sampling with a claim clock, but the error due to jitter represented as an additive sequence at the input of the A to d.

Of course, in this particular case, because of the assumption we made on the nature of the jitter, this e sub n is a white sequence. Now, I mean what do you think the effect of this will be on the performance of the modulator, so recall that what we need to do, is to replace the ADC at the input, by an ideal sampler followed by an additive noise source which is white.

Student: ((Refer Time: 20:04))

Yes, so correct, so the question as you rightly guessed, this is equivalent to, this exactly the place where you injecting quantization noise into the loop, so if you inject a little more noise.

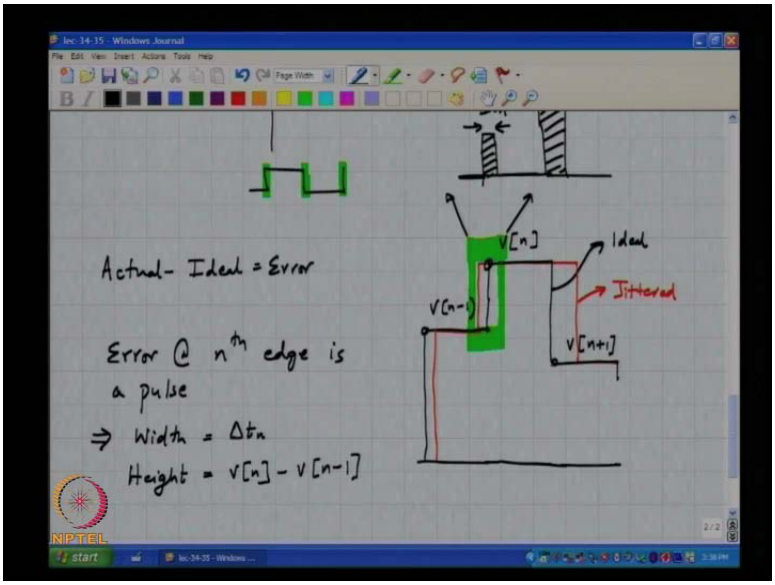
Student: ((Refer Time: 20:30))

You know it will also be shaped by, the action of the loop just like quantization noise; and please note the variance of the quantization noise is delta square by 12, which is much much larger than the variance of.

Student: Jitter

The jitter noise, so as far as the A to D converter is concerned, e n is shaped by the feedback action of the C T delta sigma loop, is this clear. Now, the next thing that we need to worry about is what happens to the ((Refer Time: 21:56)), so this is taken care of we need to worry about, what happens with the DAC.

(Refer Slide Time: 22:17)



Now, please remember, so the DAC receives that digital input code from the A to D converter and is ideally suppose to put out a wave form v of t, which is synchronous with the DAC clock which is nothing but, a delayed version of the ADC clock, and these edges are jittery. So, if the clock was not jittery and let us say V of n rather was this sequence assuming a non return to 0 DAC, what would the output waveform look like, it

would simply look like this. So, this is V of n, let me call this V of n minus 1, this is V of n, this is V of n plus 1.

So, the ideal continuous time waveform should look like this ((Refer Time: 24:40)), assuming the non return to 0 DAC. Now, what is happening the edges are jittery, so let us say without loss of generality for example, that this edge comes too late, this edge comes a bit early and this edge also goes late. When the DAC does not know what is happening, every time it sees clock edge the output changes value, so the jittery waveform will look like this.

So, what is the error between the ideal waveform and the jittery waveform, what is the difference, let us say ideal minus actual or let us say the error is nothing but, the actual minus the ideal, is the error waveform. And how will the error waveform look like, so during this interval how it will look like.

Student: ((Refer Time: 26:58))

It will be 0 until the actual wave form raises, then the error will do this and then, come back, then what about at the next edge.

Student: ((Refer Time: 27:25))

It will be negative

Student: ((Refer Time: 27:36))

Ideal minus actual

Student: ((Refer Time: 27:46))

Actual minus ideal is what I want

Student: Sir, both will positive

Both will positive, I will draw that cleanly, so if I look at the error here ((Refer Time: 28:25)), you can see that it is what is the width of these pulses.

Student: Delta t

So, it only delta t n, this is delta t n plus 1, what is the area of this these pulses?

Student: ((Refer Time: 29:21))

Please note that the width of the rectangular pulses is

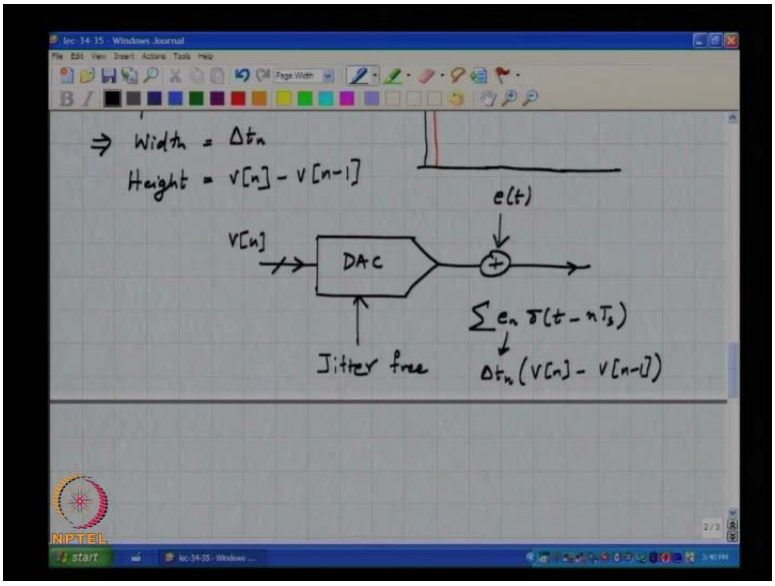
Student: Delta t of n

Is a pulse with a width equal to delta t of n and a height

Student: V of n minus

V of n minus, V of n minus 1, so one can, therefore modal the DAC, as a DAC which is been driven by an ideal clock which is jitter free.

(Refer Slide Time: 30:15)



And to this one is adding an error waveform e of t, where the waveform can be thought of as being for instance is sigma, let us say e n of t or e n is the n th error times. How do you thing we can represents this error, go back to your network classes ((Refer Time: 31:51)) you have a pulse which is basically very very thin and has some area, how do you think you can represent that as.

Student: In Dirac delta

Dirac delta, you can think of it is e of n delta of

Student: T minus n T s

T minus n T s, where e n is delta t n times V of n minus V of n minus 1 does make sense, so let see what happens in a real, I mean when you try and understand the effect of jitter in the clock, when you embed this in a delta sigma loop. Please notice is one thing, if there is no change in the sample from clock cycle to clock cycle, it make sense that the error you add is 0 even with the clock jitters, because the next sample was is the same anyway.

In other words, if two subsequent samples are the same and if we had an NRG DAC, then there is no error due to clock jitter.

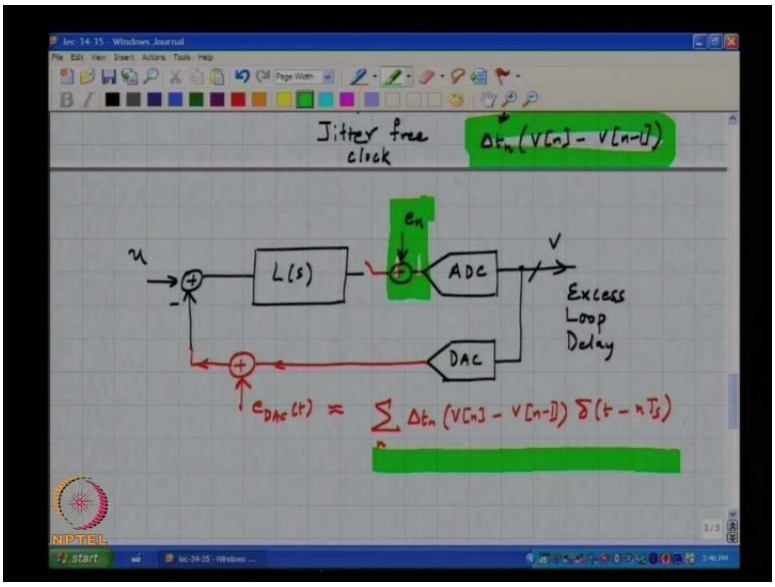
Student: Sir, this e n dimension should be voltage

e n dimension should be voltage, the yes that is correct.

Student: ((Refer Time: 33:46))

No, V of n is this delta t n times V n minus V n minus 1, and the dimensions of this will multiply and you will get, all that we are doing is we are saying that this area corresponds to the area of the impulse that is all.

(Refer Slide Time: 34:30)



Now, let us see what this does to the modulator, I am to copy and paste this ((Refer Time: 34:16)) diagram, so we have already saw that, the error with the ADC is that no

consequence, because noise shape. What we are interested in now is the error due to the jitter in the DAC, you may call this e DAC of t which can be approximated as sigma delta t n V of n minus V of n minus 1 delta of t minus n T s. Please bear in mind the delta t sub n, which is the jitter of the n th clock edge is a white sequence by assumption.

And therefore, ((Refer Time: 36:10)) this sequence it is also white, now before we get into the details of what happens to the output SNR, what do you think will happen do you think e DAC of t is detrimental to the operation of the loop, or this is also no consequence just like the error in the A to D converter path.

Student: ((Refer Time: 36:51))

[FL]

Student: It is a estimated input

Yes, so

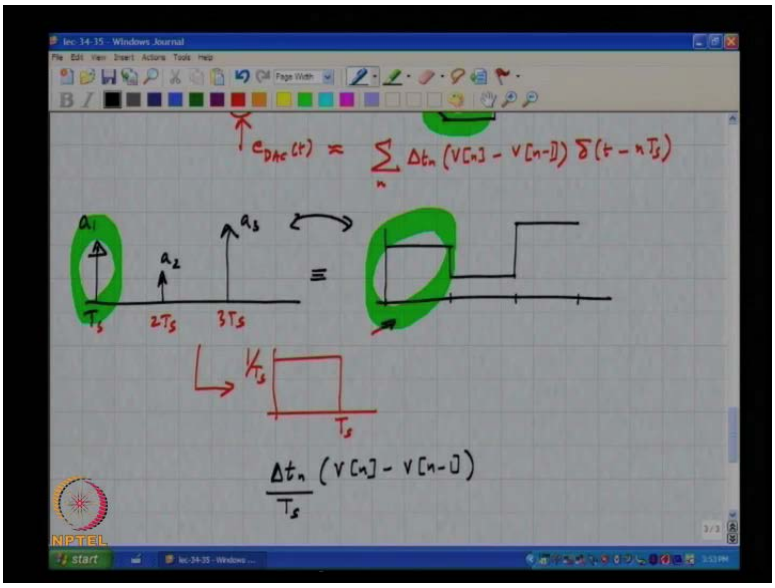
Student: So, in band noise also interrupt

Correct, so please note that this can be interpreted as adding something directly to the input of the modulator and therefore, e DAC of t, at least the low frequency component of it will come out directly. Because, the STF at low frequencies is 1. So, unlike the error due to jitter in the ADC path, which is noise shape by the loop, the error due to clock jitter in the feedback DAC path is a serious problem; and will degrade the performance of the loop, is this clear.

Now, let us try and understand what this sequence looks like finally, what frequency components of this are we interested in, we are only interested in those components of this waveform at low frequencies, that is those frequencies which are inside the signal band. So, and please note that, because we have impulses this actual signal consist of very high frequency components also, but we are only interested in band signals.

Because, the STF of the in band signals is equal to 1, and stuff which is out of band will anyway get filtered out by the decimation filter after, which occur after the delta sigma modulator, is this clear.

(Refer Slide Time: 39:03)



Now, as far as low frequency signals are concern, an impulse strain like this is exactly equivalent to, let us call this area a 1, a 2, a 3, these are the strength of these Dirac in pulses. If we are only interested in low frequency content, we can represent them also by NRD pulses like this, as long as the, what is the meaning of low frequency content, do you understand my accession here; I am claiming that as far as low frequency content is concerned both these waveforms are identical.

Given this waveform how will I generate this waveform

Student: By integrate

No, not integrated

Student: ((Refer Time: 41:04))

With what impulse response, if the input sequence to a filter is this, and the output is this

Student: U of T minus U of T minus T s

So, it is U of T minus U of T minus T s, so if this is say T s, this is 2 T s, 3 T s and so on, you can think of this waveform as being generated by this waveform, pass through a filter which is 1 here and class up to T s, you understand. If you want the low frequency content of this to be the same, as the low frequency content of this held waveform, you what do you want the gain of the filter to be at d c, you wanted to be 1.

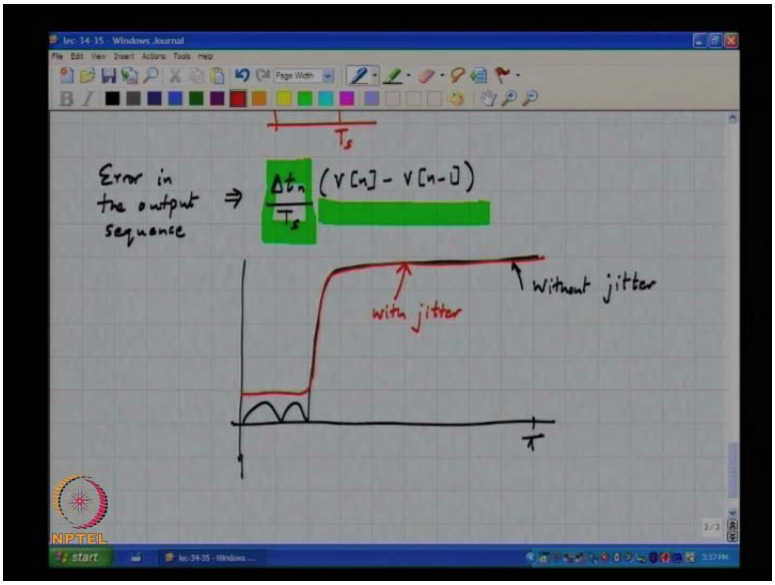
So, you should choose this to be actually not 1, but 1 over T s in other words, as long as the area of this impulse is the same as the area of that rectangle, the low frequency content which is nothing but, the average will remain the same, is this clear and that is the intuition. When you low pass filter what are you doing you are just averaging, so whether you have a sequence of impulses with a lot of high frequency content, or whether you have a sequence of rectangular pulses as long as there areas remain the same.

At low frequencies they will have the same spectral components, what do you think is a motivation for this interpretation at all, why do we need this?

Student: ((Refer Time: 43:44))

So, I mean we know that the DAC is putting out V of n times this rectangular function, now you are modeling the error also by as an NRG type waveform which means that, instead of talking about e DAC of T, one can refer this to the input of the DAC and think of it as an error in V of n itself you understand, does make sense. So, what must be the sequence, that you must add to V of n it simply the area of those impulses, which is delta t sub n times V of n minus V of n minus 1 divided by T s. So, this is the error sequence that will be produced with the output of the modulator, you understand.

(Refer Slide Time: 45:41)



And what kind of sequence is this, this is also white, because this sequence is white and it is this is telling you that the larger V n minus V n minus 1 is, the more the error will be at that sample, this make sense. Because, this is the DAC changes by a lot from sample to sample, and if the edge jitters, the error you are adding is proportional to the change multiplied by the time jitter delta T.

So, without getting into the math's, if the output sequence is an error by, I mean the in other words the actual sequence is the ideal sequence plus noisy sequence, which is white. What do you expect will happen to the output spectrum, let us say the ideal spectrum was like this ((Refer Time: 47:24)) to this you are adding white noise. So, what do you think will happen to the in band frequencies.

Student: ((Refer Time: 47:33))

So, this will be the stuff without jitter, with jitter you can expect something like this.

Student: Sir, why do not it effect the higher frequency

Well it will, but this is being on large scale is so small that, when added to the shape quantization noise it just will pale in significance, so the jitter variance goes up by 3DB, the in band noise will go up by 3DB due to clock jitter. So, the total in band noise will consist of the shape quantization noise plus that due to clock jitter, and it turns out that the loop filter itself will be noisy, because of transistors and resistors and capacitors in stuff in the loop filter.

Therefore, the loop filter will add it is own noise, so the total noise at the output will be the sum of all the three, quantization noise plus jitter noise plus thermal noise from the loop filter; so will calculate the variance of the noise due to jitter in the next class.