VLSI Data Conversation Circuits
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Lecture - 32
Excess Loop Delay (ELD)

This is VLSI Data Conversion Circuits lecture 32, in this lecture we will discuss some non idealities that are prevalent in continuous time delta sigma modulators. Let me just refresh your memory, by drawing a general block diagram of a continuous time d s m.

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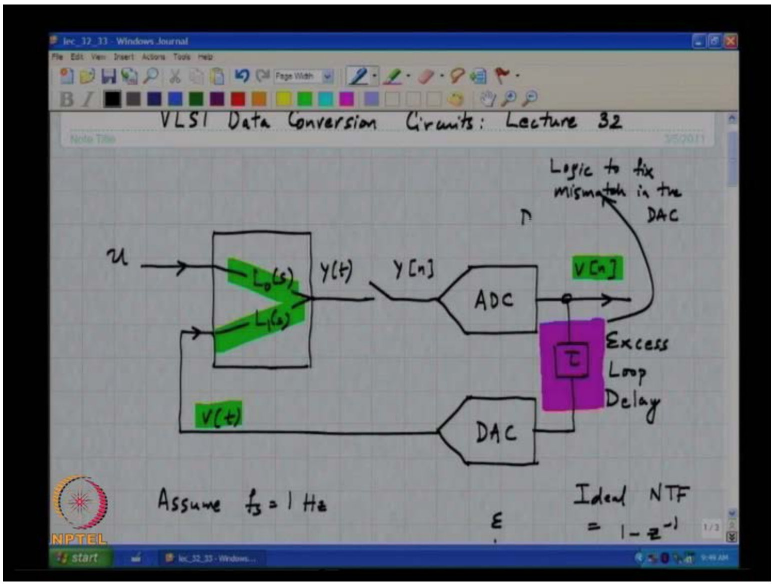

This is a generic loop filter, where the transfer functions from the quantized output port, and that from the input are different and denoted by L naught and L 1. This takes care of both a types of loop filters, namely the CIFF and the CIFB and any other variant there off. The output of the loop filter is sampled quantized, and fed back and therefore, you know as usually we have seen how to calculate L 1 which can result in a noise transfer function that we want.

One assumption we made is the following that is if y of n is available at a time instant t, V of n is instantaneously available right. And if V of n is applied to the DAC, the output V of t is instantaneously available correct, so in other words there was no delay between the sampling instant, and the time at which the DAC output is available that is what we said we have a quantizer, which is an ADC followed by a DAC. The DAC has some pulse shape right, and by implication what we meant was, that if the output of the loop filter is sampled at a time instant.

The quantized wave form that is at that at the output of the DAC is available instantaneously, that is clearly not possible right. However, fast your circuits are there will always be a finite delay between the time at which you sample, and the time at which the DAC output pulses available right. And that delay can be attributed to several factors 1 the a to d convertor will take a finite time to make a decision right and when you apply that digital code to the d to a convertor, the d to a convertor will also take some time to produce the output waveform right.

So, we have to therefore, account for this extra delay in the ADC DAC path all right, and without loss of generality we can say that I am going to club all this delay into one place. And let me say I will do it say here, where the assumption is that I can model a non ideal ADC and DAC, as far as time delay is concerned by one lump delay, and the assumption that the ADC and DAC are actually ideal does it makes sense. So, this is the, so called excess loop delay right.

And this is something that we had not taken into account, when we derived the loop filter our assumption was that the quantizer is instantaneous, and based on that we had gone and derived the transfer function of the loop filter, which resulted in a desired noise transfer function is this clear. Now, before we get into the details what do you think will happen due to this excess loop delay.

Well like in any feedback loop, the moment you add a delay in a feedback loop we know that this is always detrimental for stability right. So, you I mean what we can expect therefore, is that the noise transfer function will definitely change right because, now this samples of the loop filter output are not taken at the right times. Because, the p of t that goes into the loop filter is now delayed by some time correct, so the samples at the output of the loop filter are not the same as what you would have gotten without the delay.

So, in general one must a expect the noise transfer function to change all right and b we should expect the noise transfer function to change for the worse. Because, we know that in general if you go on adding delay into a feedback loop, the stability of the loop is compromised you understand. Now, given that this rough intuition a we need to figure out in more detail what will happen, and more importantly we need to figure out what to do to fix the problem right.

So, to get intuition on what happens in a more quantitative manner, let us take a simple example see what happens, and use that to build intuition on what to do to solve the problem right

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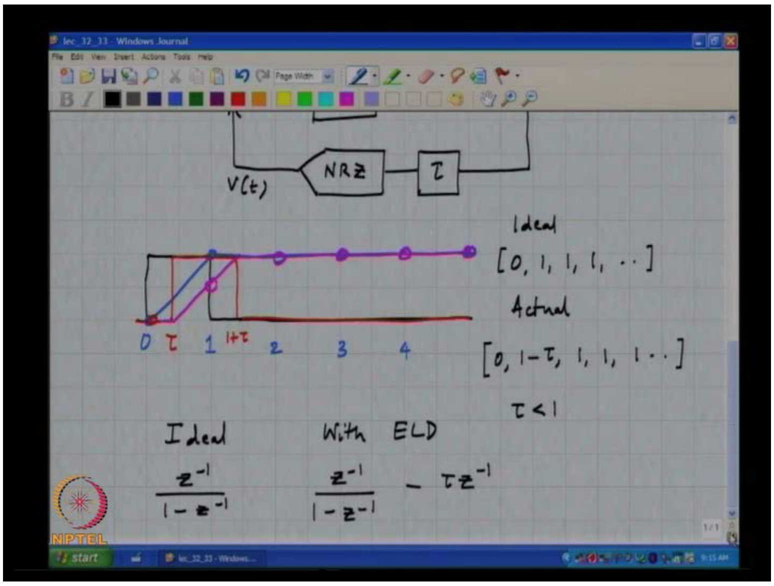

So, I will take a first order delta sigma loop as usual I will assume that the quantization error is additive, I will assume an energy DAC pulse. And I will close the loop like this ideally the NTF is what assume as usual that the sampling rate of the loop is 1 hertz, under these circumstances the ideal noise transfer function is 1 minus z inverse. Now, let us see what happens when we add an excess delay of tau in the loop, so how do we figure out the noise transfer function.

STUDENT: Inject at and lower on the loop.

As usual we did like to find the impulse response of the equivalent discreet time filter, in the ideal case this was the pulse right. And this would be the output of the integrator, so this is t equal 0, 1, 3 and, so on, the samples of the loop filter output would be these guys all right. Now, what is happening with excess loop delay, the sampling is happening at multiples of 1 second; however, the fed back DAC pulse is delayed by a time interval tau.

So, let me just draw the delayed DAC pulse, please understand that the width of the DAC pulse is the same right it is still 1 second it is just that it takes some time for the DAC to put out this pulse, in response to a v of n is this clear. So, what will the output of the loop filter look like now, it will start at tau and go to we use another colour for this, it will go to 1 at 1 plus tau correct, and remain flat thereafter. So, the samples of the loop filter output are given by where should I sample the magenta curve 0, 1, 2, 3, 4 and, so on.

So, the ideal loop filter must look like, must have an impulse response 0, 1, 1, 1 and, so on, the actual loop filter has an impulse response 0 1 minus tau 1, 1, 1 and, so on. And the assumption here is that tau is less than 1 is this clear all right, so the loop filter transfer function ideally the z transform would be z inverse by 1 minus z inverse with Excess Loop Delay abbreviated ELD, what is the impulse response z inverse by 1 minus z inverse minus tau z inverse.

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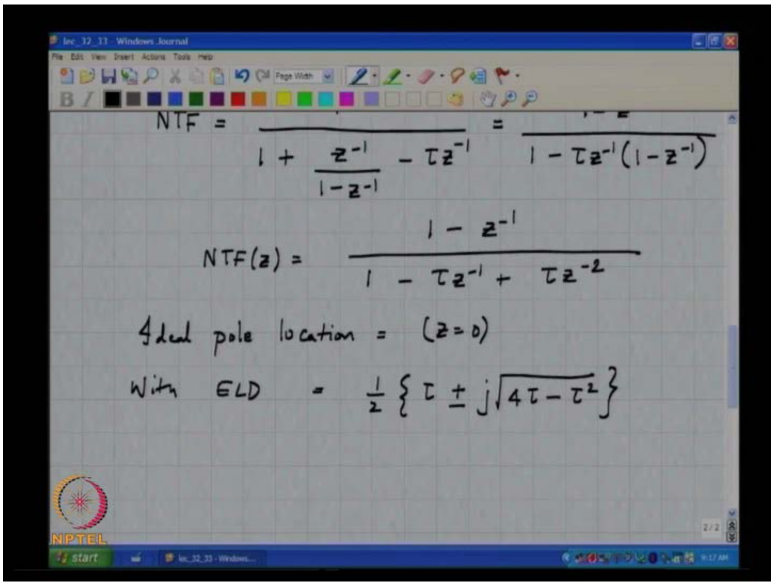

So, let us try and see what happens to the loop filter, closed loop transfer function., so the noise transfer function in practice is therefore, 1 by 1 plus l of z, l of z is now z inverse by 1 minus z inverse minus tau z inverse. We just give an which when simplified results in 1 minus z inverse in the numerator and the denominator becomes 1 minus tau z inverse times 1 minus z inverse right or the NTF of z is nothing, but 1 minus z inverse divided by 1 minus tau z inverse plus tau z to the minus 2.

The pole locations of the closed loop system ideally is at z equal to 0 with ELD, the pole locations are 1 half times tau plus minus j square root of 4 tau minus tau square all right, I mean the idea being that for tau less than 1, 4 tau is always greater than tau square. So, you can remove the minus 1 out and get j outside, and please understand that the order of the system is increased by 1 now all right that is because, of the extra delay in the loop.

And earlier the pole was at the origin with excess delay the poles have to move right, and they cannot I mean they have to get closer to the unit circle. Because, originally the poles were the only pole was at 0, and you cannot get any farther from the unit circle right.

STUDENT: Sir tau will be less than 1 the value of tau

The assumption is that tau is less than 1 all right.

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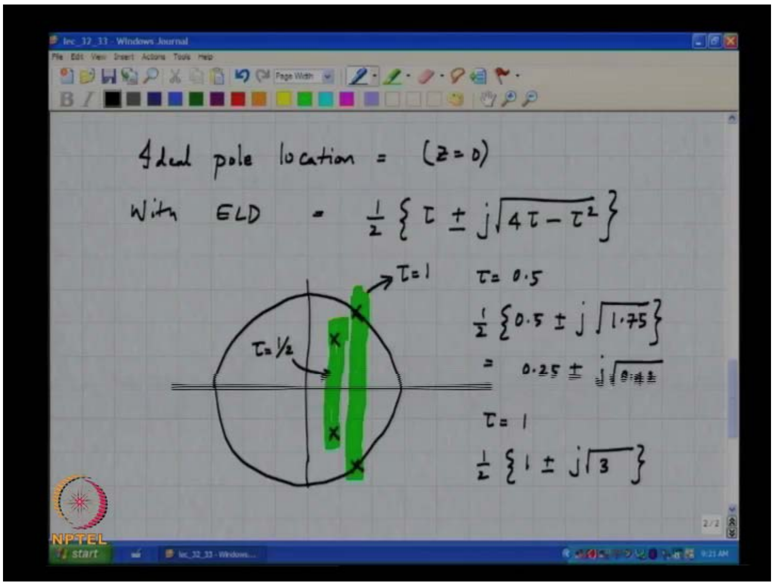

So, for, so if you plot we assume that this is the unit circle for tau equal to say half the closed loop pole locations will be 1 half times half plus minus j times square root of 1 and a half all right, which is 0.25 plus minus j square root of 0.4 or so 1.75, which means this will be close to about 0.42 or so. So, we are basically looking at some place here, after tau equal to 1 the limiting case where are the poles located 1 half of 1 plus minus j root 4 minus 1 right.

So, what is the magnitude of these poles it is one, so they are lying on the unit circle, so it is half plus on the unit circle. So, the poles are somewhere here, so this corresponds to tau is half, and this corresponds to tau is 1 and you can imagine what will happen if tau becomes greater than 1, you can use these expressions of course. But, you have to go and re-derive the loop filter appropriately, there the first 2 samples of the loop filter output will be 0 and when you do the math you will find that the poles are outside the unit circle is this clear.

So, as we expected excess delay compromises the stability of the closed loop system, so we need to do something about it. Now, for a first order system we found that the stuff is fairly easy to calculate, but one can you use the same kinds of techniques to go and find the locations of the poles, when the noise transfer function is of a higher order all right.

Now, the more important question is what can we do to fix this problem in the first place, I mean we are I mean we know what to expect, rather than trying to find what noise transfer function would be for a given tau, the more important thing is to figure out what I should do to fix the problem, and restore the noise transfer function to in this particular case 1 minus z inverse right. So, let us get our intuition about what to do from this picture what is the problem.

What is the difference between the ideal impulse response and the actual impulse response we are getting. The only difference mind you is in this sample right all the other samples are the same.

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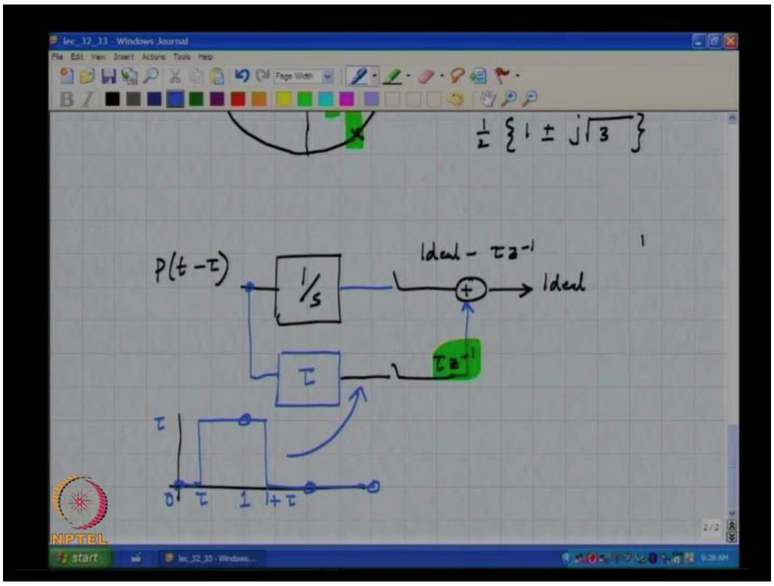

So, in other words we have this DAC pulse which I will denote by p of t minus tau to impress upon you on the fact that the pulse is actually delayed by tau, what we are getting here the samples are the ideal minus tau z inverse right. If we somehow got rid of this tau z inverse, then we will be able to get the right samples which means that you will get the right noise transfer function back is this clear.

So, in other words we have to figure out what one should I mean, clearly if you want to get you have something that you want and something that you do not want. So, you can get rid of what you do not want by in this particular case adding tau z inverse to the sampled response is this clear. So, after sampling the output of the loop filter you must get the ideal, which means that in the sampled response one needs to get rid of a tau z inverse.

Now, if we try and say in a natural thing this to say, since we need to add something to the output of the loop filter all right, what should be there inside this box in order that the sampled output is the same as the ideal right. If you want this sampled response to be the same as the ideal, please note that what we have here is the ideal or rather if you think of it this way, what we have here is the ideal response minus tau z inverse, if we get tau z inverse here then by adding the 2 outputs one could indeed get the ideal response correct.

So, if we need to get a sampled output which is tau z inverse from this box, what do you think must be there in this box what is the input to this box. The input to the box is this and the output you want is tau z inverse after sampling, so what do you think must be there inside the box.

STUDENT: Tau.

It must be simply a gain of value tau right because, the sampled output would then be if this gain was tau, this would be the wave form there. So, if I sample it I will get 0 tau z inverse I am sorry 0 tau and all 0's does it make sense correct.

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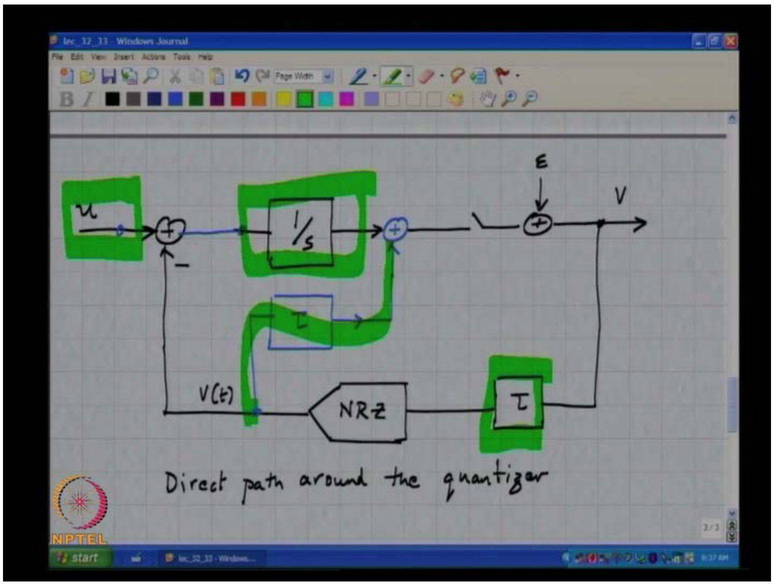

So, this is can be simplified in the following way you do not really need to sample the output separately and add it 1 can add and sample. And this upon sampling will give you an impulse response which is z inverse by 1 minus z inverse.

STUDENT: Sir, in the previous case at 1 ((Refer Time: 26:27)) but on 2 I am getting more than.

No at 2 you will be getting 0 it is simply a gain it is not an integrator is this clear, all right. So, now, let me draw the entire modulator and this corresponds to the usual quantization error, this is the DAC pulse shape N R case being the N R z pulse, this is the excess loop delay tau is being fed is this clear all right. And what is this signal here now, this is nothing, but u of t minus v of t, so one way of looking at this is to say, this tau is acting on u minus v.

So, yet another way of implementing the same correction for the loop filter, it is to say this and put another tau like this is this clear all right. And therefore, what one normally does in practice is to understand that, this path is contributing very little to the output compared to this path. So, you might say why bother I can eliminate this altogether right, and I have only this path, please note that as v of t is concerned this path simply goes this way.

So, if u was neglected for that I mean for instance, this path is equivalent to having a direct feedback path around the loop filter is this clear. And if you think about this extra path in another way, we can think of it as either feed forward around the loop filter or you can think of it as a direct path around the quantizer itself. This is the quantizer mind, you I mean the actual quantizer you know is basically this entire thing, and you can think of this as a direct path around the quantizer is this clear.

So, the solution to excess delay is to have is what we commonly find in the text books, that is a direct path around the quantizer is the way to fix the excess loop delay problem. Intuitively it makes sense, if the DAC pulse is delayed slightly then which is the sample which is most likely to be affected a very first sample is most likely to be affected, I mean seriously right.

The other samples I mean let us say you are looking at the tenth sample right of course, there it will be affected in this particular case it is not, but in reality if you have more than one integrator it will be affected. But, the effect can be seemed to be very small, right the first sample is critically dependent on the fed back quantity, which is why the first sample is most affected.

And what this direct path around the loop filter or around the quantizer is doing is to argument the lack of that first sample, by directly feeding the appropriate portion of the quantizer output, across the loop filter does make sense all right. One can also think about it in other way, this is the loop filter without excess delay we have getting the right transfer function, with excess delay you can think of it you know if you go back to your basic amplifier stuff as a phase shift in the loop all right. Which is the result I mean and the result of this phase shift can be thought of as having an extra pole in the loop right.

So, if you want to compensate for or if you want to fix the problem due to excess phase in a loop, which causes reduced phase margin and therefore, instability what will you do you add 0 correct and how do you get a 0 by feed forward is a way of getting 0's. And this can therefore, be interpreted as a feed forward path around the loop filter, thereby which enhances the stability of the loop by adding a 0 right.

Let me point out that this is a delay and this is a gain right, so let me call that k 0 and k 0 happens to be equal to tau all right. This block is not a delay, this is a gain all right maybe I should draw this in a slightly different way, so properly chosen k naught will result in noise transfer function which is 1 minus z inverse is this clear.

STUDENT: That is the value of k naught will depend upon the DAC pulse shapes.

Please note that everything is dependent on the DAC pulse shape, so we must calculate k naught based on a the delayed tau, as well as the DAC pulse shape. Some DAC pulses may not have they this excess loop delay problem at all right whereas, the energy pulse as you can see definitely has you understand. So, this direct path around the quantizer or you can interpret it the same way, the direct path around the loop filter is a way of making sure that you get the desired noise transfer function in spite of a delay in the loop filter excess delay in the loop as a excess delay comes about in practice.

Because of the finite time it takes to make the ADC come to a decision, as well as get the DAC to take that decision and generate a continuous time waveform all right. Since we have got intuition now about what to do in a first order example, when it let us go forward and see what one can do in the case of a more general noise transfer function right.

STUDENT: Sir, we know that here is the delay is between more or less or there is a delay in between a d c.

ADC DAC correct.

STUDENT: No because, is there a difference if the delay is in the ADC or there is a delay in the DAC.

As far as the loop gain is concerned right, there is no difference because, if we break the loop there, whether the delay occurs here or whether the delay occurs here or the delay occurs here or somewhere else for that matter. The noise transfer function remains the same because, the closed loop delay remains the same of course, the signal transfer function will change. Because, the absolute time at which the sequence comes out is different.

STUDENT: No, but you will have access to the point before the delay right if there is a delay in the DAC path. Now, you are taking the DAC path out for at the output of the

DAC, if there is a delay only in the DAC path then you can access the point you know the ADC output point will have no delay at all.

In this particular model that is correct.

STUDENT: In this in this particular model, you will not have no delay at all, then in that case if you can always have that first pulse that p of t will not be delayed at all. So, does that mean you can compensate even for I mean excess loop delay is more than 1 clock cycle.

So, let me come to that right, so what to the question is raising is the following, in this particular way of modelling the delay, what we have assumed is that. For example, this can be thought of as clubbing all the delay into the DAC right, so the point is making is you still have access to that digital decision right. So, the question is can you use that and I mean use that to make sure that you can close the feedback loop using this signal here rather than the output of the DAC.

The you have to be a little cautious here because, the short answer to this is yes if one can come up with a DAC which can if please note that you finally, have to feedback continuous time waveform correct. So, this as such cannot be this signal as such cannot be used, it has to be converted into analogue form right it is of course, conceivable that one can come up with a DAC, which is got let us say maybe as not as precise as the main feedback DAC right.

But, it is quicker that always it takes a longer time to do a conceivably it takes a longer time to do a good job of the DAC, rather than do a sloppy job. So, you can say I am going to have a quick and sloppy DAC, which you know gives out a decision which I mean which gives out the waveform quickly right. And I use that somehow to close the loop rapidly, but the accuracy is determined by the slow and accurate DAC in the feedback path.

I mean this is indeed conceivable, you know one thing you can also say is that, in many cases when you have a multi bit modulator, where the you have a lot of levels in the feedback loop, feedback DAC the delay of the DAC becomes large, let me get into the details of this later. But, at this time all that I am asking you is to believe that if you want to generate many levels in the DAC right, it takes you know some finite amount of time simply logic delay and things like that, which will cause fair amount of excess delay.

However, if you are only interested in a single bit decision right that can be done very easily. So, one can think of a way of a loop or several loops where the quick feedback is provided by the sloppy low resolution DAC whereas, the slow feedback is provided by the clean and slow DAC all right. So, many combinations are possible, in really high speed modulators what will happen is the following, the ADC itself will have a significant delay right, and the DAC will also have a significant delay.

So, it is not I mean, so having access to the ADC output will only reduce the problem by a factor of two right. If both of them have a comparable delays then, if you say I am going to use the ADC output and generate a quick feedback signal for the to close the loop quickly, it I mean you only solve them you know you only have a gained about half the delay right. So, it is most common to sit and compensate for the entire delay of the ADC DAC path is this clear.

The message is that, this cannot I mean this signal as such cannot be used because, it is in digital form right. This has to be converted into analogue form in order to be used, and that digital to analogue conversion takes time, and not only that if you have a high resolution a to d convertor and a high resolution d to a convertor, which is common in a multi bit modulator. Resolving a signal to a better accuracy presumably takes a longer time, you understand right.

So, and similarly converting a signal with many quantization levels into a continuous time waveform is also expect it to take a longer time. And therefore, as the number of bits in the quantizer keeps increasing, the excess loop delay generally increases, yet another thing I want to point out which is a significant source of excess delay is the following. When you did you assignment the third time I mean the third assignment you saw that if the d to a convertor is not ideal.

In other words there is the levels of the d to a convertor or not uniformly spaced right, you saw that the in band noise can get I mean terribly corrupted right that is because, the DAC is no longer linear. And therefore, you know all sorts of frequencies can fold into the signal band, raising the noise floor as well as causing significant amount of distortion, fortunately there are several schemes which can take a DAC with non uniform levels, and digitally fix those levels.

And that is done by inserting logic in the ADC DAC path, going back here you add logic in here right I am going to cover this a little later. But, this is logic to fix mismatch in the DAC all right, and this is called Dynamic Element Matching at or DEM at this point I would not worry about the exact details of this. But, all I am saying is that we know that mismatch in the DAC is a problem, I am telling you that techniques have been developed to fix this mismatch.

And that involves adding some logic between the ADC output and the DAC input, this logic has a finite propagation delay and that will naturally add to the delay of the loop. So, it is indeed a very common thing to have a lot of excess delay, especially if you are running a very high speed modulator, in which case this the logic delay plus the ADC delay plus the DAC delay can be a significant portion of the clock build.

So, I think I will stop this is a logical point to stop, I will continue in the next class where we will take a look at what one can do to compensate for excess loop delay, when you have a high order noise transfer function. In other words we have a loop filter with some coefficients we have calculated, we have seen how to calculate these coefficients right, if you want to give an NTF we have seen, how to calculate this k 1, k 2, k 3 and, so on, which are the gains of the first integrator and the second integrator, the I mean the 3 integrators in casket, 2 integrators in casket, 3 integrators in casket and, so on.

We have seen how to find those coefficients, so that the noise transfer function is what we want right. This was assuming that there is no delay, if there is delay we need to figure out what to do to I mean how do we fix these coefficients or change these coefficients to get or restore the noise transfer function back to it is original value. Clearly excess loop delay will change the noise transfer function, all we are saying now is what should we do to restore the noise transfer function back to it is original value, and we will see that in the next class.