VLSI Data Conversion Circuits
Prof. Shanthi Pavan
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 25
Single Bit Modulators

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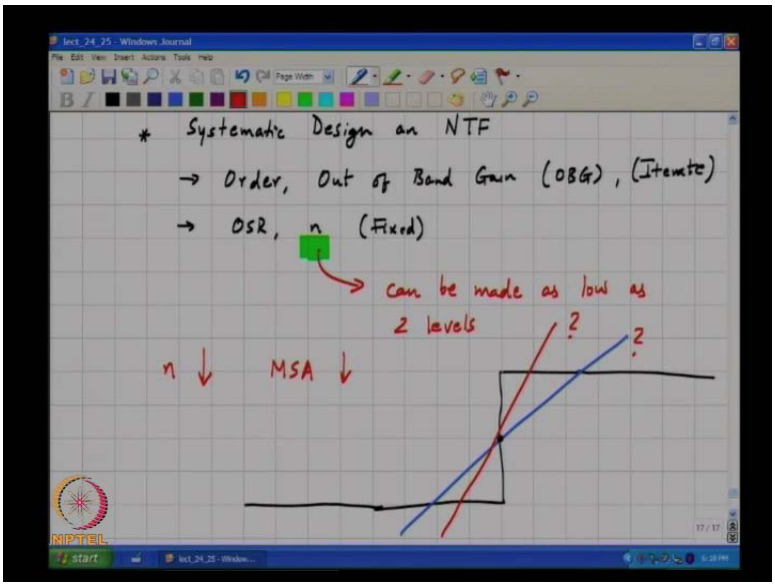

So, this V L S I data conversion circuits, lecture 25; in the last class what we learnt was how one would systematically design an N T F. So, as to achieve the desired signal to noise ratio in the signal band of course, as we saw last time, it involves iterating on order the out of band gain of an abbreviated by O B G. And, what was fixed was the signal bandwidth which is determined by the O S R, and the number of levels of the quantizer right. So, these are assumed to be fixed and we iterate on the order and the out of band gain in order to achieve the desired S Q N R in band, all right. So, clearly the choice of n is still something that we need to discuss a little bit more about, as we saw last time; increasing n only increases the in band S Q N R for a given N T F by 6 d b. So, we can take it the other way around and say reducing n by a factor of 2 which means; you reduce the number of levels you have by a factor of 2 which will only reduce the S N R by.

Student: 6 d b.

6 d b and that can be easily fixed by doing what? Simply increasing the out of band gain, you understand. I mean 6 d b seems like such a small number now right, by simply increasing the out of band gain by a little bit the in band N T F can go down you know a lot, all right. And therefore; it is very seems very straight forward to gain that 6 d b back, all right. So, then we say we reduce the number of levels by a factor of 2 increase out of band gain a little bit, and get back the S N R. Then, you get greedy and say reduce the number of levels again by a factor of 2 right, and increase the out of band gain a little more and I will get another. So, I mean what I have achieved by going on reducing the number of levels.

Student: Quantizer design.

The design of the quantizer becomes.

Student: Easier.

Easier right, because the presumably what we need to do is to compare the output of the loop filter against a bunch of levels, and generate an output analog quantity which is you know, which is dependent of these levels, right. And, the number of the fewer the number of levels we have, the easier the design of the quantizer inside the loop becomes. So, there seems to be a big motivation to try and reduce the number of levels as possible, right. In the limit how can you I mean how low can you keep going.

Student: ((Refer Time: 03:56)).

Right, so you can the lowest you can go is to have 2 levels right, 2 levels correspond to 1 bit. So, in the limit n can be made as low as 2 levels. So, as you keep reducing the number of levels, what do you expect to happen to the M S A.

Student: Reducing.

Goes on reducing all right, and when in the limit when you make n equal to 2, the number of levels reduce the maximum stable amplitude also goes down. And, the smallest number of levels one can have is to have 2 bits I mean 2 levels, or what is called single bit quantizer, or a 1 bit quantizer. The implementation of the quantizer is now, as simple as it can get, you understand. And, indeed this is done in many practical situations simply because the ease with which the quantizer can be implemented. The question now

is you know we divide all the models, and the math assuming that the quantization noises can be modeled as an additive process with white spectrum and all this stuff.

And, as we have seen in the assignment this is only valid as the, as a number of levels in the quantizer start to become large. So, clearly I mean we are pushing this too much when we say; now, I am going to make the quantizer a single bit 1 and then expect, all the math and the results to hold. So, it turns out that for a single bit modulator while the general ideas that we talked about are valid. I mean; noise is still shaped out, but since you are having only 2 levels, I mean technically speaking the quantizer is always over loaded right, because it is always saturating.

So, you find that and there is no staircase to peak off right, you just have to jump from the ground floor to the upper level right, there is no clean staircase. So, this linear approximation is you know anything is a good approximation to a step right, for example; if we had something like this is now open to question whether the best straight line that approximates; please note that this extends all the way from minus infinity to infinity, correct. So, it is open to question whether the best straight line that approximates this is this or this or what you understand.

So, it is very difficult to define the gain of the quantizer because the quantizer seems to be perpetually overloaded, correct. And therefore; all the noise assumptions we make about additive noise and all that are not valid anymore, but quite dramatically and quite almost by magic you know you can still use a single bit quantizer and get away with it.

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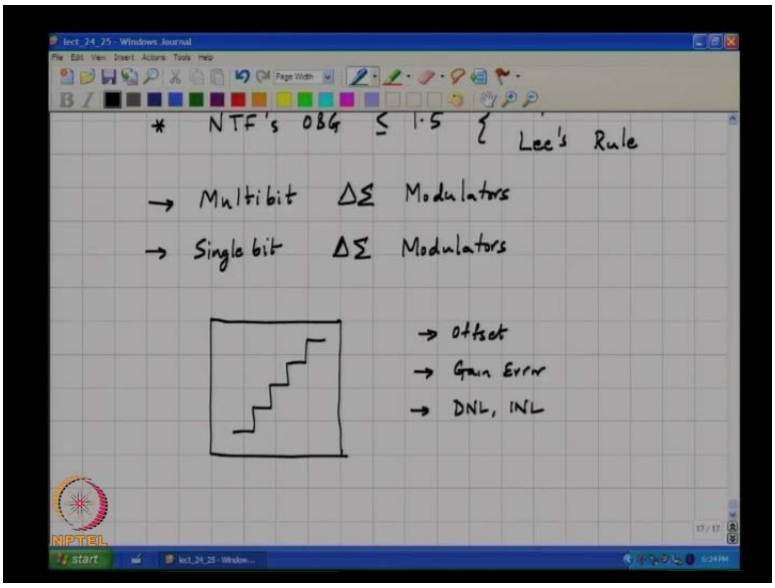

And, it turns out that now, people did some experiments or I mean enhancement simulation experiments and found that the noise transfer function gain must be less than or equal to one and half, right. So, this is an empirical rule right, is often called Lee's rule, there is a master's thesis at M I T like may be 20 years back or something like that ok.

So, where you know a whole bunch of simulations were run on single bit modulators and rule of thumb is to say; if I choose an out of band gain of about one and half. In other words; if I do not make the noise transfer function too aggressive that makes sense intuitively, right. As you go on increasing the out of band gain right, a modulator becomes unstable right. Or for a given out of band gain if I go on reducing the number of levels the modulator will tend to become unstable. And, for a single bit modulator it turns out that the maximum gain thatone1 can choose right as a thumb rule is.

Student: 1.5.

About 1.5 now, this does not mean that if I choose 1.51 the modulator will magically become I mean; will not work, right. It is just that this is a good rule of thumb, you can always, you know go a little bit above and below this. And, as I said this is this is empirical rule called Lee's rule, and works quite well in practice. So, if from the point of view of implementation of the quantizer; you decide to do a single bit quantizer then, you choose you start off I mean there is no iterating, right. You have the order you have

the out of band gain you choose Butter worth or you know a Butter worth with a pass band with complex zeroes, right. You compute the in band S Q N R, all right. It either meets your expect or it does not meet your expect, and if its meets your expect you are done. If it does not meet your expect the only thing you can do is increase.

Student: Out of band.

No you cannot increase the out of band gain any more because you know at least empirically.

Student: Out of band increases.

You know increasing the out of band gain does not help you. So, the only thing you can do is increase order, or increase the over sampling ratio. Because you know the signal bandwidth is fixed, if you want to keep the same order, but you want a lower in band quantization noise ratio, you simply increase the OSR, you understand. So, this I mean. So, therefore; modulators are of 2 kinds those with many levels are what are called multi bit delta sigma modulators, or single bit modulators. And, this is where oversampling and noise shaping are pushed to the extreme, right. So, you can take a 1 bit quantizer and make it look like a; within a signal band you can make it look like a very precise quantizer ok.

So, in most of lot of your P C sound cards for example, where voice is digitized and you are getting sound out, single bit modulators are at work. So, you can get very high precision and performance by taking a quantizer which is as bad as a 2 level quantizer. And, putting it in a negative feedback loop and making it really very precise. Now so, let us try and see; what are the motivations for going to single bit apart from the fact that the quantizer implementation is simple, you understand. So, when you try and build a multi bit quantizer, the loop quantizer is I mean; when you try and build a multi bit delta sigma modulator, the loop quantizer is a staircase like transfer curve. But when you try and realize something like this, you know that in practice, you will never get the ideal staircase, right. What do you expect?

Student: ((Refer Time: 13:53)).

I mean offset there will be offset, and there will be gain error, and there will be D N L, I N L, all right. So, let us see what happens when the staircase is not a real staircase, rather not an ideal staircase ok.

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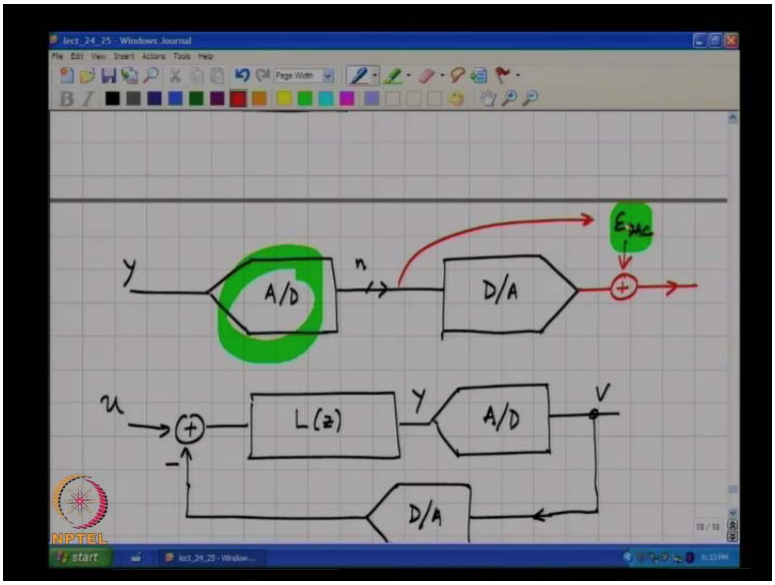

So, please recall again before we go into the integrity of this is that the quantizer is cascade of A to D and D to A converter, all right. So, the actual modulator; well, in practice look like this for example, all right. So, if the A to D converter thresholds are ideal and the D to A converter. What is the D to A converter doing? It is taking a digital word in and putting an analog quantity out, right. So, there could be errors I mean the reason why this quantizer is not behaving properly is because there are errors in the A to D. What errors could be there in the A to D? The thresholds of the A to D converter are not the ideal thresholds, right. And, the D to A converter is not ideal means what?

Student: Not a threshold.

I mean what is D to A converter doing?

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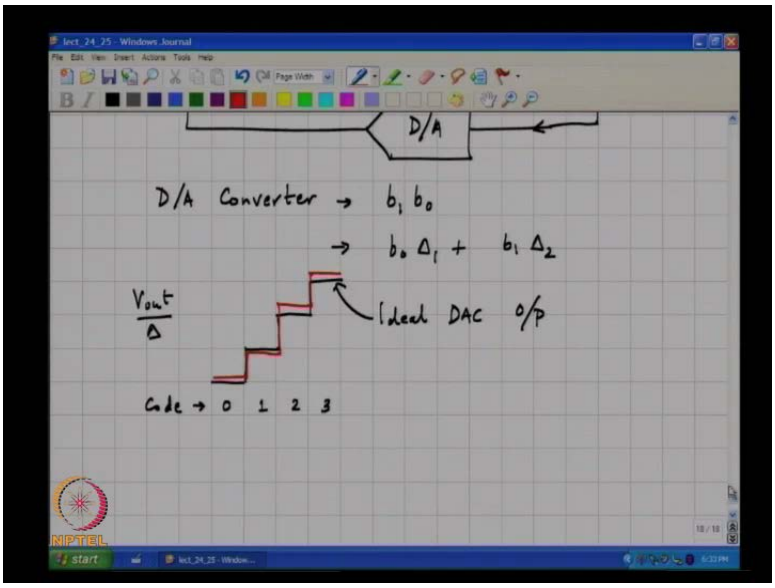

Let us say you had a say a 2 bit word, and you want to convert it into an analog quantity. What will you do? The output voltage or current should be b naught times some V ref plus b 1 times or let me call this not V ref, but delta plus b 1 times 2 delta. So, if b naught and b 1 take on values 0 and 1, you get 0 delta 2 delta or.

Student: 3 delta.

3 delta, so, if the D to A converter is not ideal; it means that the, what you get will be not b naught into delta plus b 1 into 2 delta. This will nominally be delta, and this will nominally be 2 delta, but there will be some errors, you understand. In other words; for an ideal DAC in this example depending on the bit code, if the code is 0 1 2 or 3 you must ideally get 0 1 2 and 3 times delta, correct. So, this is the ideal; what do you think will happen in practice.

Student: ((Refer Time: 19:46)) delta 1.

So, instead of this being these levels will be; it will be off. Please note that the x axis cannot change that is only code, correct. Only the output levels will be off from the ideal values is this clear. Similarly so, how can you model the error can you suggest a way of modeling this error.

Student: 2 c.

Pardon

Student: 2 C inside can.

So, what he is suggesting is that you can think of a non ideal D to A converter where the levels are not what you expected, right. As an ideal D to A converter plus some error sequence e DAC right where clearly this e DAC depends on code. So, this is a code dependent error, all right. And, please note that this is a deterministic quantity, and can be determined in principle by applying the various codes to the input of the DAC, measuring the outputs. And, you know what the ideal output should be right, and by subtraction you will be able to get e DAC of n.

When we go deep into DAC design we will understand why these errors come about, but for the time being all that we are interested in doing is studying the effect of non idealities in the in the A to D and the D to A converter, the cascade of the A to D and D to A converter from the quantizer, correct. So, the A to D converter will be non ideal, and the D to A converter will be non ideal. Non idealities in the D to A converter can be modeled by a sequence, which adds to the output of an otherwise ideal DAC, and this sequence is a function of the.

Student: Input sequence.

Input sequence into the DAC, is this clear. Now, what do you think could be a problem with an A to D converter, what kinds of non idealities we have seen this before. So, basically the thresholds are not what you expected them to be, correct.

Student: Voltage.

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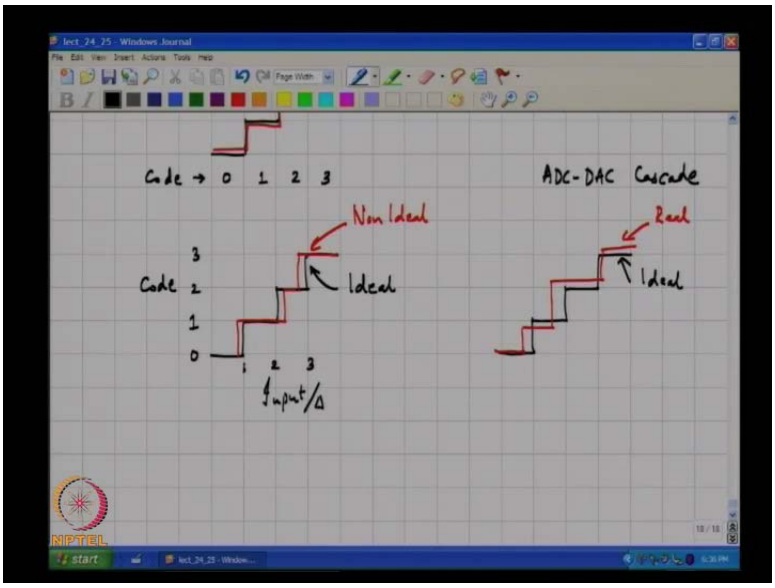

So, an A to D converter basically has a transfer curve like this, ideally you should get. So, this code on the Y axis is the code that must be 0 1 2 and 3, and this must be input by delta. So, this must be ideally 1 2 3 unfortunately, because of the way an A to D converter is implemented, the thresholds are different from the ideal values. And, say or perhaps like this. So, the red 1 is the non ideal 1, and the black 1 corresponds to the ideal characteristic.

Student: Sir earlier we have seen that a quantizing error is centered around 0 bit.

So, this is like adding an offset.

Student: Thank you.

All right, now when you cascade the A to D and D to A converter together, ideally you are expecting a characteristic which was doing this, correct. Now, what do you think will happen? When the A to D converter is not ideal and the D to A converter is not ideal what do you think will happen?

Student: Are in same.

What happens to the transfer curve?

Student: Collapses.

Pardon

Student: I mean Y levels they will be different.

The Y levels will be different and that is coming because.

Student: The DAC.

Because the DAC is not ideal, yes. X thresholds will be different because.

Student: A D C.

A D C very good. So, the real one will probably be like this. So, this is real, and this is ideal. And, just as how we modeled the error in the D to A converter, one can also model the error in the A to D converter by.

Student: An error sequence.

We can add an error sequence here, at the input of an otherwise ideal A D C, it is right. I mean; it is only a matter of what I must add to make the thresholds move. So, now let us see what the effect of these errors, please mind you these are all deterministic errors. There is nothing random about this ones you make a DAC you can actually go and find the errors in the threshold of the in the output levels of the DAC, you can also find the errors in the thresholds of the A D C, right. Now, we would like to understand what happens in the light of these inevitable errors in practice, and please note that these errors have got nothing to do with quantization, even if the A D C and the DAC were ideal you will still have.

Student: errors.

Quantization errors this are in these error sequences are in addition to.

Student: Quantization.

Quantization right, so, the effect of these errors therefore; is to this is e A D C, e D A C again this is Y this is v.

Student: Sir, V is the overall factor D to a as per the observation.

Pardon

Student: V is the overall signal after the D to a as per the best.

The final sequence that you are taking out in to the decimation filter is the output of the A to D converter.

Student: Ok that is called the decimation filter.

Is not it?

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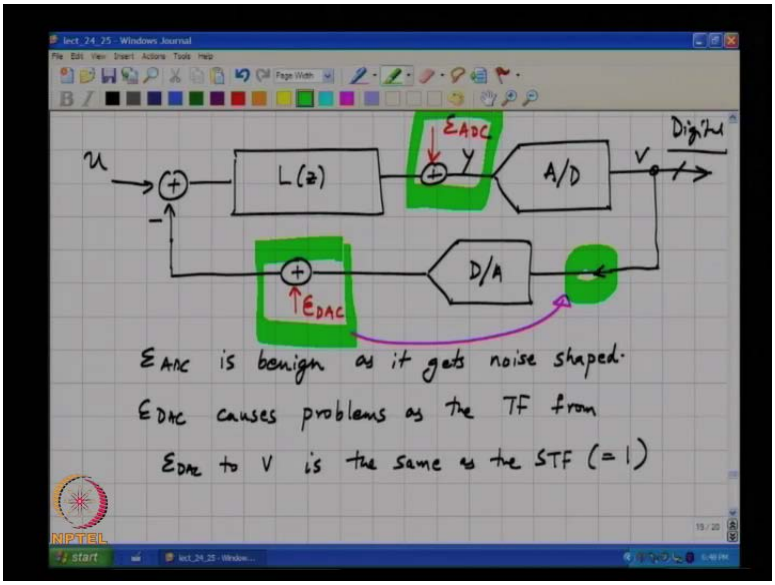

The final quantity of interest is please notice that this is the digital sequence which goes into the decimation filter, all right. So, this is the digital sequence all right. So, in other words you can say that if the D to A converter was ideal this V this digital sequence which goes here, is that digital representation of V, right. But unfortunately the D to A converter is not ideal, and the non ideality is being modeled by this sequence e DAC, which again I will remind you, is a function of the code, all right. Similarly, the thresholds with A to D converters are not ideal, and you can therefore; think of this as some kind of error waveform, which is the function of the input, right.

So, we would like to understand what happens to our delta sigma loop with these errors in practice, all right. So, let us start with the A D C error first; what do you think will

happen or what is the influence of e A D C on the in band S Q N R. Any other comments, yes.

Student: ((Refer Time: 31:30))

Pardon

Student: ((Refer Time: 31:33)).

Why?

Student: Regarding ((Refer Time: 31:38))

Well, what do you think will happen?

Student: A D C is forward loop and.

Pardon

Student: It is in forward loop e A D C.

Yes.

Student: So, 1 by 1 plus L of Z.

Correct.

Student: e A D C will decrease.

Right, so, great; so, you can see that in any case I mean you can think out this way the output of the loop filter is being quantized, right. So, we are anyway going to add, you know lot of quantization noise to the output of the loop filter. So, in principle you know corrupting the threshold value a little bit should in principle not matter too much. Another way of thinking about it is that the quantization noise is also being added at the same point. Therefore; the transfer function from e A D C to the output is the same as the transfer function from the quantization noise to the output, which is the same as the.

Student: Input.

Noise transfer function of the loop, right therefore; this errors in the thresholds of the A to D converter will get shaped out of the loop bandwidth rather out of the signal band just like.

Student: Quantization.

Quantization noise right, so, e A D C is a benign thing or let me say e A D C if it is much smaller than the quantization noise is a benign thing, right. As it gets noise shaped by the same token can you now comment on what would happen to e D A C. What is the transfer function from e DAC to the output?

Student: Is the same as signal transfer.

Is the same Signal transfer function because its adding you can think of it is adding directly to the input, right. So, e DAC causes all right, recall that in the signal band, you want to make the S T F equal to 1. So, errors in the DAC levels appear as if they are added along with the input. And therefore; will appear at the output of the modulator as this I mean this is with the I mean in line with the general intuition that if you have a feedback system, the output is largely determined by the by the feedback block. Is not it, if the feedback block is creating mischief then that will reflect in the output, right.

And, whatever happens in the feed forward amplifier as long as the gain of the amplifier is sufficiently large right, all that stuff is shared. I mean, does not affect the output of the loop. That is a general intuition from negative feedback theory, and in these conclusions must therefore; come as no real surprise, right. So, one of the penalties of using a multi bit DAC or a multi bit quantizer inside the loop is to add this error e DAC all right, which as I said is a non-linear function of the input sequence. So, if you take and what is this sequence nominally; what is the signal there? It is input plus shape noise, right.

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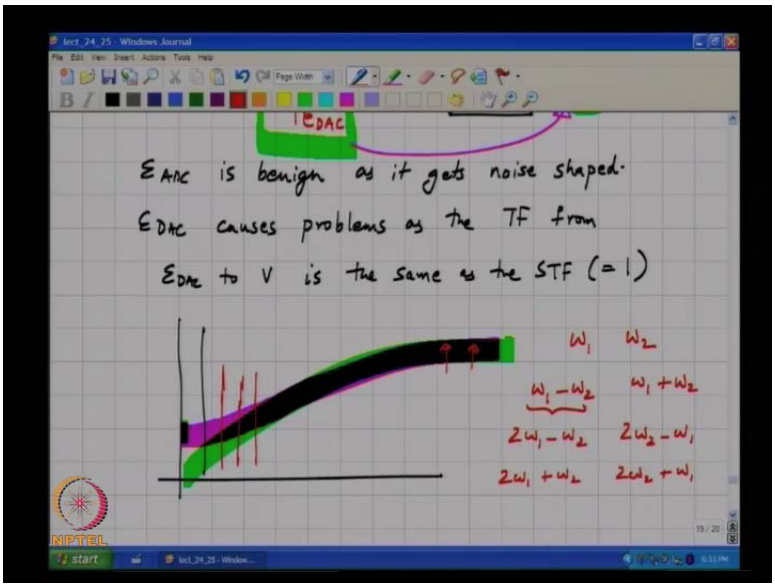

So, the spectrum here is consists of the input plus some shape noise, right. And, e DAC is a non-linear function of this sequence which has got this spectrum, right. If you take something like this and pass it through a non linearity what do you expect you will get? If you take a sinusoid and pass it through you will get harmonics, very good. So, in so, you start to see harmonics of the signal and what else do you think you will see, what about noise.

Student: ((Refer Time: 37:42)).

So, yeah you pass it through a non linear transfer curve, and you know stuff from I mean you please recall that if you have 2 sinusoids at omega 1 and omega 2 and pass them through say even a third order non linearity. You will get components at omega 1 minus omega 2 and.

Student: 1 plus omega.

Omega 1 plus omega 2 you this is for second order non linearity. You will get 2 omega 1 minus omega 2, 2 omega 2 minus omega 1, 2 omega 1 plus omega 2, 2 omega 2 plus omega 1 and you know, therefore; it means that noise from for example, omega 1 minus omega 2. So, consider a noise component here and a noise component here, once you pass them through a second order non linearity. What will happen is that it will cause the in band noise to ((Refer Time: 38:54)), all right. So, now we are stuck with not only

having harmonics of various magnitudes, because of non linearity folding causing harmonic distortion, right. This quantization noise will also. You know fold back into the signal band due to.

Student: Non linearity.

These non-linearities, does it make sense? And therefore, what has happened now. I mean all the handwork that you put in to try and shape the noise out of the signal band has been brought to not simply because of errors in the output levels of the D to A converter. Does it make sense? So, I mean what you think you can do to fix should be done to fix this problem. So, I mean the only way to fix this problem is to make sure that the DAC, even though the number of levels in the DAC are small you must make sure that those levels are sitting on a perfect straight line, right now, that is not happening. So, ideally if I join the midpoints of the staircase I must get a straight line. Now, what is happening? If it is I am getting some kind of weird non linear curve right. So, it is doing something like that, is this clear?

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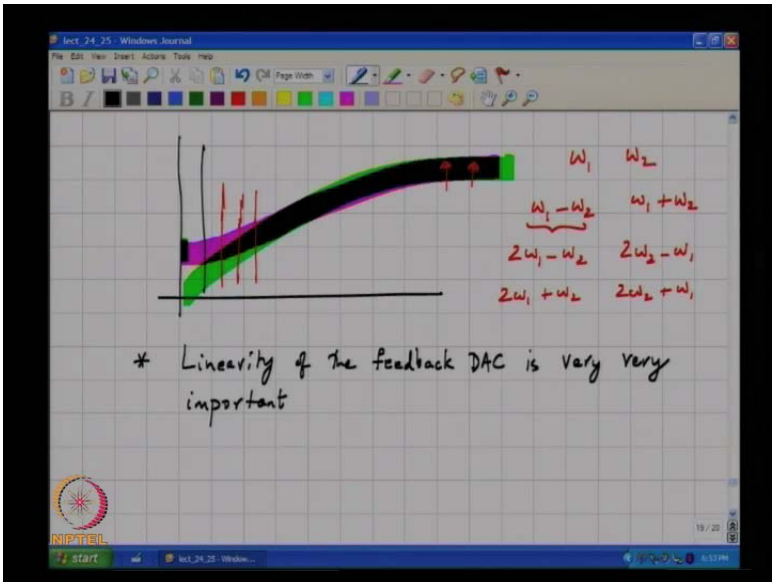

So, linearity the bottom line therefore; is that linearity of the feedback DAC is very important, because the errors in the DAC output directly it appear, as if they are being added to the input. And, therefore appear directly at the output of the modulator. Whereas errors in the flash I mean the in the A to D converter thresholds are not really a problem because they get noise shaped, is this clear. So, this is regarding a multi bit

modulator. So, now if we change the scene and make I mean do a similar analysis for a single bit modulator.

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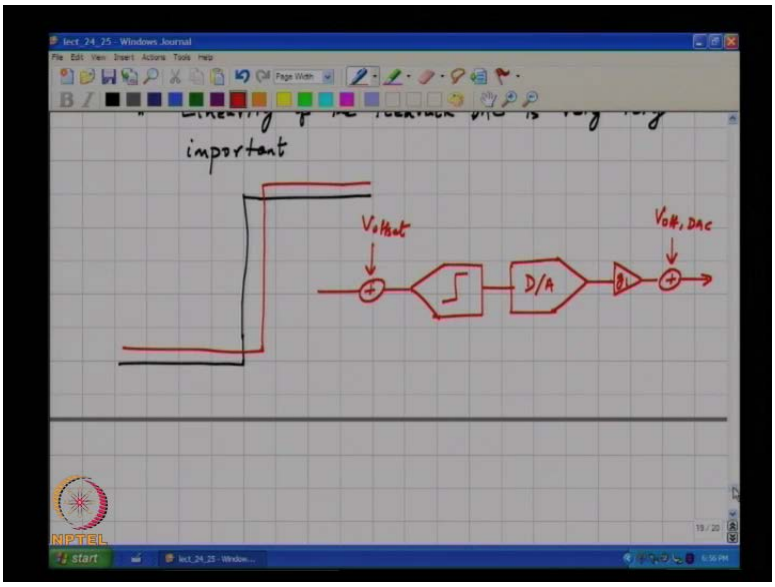

What do you think will happen? An ideal signal bit quantizer transfer curve must look say like this. What do you think will happen, if you have a non ideal single bit quantizer? I mean have a single bit A to D and a single bit D to A right. So, the A D C threshold not being correct means that they will be the staircase will shift horizontally, and the D to A converter not being ideal means that the levels are.

Student: Not same.

Are not the same as ideal once so, how can this be modeled? In the same way, but given that there are there is only you know 2 levels in the D to A converter output, and is only 1 transition point the A D C error can be modeled simply as a.

Student: Offset.

Offset right, and the D to A converter this is a 1 bit A D C, and the D to A converter error can be modeled as instead of getting say 0, and delta I am getting alpha and delta plus beta. So, what can this be modeled as.

Student: Offset and gain error.

Offset and gain error between any 2 points you can draw a straight line, right. That straight line may not have a slope of 1 and will not pass through the origin, but it is a straight line nevertheless. So, you have the D to A and then, you can modulate as an offset and a gain error. So, let me call this g 1 and then add an offset, all right. So, now if we analyze; what happens to a single bit modulator with an offset the A D C.

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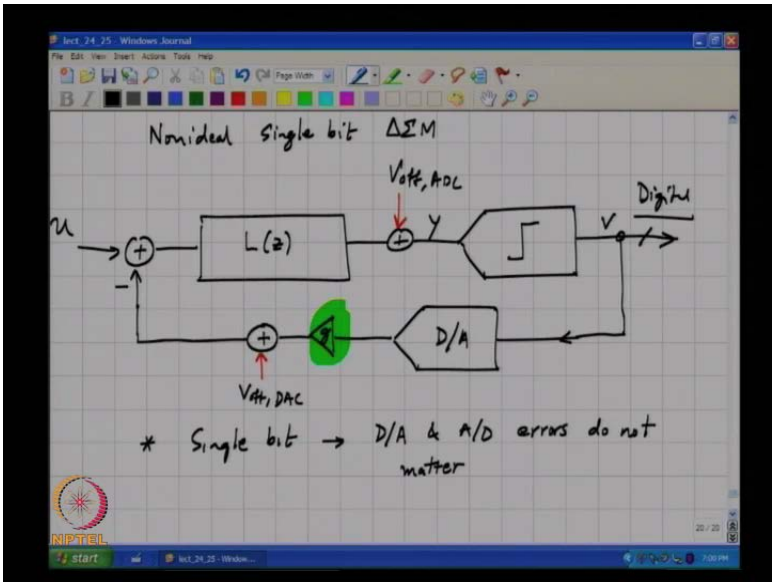

Let us say a gain error g which is very closed to 1 because hopefully the errors are small and there would be a V offset in the D A C. So, what do we conclude the offset of the A D C is as usual, not a problem at all, the offset of the DAC do you think it is a problem. It will simply add it will appear as if the input is offset by some amount. So, as far as the linearity of the entire modulator is concerned again, it is not a problem at all. Simply, because as we discussed early on this course, if you have an offset it is benign, because in a system you can always remove it by estimating it and correcting it off, what about the gain error here, what do you think it does.

Student: ((Refer Time: 46:46))

When the feedback gain changing slightly, we will only introduce a gain error in the?

Student: Overall transfer function.

Overall transfer function again it does not affect linearity, you understand. So, this is an extremely important advantage when you design a signal bit modulator, right. So, in a

single bit D S M right, the D to A and A to D errors do not matter, because they will just translate into gain and offset errors. And, the intuitive reasoning for this is that if the DAC errors which are the usual cause of the problem are not the ideal once, they can simply be modeled by I mean; if you have 2 points you can always draw a straight line right.

So, the errors in DAC levels will only result in an offset and a gain error which are very small. So, one need not worry about trying to build up good D to A converter where the levels are very precise that is something we need to do when you use a multi bit quantizer. So, you can see that you know the multi bit quantizer has some advantages; one is that you can use an aggressive noise transfer function, and because the out of band gain can be high all right. And therefore; you can reduce the in band quantization noise all right, or if you want to realize a given S Q N R within a given signal bandwidth the OSR can be reduced, all right.

On the other hand, you need to take a lot of care to make sure that the levels of the D to A converter are very precise. On the other hand; a single bit designs the quantizer design is easy one need not worry about the linearity of the DAC itself, but the out of band gain can only be about one and half. And, if you want to get a high S Q N R, this translates to either increasing the order or increasing the OSR, which is mostly what, happens in practice, you understand. We will stop we will continue in the next class.