Analog Integrated Circuit Design
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Lecture - 60
Transistor Sizing in Practice

Hello and welcome to lecture sixty of analog integrated circuit design. Hello and welcome to lecture sixty of analog integrated circuit design. This will be the final lecture of this course. In this lecture will finish some of the unfinished thread from earlier lectures and also summarize the course. In the previous lecture we were talking about discrete time filters, that is implementing discrete time filters using switch capacitors and op-amps, and we discussed how to generate the topologies for by linear transform filters and so on. What will discuss now is one particular detail of implementing switched capacitors which will reduce the errors.

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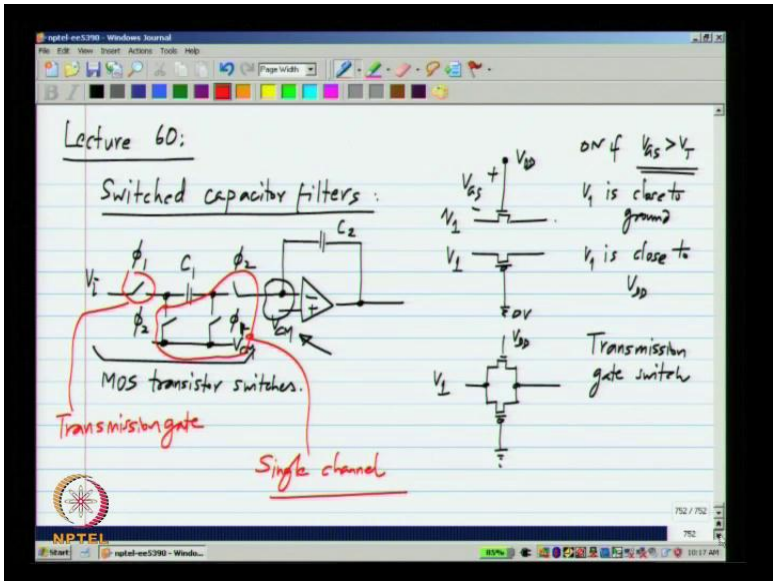

We know that a switched capacitor filter consists of units like this, I will show just one switched capacitor unit, which can be part of an integrated, and let me label these lecture phi 1 phi 1 phi 2 and phi 2. And the reality these switches will have to be implemented using MOS transistors. So, what happens is that, all these switches are implemented using MOS transistors. Now we know that if you have a MOS transistor switch, and the switch will be on if this V G S is sufficiently higher than V T. And you would like to

have as large a V G S minus V T as possible. So, that the on resistance of the switch is small. So, if you have an NMOS transistor to terminate on you would tie the gate to V D D and if you have a PMOS transistor you would tie the gate to zero volts of ground.

So, because of this what happens is that if the voltage at the terminal of the switches let us say V 1 is close to V D D, the NMOS transistor going to be off or at least will operate with the very small V G S very small V G S minus V T. So, that means, that the switch resistance will be rather high. So, the NMOS switch is good when V 1 is close to ground and the PMOS switch is good when V 1 is close to V D D. So, depending on the voltages that you want to switch you may have to use an NMOS switch or a PMOS switch or a combination of the two. So, if your V 1 occupies the entire range or a significant part of the range from zero to V D D then what you would do is use a parallel combination of P and N MOS and tie this to V D D, and tie this to ground in order to turn it on.

So, in this case for lower values of V 1 the NMOS switch will be active, for a high values of V 1 the PMOS switch will be active, and you can work with a larger range of V 1, and this is known as a transmission gate switch. Now typically what happens is that will as usual have a fully differential implementation and this point I will single ended circuit for simplicity, but this point will be at the common mode voltage of the op-amp, the input common mode voltage of the op-amp, and these things will be connected to common mode as well. Now this switch the first switch here is connected to the input V i. So, it has to handle the voltage range that is occupied by the input voltage whereas, the if you look at these other switches they are connecting this point to common mode voltage. So, they do not have to handle a large range of voltages.

So, typically this has to be a transmission gate switch, and these can be single channel switches, and if the common mode happens to be closer to V D D you would use a PMOS switch and if it happens to be close to ground you would use an NMOS switch if it is in the middle both are equally barred, but an NMOS may be better because of its higher mobility, which means that it will a lower resistances. So, that is one particular practical aspect in implementing these switches.

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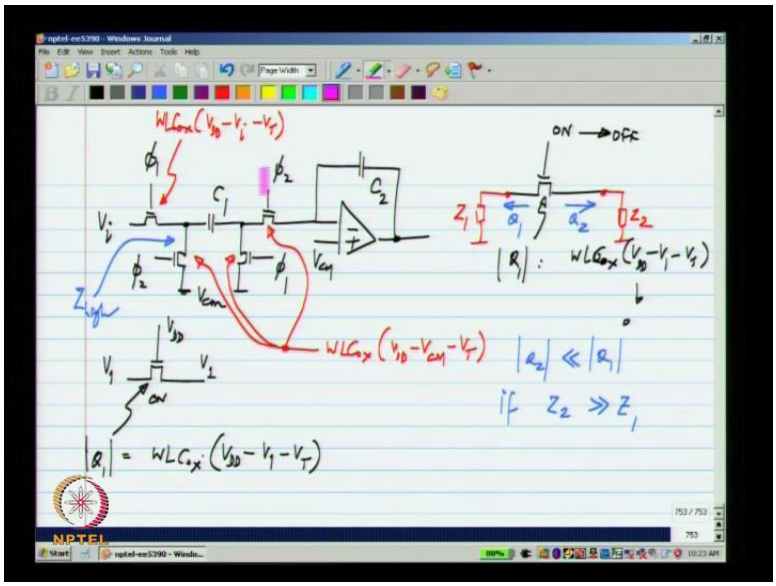

Now when you implement these with MOS switches I will show single channel switches everywhere does show that the diagram is simpler, but it understood that the input switches usually a transmission gate switch. These will be the common mode voltage of the op-amp and I am showing a single ended implementation, but it understood that we will in practice make everything differential. Now whenever MOS transistor switch is on that is lets an NMOS transistor whose gate is connected to V D D. So, this is on it will have a charge whose magnitude equals the gate capacitance times overdrive voltage.

Overdrive voltage depends on the voltage to which the gate is connected and also the voltage to which the drain and source are connected when it is on this voltage and that voltage will be approximately the same. So, i will call both of them V 1. Now if you examine the charge on each of these, this one will have channel charge which is WLC o x V D D minus the input voltage minus V T when it is on. And all of these things will have a channel charge that is V D D minus V c m minus V T. So, the important difference is that the channel charge of this is dependent on the input signal whereas, the chance charge of these switches is not dependent on the input signal its some fixed value. We cannot determine precisely what it is, but you know that it is some fixed value because the drain voltages are some fixed value V c m.

Now what happens when a transistor turns off remember when the transistor when this transistor turns off that is when the voltage across this is to the value of the remember the

sampling instant is determined by the turning a of this switch when the switch is turned on when phi 1 is high the voltage here is V i and here it is zero and when phi 1 becomes low these become open circuits, and the sampling instant is when phi 1 times low, at that point the value of V i is stored on this, but also what happens is when a transistor turns off that say it is on and it goes to off. So, this Q i will go from whatever value it had to zero. So, it has to go out of the drain and sues terminals, and it turns out that I will show whatever is connected either side by some impedances Z 1 and Z 2, and a certain amount of charge will go that way I will call it Q 1, and I will call that Q 2. The sum of Q 1 and Q 2 will be Q i. So, it turns out that the part that goes out Q 2 will be much smaller than Q 1 if the impedance Z 2 is much higher than Z 1.

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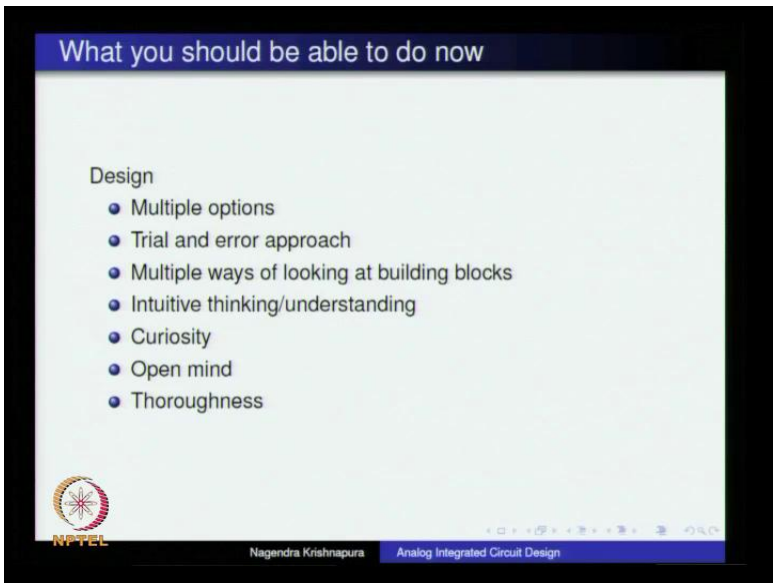

So the bottom line is charge tends to flow into the side, which has a lower impedance connected to it. Now there are papers, which analyze the phenomenon in detail you can consult them if you want the details with this, but the summary is that if you do not want the charge to go to someplace you would like to establish high impedance at that point. Now I just now said that when the switch opens the value of V i even established on the capacitor, but it is not just the value of V i any charge that flows out of the switch will also going set on the capacitor. So, the sample value will be error, and this happens everywhere you have switched capacitors any switch that turns of also injects an error charge into the capacitor, and exactly how much it is depends on the relative impedances and so on.

So, the main problem here is that the charge in this is dependent on the signal and it is usually not such a simple dependent it will have some nonlinearity as well. So, when you turn off this will switch you will get some error which is typically non-linear on C 1. So, in order for the charge from this not to flow to that side what you would like is to have a high impedance looking to the right that is looking that way you should have high impedance, and that can be established by turning of this switch whatever is labeled phi 1 here near the virtual round before you turn of that one. Although both are labeled phi 1 in practice what you do is you turn of this switch before that one. So, once this is turned off looking this way it is an open circuit, and when then you turn this off turn of this switch and most of its charge will go into the left side whatever is provided V i and nothing is going to C 1. So, the sample value will be accurate.

So, in general it turns out that the switches they are connected to the virtual ground should be turned off before the switches they were connected to the other side, the input side. Remember in some configuration this could be phi 1 and another this could be phi 2 and so on. So, it is very typical to have two versions of phi 1 that is you have something that turns hourly for the for use on the right side, on the virtual ground side, and you have something that turns of late for use on the input side. So, in a practical switch capacitor filter although we initially labeled everything with two phase phi 1 and phi 2 will have four phases.

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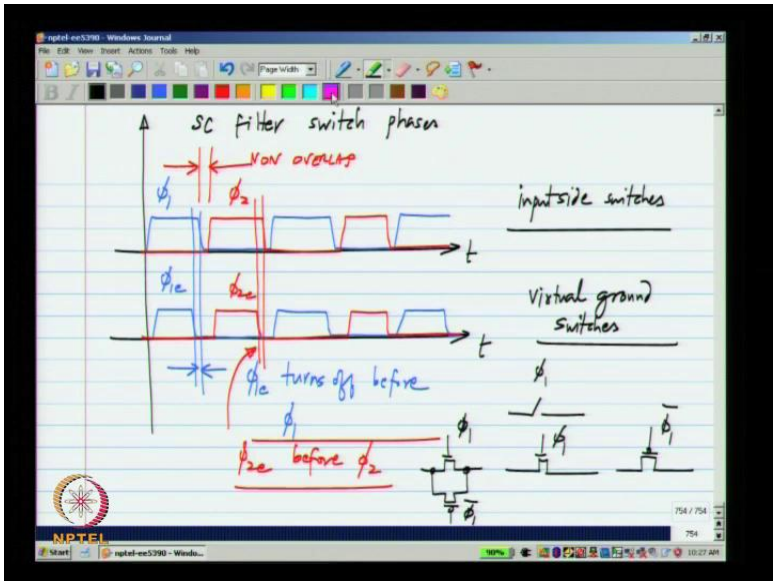

Now, first of all let say this is phi 1, and phi 2 will be like that, there will be a certain non-over lap and this is required because you see that this is phi 1 and that is phi 2 if the two or on simultaneously it will short-circuit the input. So that is absolutely unacceptable. So, there has to be overlap between phi 1 and phi 2. And top of it you also have two additional phases I will show it has a smaller than the other phi 1 it may call it phi 1 e and similarly phi 2 e. And the point here is to have a gap between these two phi 1 e turns of before phi 1 and similarly, your phi 2 e turns off before phi 2. And this is used for the virtual ground switches and this is used for the input side switches.

So, this is something very important in a switched capacitor filters you have to do this in order to reduce the errors you do what is known as charge injection this phenomenon of showed charge inside a MOS transistor coming out when the switch turns of is known as charge injection and charge injection flaws out of both drain and source, but it flows more into the side which as lower impedance. So, if you do not want the charge injection error to appear in someplace we should make sure that that side as a high impedance. So, that is the general principle.

And by the way these are the control voltages for an NMOS switch that is let us say when I have a switch labeled phi 1 what it means is that I could have an NMOS switch with phi 1 as the control voltage where phi 1 goes from zero to V D D or a PMOS switch with phi 1 bar as the control voltage or a transmission gate with phi 1 controlling the NMOS and phi 1 bar controlling the PMOS. So, you can see that although ideally you label the phases in the switch capacitor circuit phi 1 and phi 2 you can end up with a lot of phases you have phi 1 phi 2 and the early version phi 1 e and phi 2 e, and also the complemented versions if you have both N and P MOS switches. To that brings us to the end of discrete time filters we have dealt with them very briefly it is just an introduction that will help you start off with if you read other references question papers with this you should be able to at least understand how discrete time filters can be designed.

And then with a little bit of extra material you should also be able to design them and cannot simulate them there will be handout an addition to this course which will tell you how to stimulate switched capacitor of filters. The next thing that we look at is how to choose transistor sizes in a circuit we have made a number of circuits mainly op-amps and trans conductor and also transistors were use to make current sources, and so on. Now we have to choose transistor sizes and…

So, far we have use the square law model some kind of guidance what first of all we know that the square law model itself is highly oversimplified and especially when the channel lengths become very short is quite inaccurate. So, what is done in practice what a real designer would do is when you are exposed to some technology you first play around a little bit. So, that you get familiar with the parameters, and then when you want to start off designing some circuit you choose the sizes accordingly that is what I am going to outline in the next few minutes.

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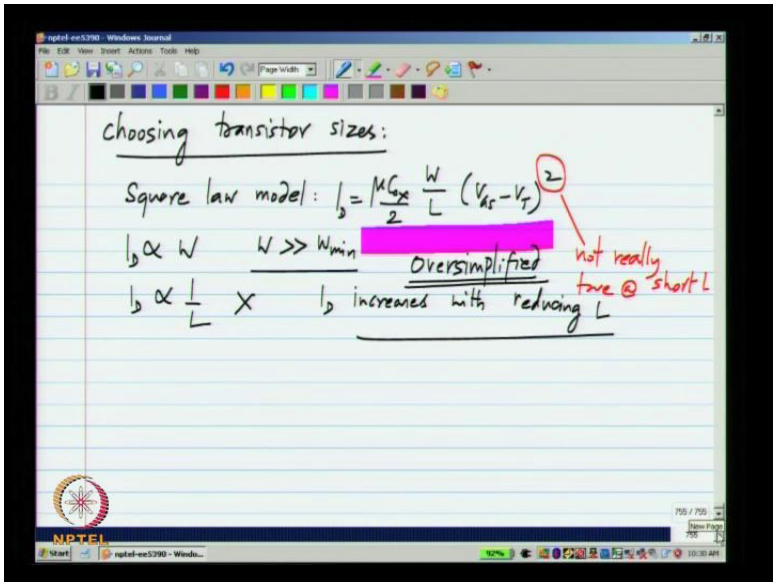

Now, the square law model it says that the saturation current in reality many of these things are highly inaccurate. First of all the square is not really true at short channel lengths, and also I D is proportional to W this is marvelous true when the transistor width is much more than the minimum width given in the given technology and this is usually true for analog circuits, but this the inverse proportionality L this is not really true it is true that I D increases if you reduce L, but it is not true that its exactly in inverse proportion.

And then of course, this is highly oversimplified as well. So, what should you do what you must do is essentially calculate the g m and other quantities of interest for a transistor using a simulator over a range of bias currents, and this is something that you have to do anyway initially when you are exposed to a new technology you do this. So, that you get familiar with the possible parameter ranges and then you choose the

transistor sizes properly. Now what parameters are interested in usually g m is of primary interest because in analog circuits you have gain to be g m times r L on a common source amplifier or g m by c as unity gain frequency of an op-amp and so on. So, g m is definitely of primary interest now another quantity of interest g d s or many times you can think of g m by g d s which is the inherent DC gain of a transistor this appears as a DC gain of op-amps and so on. When it is loaded by itself that is when it is not operating with an external load. So, that is another quantity and also you have to be worried about swing limits that is headroom issues, so V G S minus V T and the absolute value of V G S or other quantities of interest.

Because these will tell you how much room you have after allowing for these things for the signal swing and finally, you have f T or g m by C g s as quantity of interest f T does not directly tell you what frequency the circuit will operator at, but it will only give you a guideline that you have a larger f T your circuits frequency operation could potentially be higher. Now typically datasheets that tell about a technology also list the value f T usually a single number is given, but this is not very useful because that is evaluated with the usually an unrealistically large value of V G S and V D S and so on. So, again you evaluate this with the values of V G S and V D S that are reasonable now.

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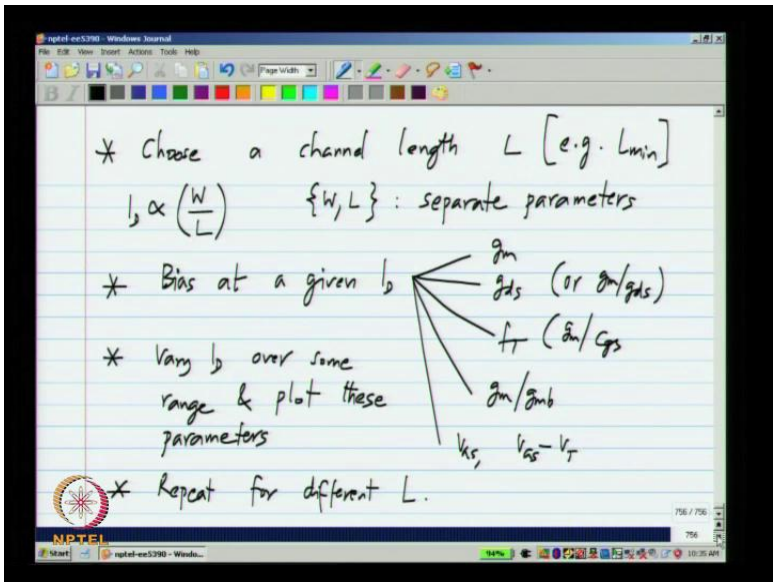

How do we go would doing this, first of all you choose the channel length. Now again as I said although the square law model says that I D is related only to the W by L ratio it is

best to think of W and L as two separate parameters. So, you choose the channel length L based on some criteria I will come to those things, and then you can scale the parameters based on W because I D will be proportional to W. For instance let us say you start with the minimum channel length in some technology. And then you bias at a given I D and determine many parameters let us say g m and g d s or g m by g d s switch is an indicator of the DC gain and f T or gm by c g s and some time you may also be interested in g m by g m b that is the bulk trans conductance, and also V G S and V G S minus V T and these are usually have interest for the swing limit. And then you vary I D over some range and plot these parameters.

Now once you do this you will get an idea of how much g m you will get for what I D and what is the kind of g m by g d s you can expect and so on. And, this process has to be repeated for a different length let us say you find that the g m by g d s is rather inadequate then you have to increase the channel length and do this. So, typically what I would do and what I would recommend the duo also do is you choose the minimum length and may be twice the minimum length four times the minimum length etcetera and then list all these parameters are plot all these parameters versus bias current, and then you will get an idea of what possible g m s you can expect, it also tells you whether you will be able to accommodate that in a given supplies because you also plotted the V G S and V G S minus V T and so on. So, just to give you an illustration let me write down the final step here.

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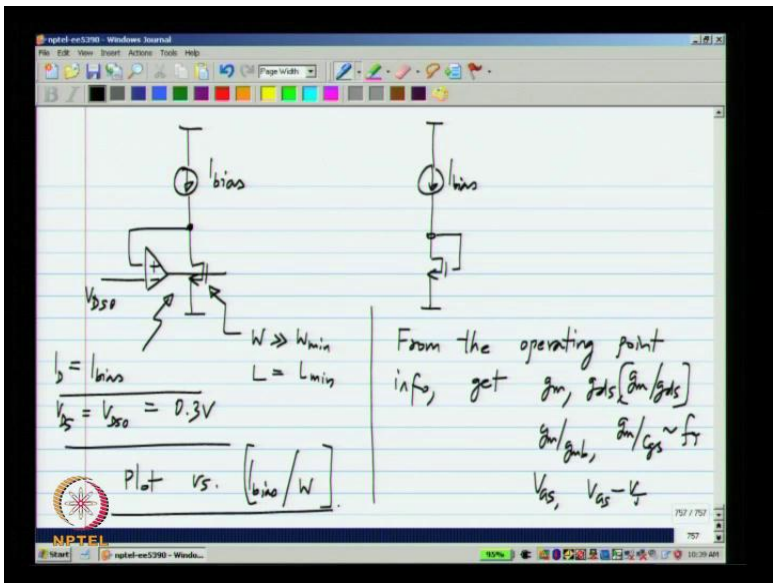

Now how do we go about simulating these things first of all you can bias the transistor at a given current using negative feedback. So, the transistor is real typically you choose something W much more than W min and L of whatever value you want. So, let us say I start with L equals L min and I will bias the transistor had a particular V D S that I would like to have the reason is that I could have done this as well.

Now if the current happens to be rather large what happens is that you will end up with the very large V G S usually you do not bias the transistor and an analog circuit with the very large V D S. Now you could do that the reason you do not do it is you have as much headroom as possible and when you reduce the V D S it does have some influence on the parameters. So, typically you do this with reasonable value of V D S keeping that fixed although there is nothing long with using a divot connection.

So, once you have this then this will get biased at a drain current of I bias V G S will get adjusted by negative feedback, and let me call this V D S zero V D S will be V D S zero, which you could choose to be a relatively marvelous value of let us say 0.2 V of 0.3 V. So, then depending on your simulator you could do various things first of all typically this simulator will let you evaluate the operating point simulate the operating point and report the value of g m. You can get g m and g d s also and of course, from these you can calculate g m by g d s you can also calculate g m by g m b if that is of interest to you and you can also calculate g m by c g s which is approximately the f T and this f T is evaluated with relatively small value of V D S, and also not the highest value of V G S that is possible, and you can also report the value of V G S and V G S minus V T.

And you can plot this you can plot versus I bias that is usually that have better to plotted versus the current density that is I bias by W. Because as I said repeatedly all these things will scale right if you double the value of W keeping the V G S as the same and V D S as the same, you will double the value of the drying current you will double the value of g m, f T will remain the same and so on. So, you plotted versus the current density essentially you should tell you what current density to bias to get what value of f T, and then g m and I D can be scaled from this.

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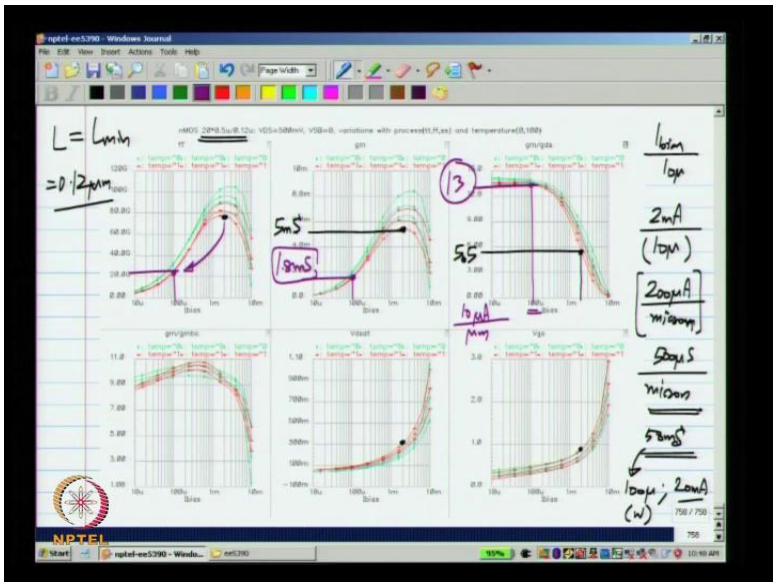

I will show on example of this which as evaluated for some particular process. So, this is exactly what I meant. Here X-axis is shown as I bias and this is for a un-micron wide device. So, the current density can be calculated as I bias divided by 10 micron. So, I will can said you could plotted versus the bias current per micron or versus the bias current itself you are worry does not matter because everything will scale with the width. Now what are these different curves the first one says it is f T, the second one is g m, the third is g m by g d s, fourth is g m by g m b s and V d sat and V G S and so on. So, let me start with the g m curve what it say says for this particular transistor. As you increase the bias current g m will increase, but after certain point it is start decreasing this is partly because a transistor tends to going to a try out reason as well the V G S starts increasing beyond a certain value.

And also as you increase the value of I bias the f T value goes on increasing, and if you are operating at high frequencies you would like to operate with as I f T and as possible. Now I said f T does not give you directly what frequency the circuit will operated, but it essentially use full the relative size of the parasitics if you have a large value of g m by C g s of the transistor; that means, that the transistor parasitics are relatively small that is one way of thinking about it. So, at high frequency you would like to have large g m by C g s. So, that it can drives on external capacitance or even the internal capacitance can be driven faster. So, this gives you an idea of what f T to operated.

And similarly the value of g m by g d s tells you what value of DC gain you can get if you bias this with current source that is an ideal active load. Now you can see that this by the way for transistor length which is the minimum in this particular process which happens to be 0.12 micrometers, and you can see that the maximum value of g m by g d s is only I wrote 13 or 14, and it keeps falling as you increase the value of I bias it is constant up to some value and then it keeps falling this is again this typical if you try to operated a very high current density you will end up with a rather poor DC gain.

And g m by g m b s this tells you how much the influence of the back gators this may be of interest in cases where you have body effect in this case the g m b s is rather small compare to g m. Now the other important things here are the V d sat and V G S. So, what do these things tell you let see you choose the peak of the f T curve that is you choose to bias effect two million for 10 microns that is you choose to bias effect two million for 10 micron width, and this part is 10 micron because that is what I have simulated. In fact, the better way of thinking about this is to think about as 200 micro ampere per micron width.

So, it looks great because you get the highest g m by C g s that is possible, but if you look there at two million, the V G S value can be as highest 0.9V source now that may or may not be acceptable for you. By the way you see there are many curves here there are three green curves and three red curves. Now as I mentioned in in earlier lecture dealing with the CMOS process there will be process variations.

What have plotted here is for different process corners and also for different temperatures. Now you do not have to do it for every possible corner here the green curves corresponds to a low-temperature of 0 degrees and the red curves correspond to a high temperature of 100 degrees. The reason to do this is that you also have to deal with the worst-case scenario you can see that f T is low at a high temperature. So, this is what is going to be limiting your performance right, and gm is also low at a high-temperature and so on.

So, if you do not want to calculated over all the process corners and temperatures at least you could do it over the worst corner, which is typically called slow corner where the mobility is rather low and also at the highest temperature which could be 70 degrees or 100 degrees based on your interest, and you can do it for the worst-case because there is

no point simulating in the best case and then you simulate in the other corner and finding that the circuit does not go any more. So, you should have an idea of what the worst-case is even before you start to design.

So, here you see that the transistor V G S is rather high and if you go to the higher current density it will be even higher the transistor V G S is even higher and you may or may not be able to accommodate that much V G S similarly, V d sat here is at this current density is about 300 milli volts. So, if you acceptable that is fine you could bias it and have relatively high-frequency performance from your circuit otherwise you will have to back down from the peak current density you have to biased it see 100 micron appeared for micron or something lower.

Now what else can you do with this. So, let us say you clue individuals to bias here. So, this gives you a g m of 5 milli siemens that is for 10 micron width. So, you can think of it as 500 micros siemens of g m for a micron of width. So, depending on the g m value that you want you scale up the width. So, let us say you are interested in an transistor with the 50 milli siemens g m what you must do is choose a 100 micron width and choose a bias current of 200 micron ampere per micron times 100 microns which is 20 milli amperes. So, that is how you would use these curves. So, like I said generating this curves itself is an educational experience you should do this for a given process then you get a feel for this process. Now you having done all this then you look at the value of g m by g d s you get is rather miserable it is just about 5.5 also. So, even if you bias this transistor with an ideal current source active load the DC gain that you get will be 5.5.

And this could be your limiting factor in some cases it is not that in every case you would like to maximize f T or a g m a given current what you may want is high DC gain. So, for that reason you may have to choose smaller bias current, smaller bias current density what is important is the current density that is current per micron of width. So, let us say you would like to have as high DC gain is possible then you would choose a different operating point. So, let see somewhere here this is 100 micron ampere of current per 10 micron width or corresponds to 10 micron ampere per micron, and in this case you will get a DC gain of about 13 which is still relatively low value, but higher than before.

Now if you go back and look at the value f T, now I see that you come down significantly from there, and you solves the illustrate the trade of if you would like to have a high DC gain you will end up with a slower device. So, that is another issue and similarly, you will have a g m that is rather small you will have to leave with this value of g m instead of 5 milli siemens it is may be 1.8 milli siemens for so. So, this is for the minimum length and as you know if you want a higher DC gain typically you would not choose the minimum length you would choose longer transistor.

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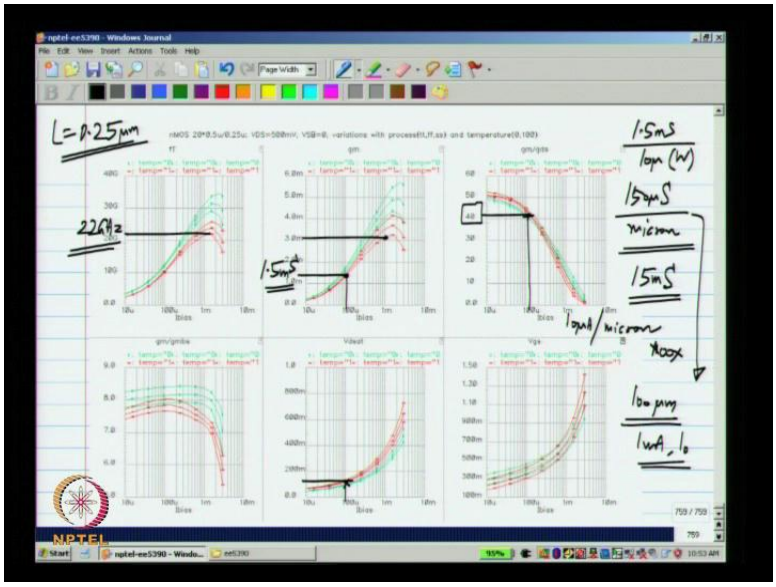

So, what I have done is also evaluated this for approximately twice the minimum length and that is 0.25 microns. So, you notice many things immediately. First of all previously the peaks of f T and g m are occurring somewhere around bias current of 2 millions that is 200 microamperes for microns. Now here they occur slightly earlier and also the values are lower. So, you see that this worst-case peak f T is almost 75 gigahertz here whereas, here the worst-case peak f T is some 22 gigahertz. So, you do fall significantly in the peak f T when you go to a longer channel length similarly, if you look at 1 milli ampere bias current or 100 microamperes per micron of bias current the g m value here was about 5 milli siemens whereas, here it is about 3 milli siemens again I am only looking at the worst-case there are this curves here for three corners and two temperatures.

But worst-cases what matters similarly, again you see that for 1 milliamp already you reach V G S. Of 800 milli volts of source and so on, but what is the advantage of going to l equals 0.25 micron the highest g m by g d s that you get is lot higher where as previously you are limited to about 14 now if you operate with a 100 micro ampere bias current which corresponds to a 10 micro ampere per micron width you will get a DC gain of 40 which is a not higher than before. So, if you want a large DC gain. So, let us say you are designing cascade op-amp where the DC gain is the order of g m by g d s square and the DC gain you required was of the order of 1000 clearly each transistor must have a g m by g d s which is 30 or 40 or even higher because what appears is not just the g d s of a single transistor, but of many transistors.

So, you would have to choose a longer channel device, but this also means that he will be compromising on speed. So, this is a trade of that you cannot avoid, but this curves will help you a figure out which transistor lengths to use and then from where you can scale up for a given g m. So, let us say you have decided to operate where the g m by g d s is around 40 that is 10 microampere per micron so; that means, that will be operating somewhere here. So, this is let us say this is about 1.5 milli siemens it is a little less than that, but I will approximated 1.5.

So, I have 1.5 milli siemens for 10 microns of width. So, that is 150 microns siemens per micron width. I would like to keep the same DC gain g m by g d s, but I want a higher gm let us see if to obtain the desired unity gain frequency in an op-amp then. So, let us say I wanted 15 milli siemens what I would have to do is use under micron width because I have to scale this up by factor of 100, and also I have to scale up the current density by a factor of 100 I am operating at 10 microampere per micron and I have to operate this at 100 times higher current that is 1 milli amps of I D and at that point my V G S minus V T will be around 150 milli volt which is usually rather acceptable value and you can comfortably bias the op-amp. So, this is how would you use this shot of cheat sheets right.

Now, if you look at the literature there is something known as the g m by I D methodology, and it is something similar what you plot there is just the value of g m divided by I D versus the V G S or V G S minus V T. Now you can do that that the information that we will not get from there is the value of the inherent DC gain of the transistor that is information about g d s and so on. Now whichever you choose to use

you have to generate this plots yourselves there is not much point looking for this plots for a given technology it is only by playing around with the technology yourselves that you will get a feel for what the process can do, and where to bias the transistors and this simulations are rather simple and or an interesting way to get started with the process, and also get useful information. Of how to start up your design just for completeness I will show you the curve for.

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An even longer channel transistor in this case I have used approximately four times the minimum length or 0.5 micron and the width is the same and you see that the peak f T comes down even more, but the reason for going to a longer channel is the higher DC gain and you can see that you can get a DC gain of almost 80 75 are so, in the worst-case. So, if you want higher and higher DC gain you have to longer and longer channels, and there is no end let us say that you are looking mainly at DC gain performance and primarily not at speed then you can even increase the channel length and do this ah simulations. Once you do it for a few different channel lengths you will get a feel for what you have to do and you want a DC gain beyond the values that are given by.

Whatever your simulated then you go to anyone longer channel length. So, that is quite easy you have to do this for both PMOS and NMOS. So, that you have information an both because many times you use a PMOS input pair and NMOS input pair and a different loads and so on. So, I would say that whenever you are introduced to a new

technology a good point is start-up with is to generate these curves of g m. g m by g d s and f T and also the bias values of V G S minus V T and V G S for different current densities, and you should try and similar these things with width that is much more than the minimum width because that is where the scaling with the width is valid, and it is also convenient if you plot these things versus the current density that is the current per micron of width rather than the current itself as I have done, and then that will give you a good starting point for value of designs. So, that is out off brings us to the end of the course.

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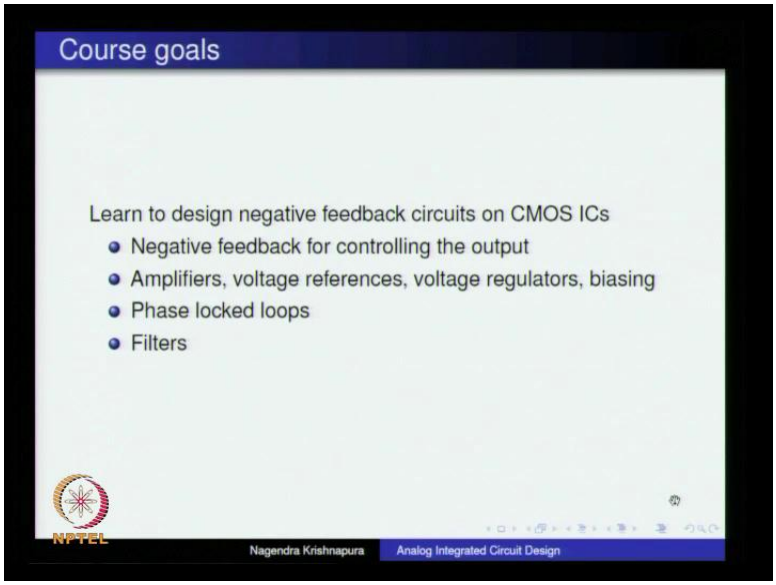

I will quickly summarize what we have done in this course and rapid up. This is what we start of course goals we wanted to learn about how to design a negative feedback circuits an CMOS IC's. Basically you look at the principal of negative feedback for controlling the output to a desired value then design amplifiers and voltage references and some other circuits mainly I learn the design of op-amps and also we wanted to see how to make phase lag proofs are basically frequency generation circuits using negative feedback and then some kinds of filters, now what I have actually done.

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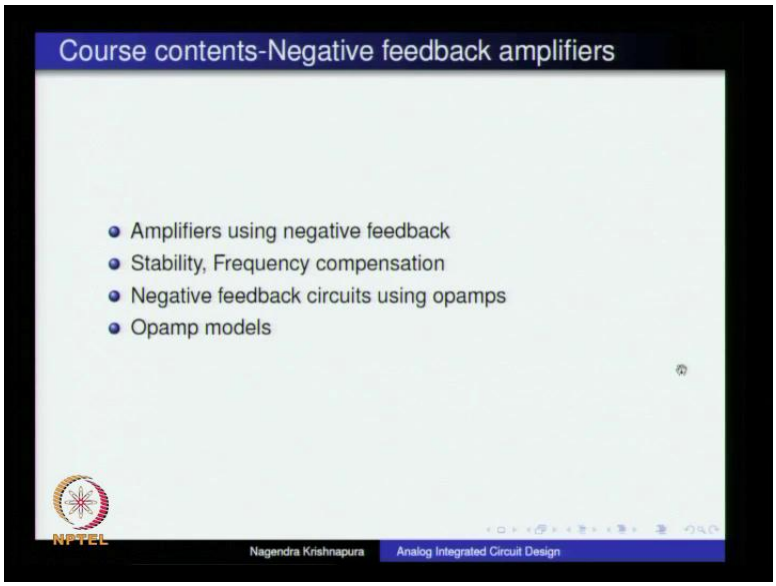

We did go through in great detail about negative feedback amplifiers is. So, how to design amplifiers using negative feedback and dealt with stability, and how to frequency compensated that is to configure the negative feedback loop for stability then we saw negative feedback circuit using op-amps and op-amp models that you can use.

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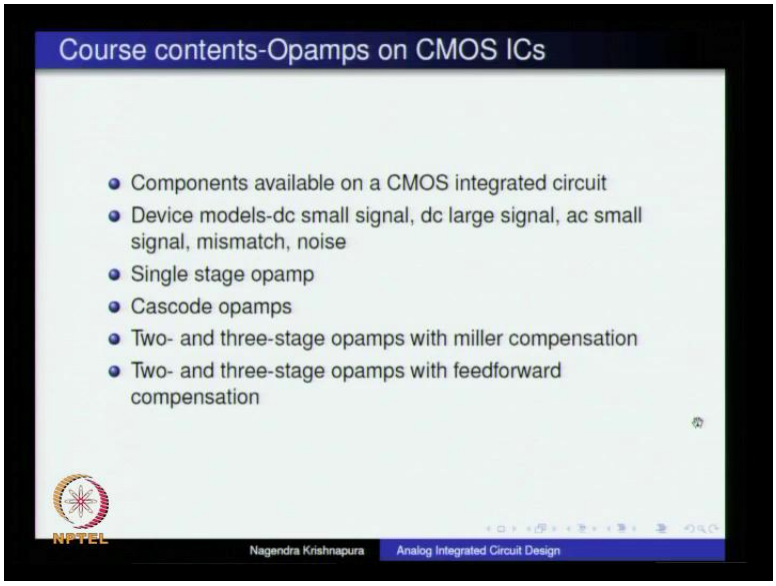

Then you saw how to make op-amp on CMOS IC's to do that first we went through the components that are available on a CMOS integrated circuits, and the device models that you can use for the CMOS transistors, and also some things that you would probably not

be familiar with earlier, but the relevant to IC design such as miss-matching noise when we saw number of different kinds of op-amp. So, single stage op-amp on cascade op-amp which gives a higher DC gain and two and three stage op-amp with miller compensation and two and three stage op-amps with free forward compensations different structures for getting higher and higher DC gains while meet any stability. When we look that fully differential op-amps common ways of analyzing fully differential circuits using differential common mode half circuits.

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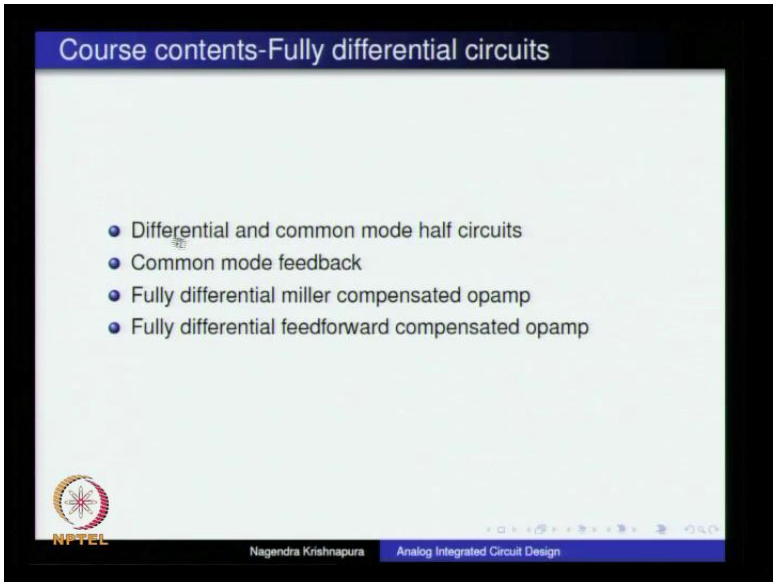

And common mode feedback which is an essential part of wall fully differential circuits and fully differential versions of the miller compensated op-amp, and the feed forward compensated op-amps.

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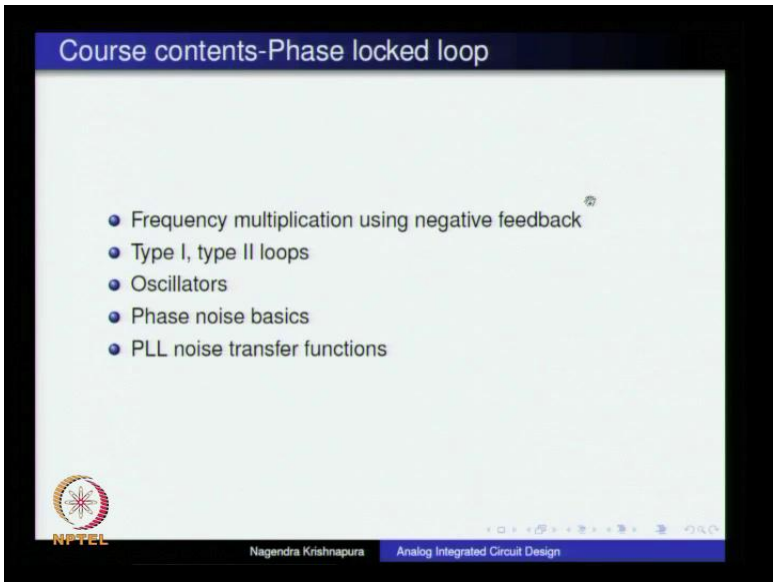

When we looked at the phase lag loop as a problem of frequency multiplication using negative feedback that quickly broad us to type 1 loop, which was rather not practical and the typed loop which is widely news any way briefly looked at accelerators and also the phase noise of accelerators and. So, on and we also looked at the noise in a phase lag loop. The noise in a phase lag loop is in the phase do mine and it somewhat distinct from the voltage noise that you are familiar with in circuits. So, we knows how to calculate those things and how to interpret the phase margin.

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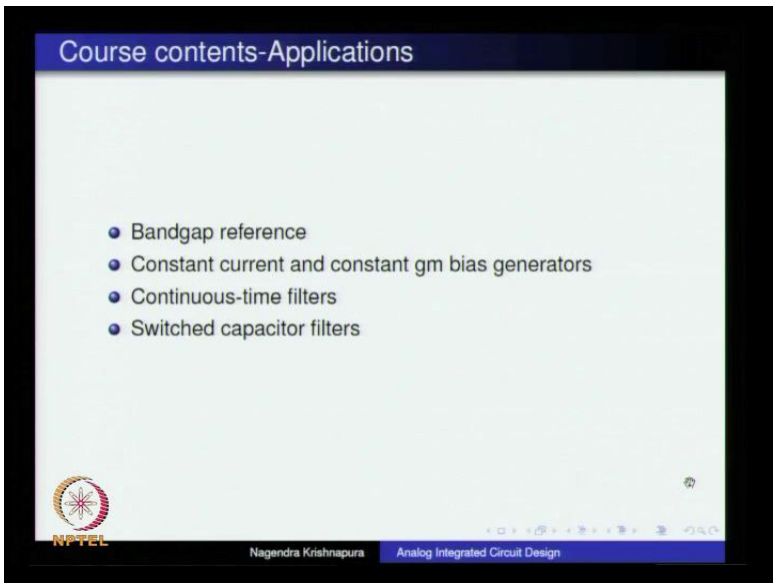

Even came to applications we dealt with how to make a band gap reference that is constant voltage reference on an integrated circuit we also looked at how to make certain types of current references that is current references which are proportional to absolute temperature and which result on a constant g m when you bias MOS transistors and. So, on then we also very briefly looked at continuous time filters and Swiss capacitor filters. So, finally, the point is what should you be able to do.

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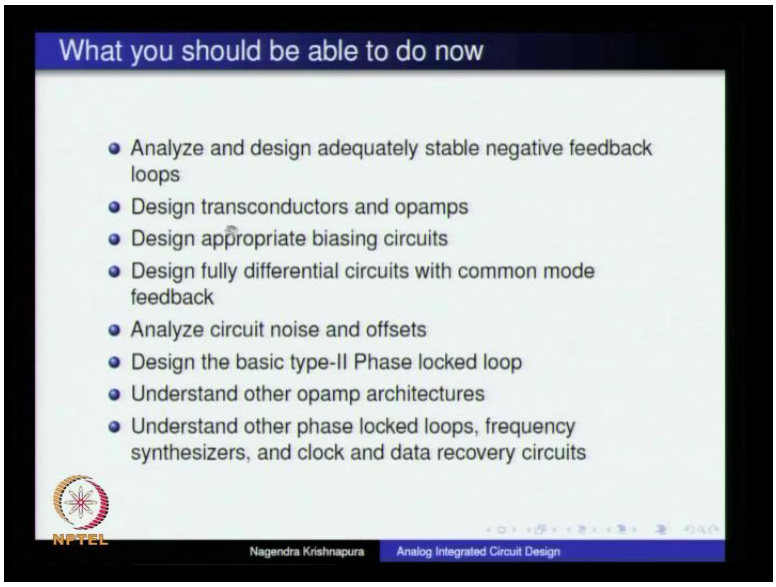

Now if you are followed the course properly you should certainly be able to analyze and design adequately stable negative feedback loops, and design trans-conductors and op-amps and also appropriate biasing circuits for the these or any other circuits using transistors. You should also be able to design fully differential circuits and design common mode feedback circuits for them. And also you should be able to analyze circuit noise and offsets based on the noise models, the type-II PLL something that we dealt with in detail.

So, the basic type to PLL you should be able to do and simulating the phase do mine, and if you come across other op-amp architectures I think based on this you will be able to understand with the little bit of work and perhaps, also understand other phase locked loops which may have some more details and refinements, frequencies in the synthesizers and clock and data recovery circuits. These are a type of phase locked loop

used with not periodic input signal, but with a random data input signal when you want to extract the clock that corresponds to the data.

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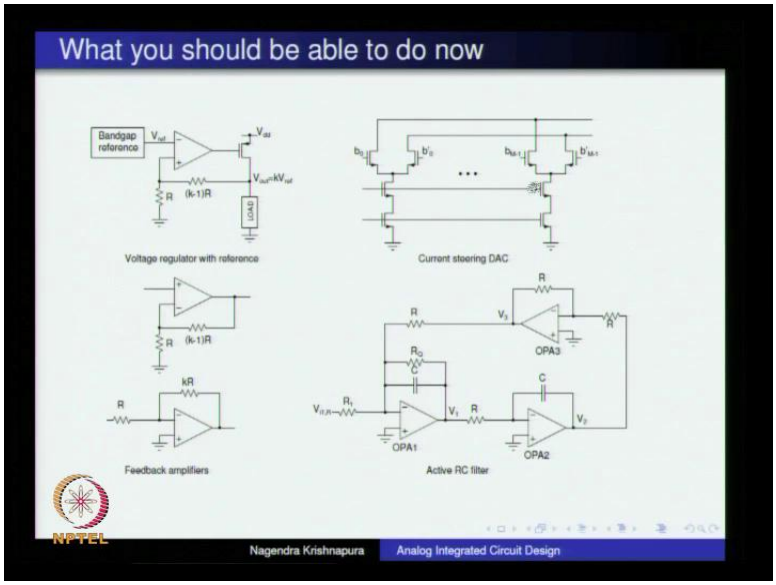

Here there is a some examples of circuits, this is voltage regulator with a band gap reference you would be able to in principle design this based on what you know so far. And this is something that we are not dealt with at all a current steering digital to analog converter, but basically it is a bunch of differential pairs and again you should be able to design these things. So, that it was properly in feedback amplifiers of course, and then the continuous time filter.

So, the bottom line is you should be able to do some design beside the specific technical knowledge that you acquired for design you should be comfortable with evaluating multiple options because there is no real one good option there are many topologies is the different people have investigated, which are suitable for different contacts and find you may have ourselves find that when you go from one process technology to the another some topology is better than the what you used in the other process and so on. So, what you need is basically short of mental flexibility you should have multiple options on your hand you should also be comfortable with trial and error approach because you may not be able to analyze everything completely before the start of the design. So, design into little bit and see how it goes, and come back and it right and so on.

And multiple ways of looking at building blocks, so that you understand them thoroughly and you should also develop inclusive thinking on understanding and this is kind of related to what I mentioned earlier if you understand the same circuit from different points of view you also gain valuable intuition about its operation. And finally, is the last three are very important for design and especially for coming up with new designs that may not have been done before at all.

First of all curiosity otherwise we will not be able to look at new things at all you should be open-minded that we should not be. So, rejected about some circuits that you already design you may you should be open to the possibility that there may be some other circuit that will work better in the given in the context and finally, it is have two thorough because many time superficially you can come up with a circuit idea, but you have too evaluated thoroughly to see whether it really fits in with the application that you have in mind. And there are other op-amp architectures.

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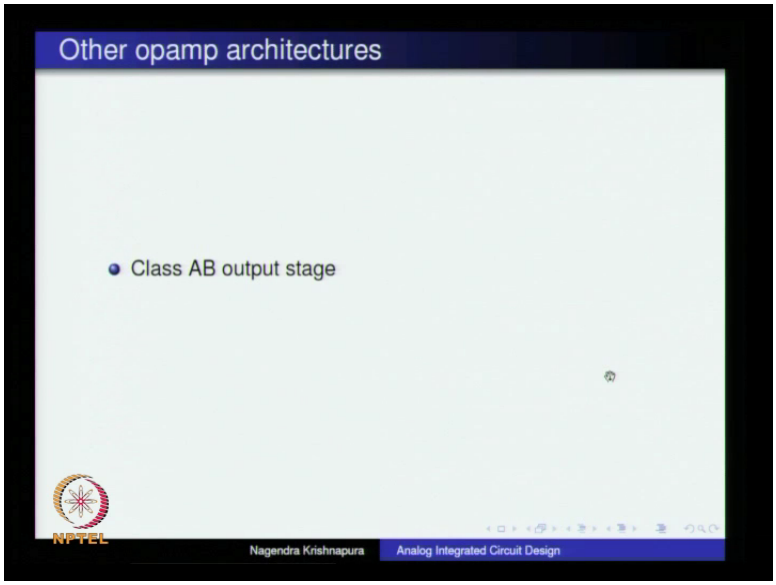

I will just mention the class AB output stage this is something that we did not deal with in this course is mainly used when you have to deliver a very large load current this is the op-amp that we have discussed in the course in great detail the two-stage op-amp.

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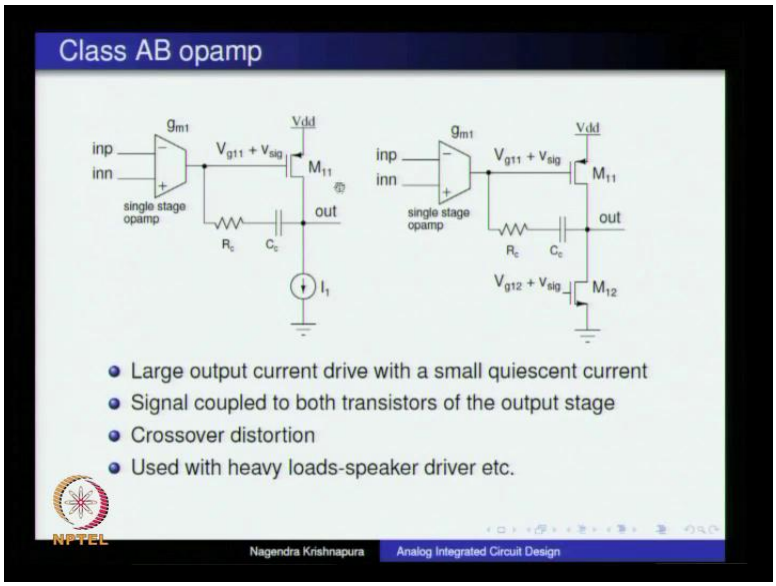

The single stage op-amp is shown as a trans conductor here, and it has the second stage main point is that the bias current of the second stage is fixed. So, if you have to deliver a large current this I one as to be more than that very large current. So, that leads to a very high quiescent far dissipation of the op-amp. So, the basic idea behind the class heavy op-amp is to not used a fixed current source here, but use a current source that is dependent on the signal. So, if you have a large signal you make this current source large and if it is the signal is not there you keep it at a small value. Now in our traditional op-amp only the gate of a transistor M 11 received the signal now M 12 also has to receive the signal around a different bias voltage V g 12, you cannot simply connect this to that one that will also lead to a very large current. So, there are many arrangements to do this.

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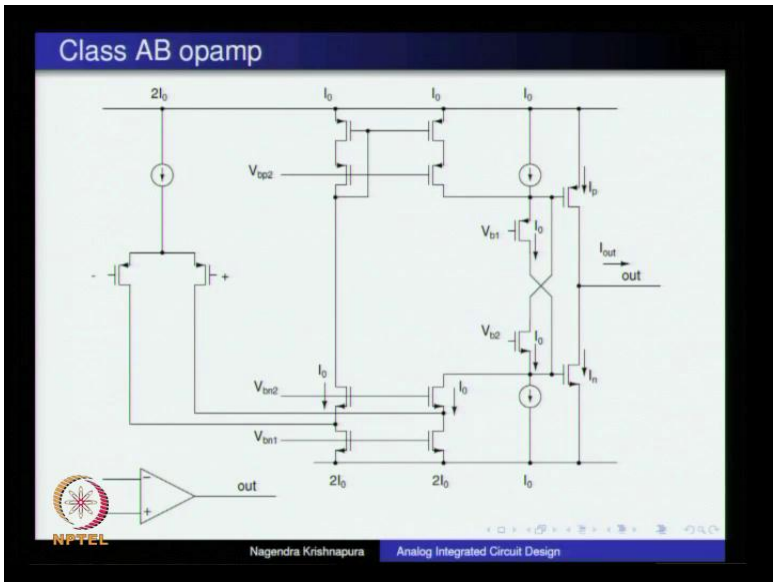

But one classic arrangement is what was publish I initially by denni spontyselly it is a particular kind of biasing circuit which you apply the signal directly to the NMOS transistors here, and it also gets of converted to the PMOS, and it turns out that you can adjust the kaizen current independently for the output branch.

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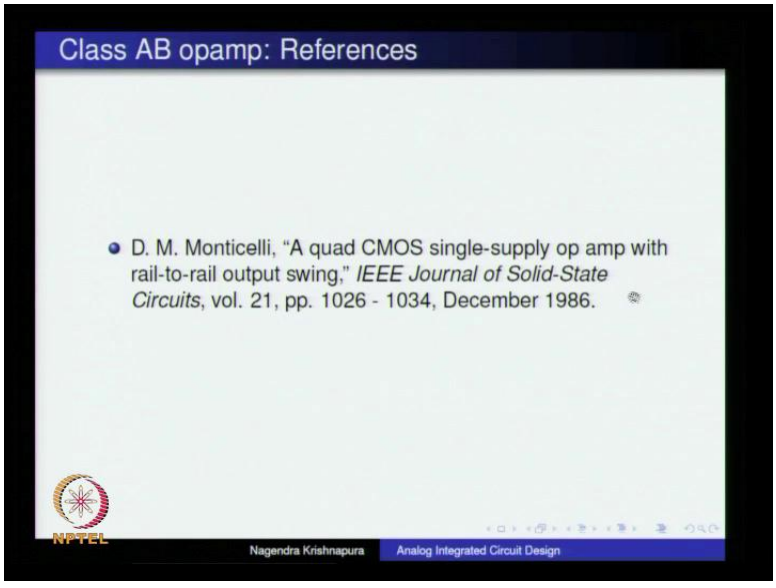

Based on this one and you can see the details in this particular paper. So, this is a particular op-amp of tremendous practical interest that you can look up in the references

and the basic principle is exactly the same as what we have done before the output stage is different and the operation of that you can look at from this reference.

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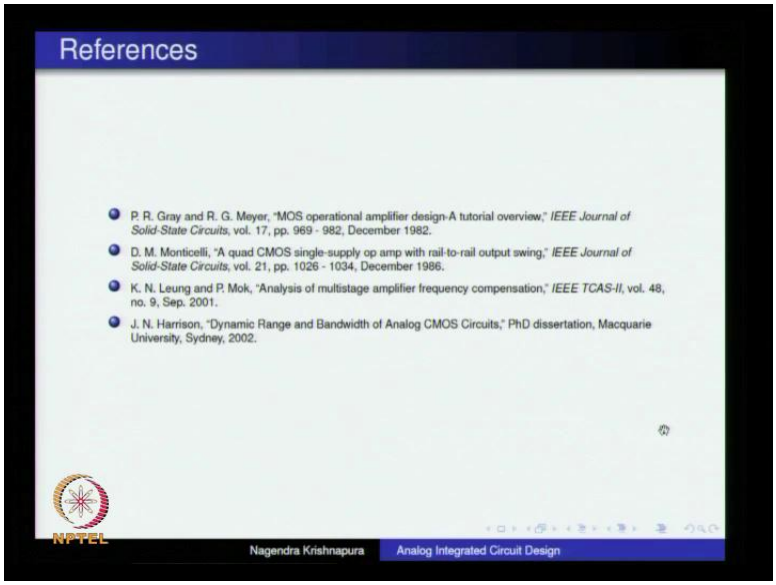

And many other references in the literature, and these are some general references you can use this is a classic tutorial an op-amps which is still rather useful and this is about the class heavy op-amp, and this the third one is in particular about ah op-amps with multiple stages and then the last one is about feed forward op-amps.

So, that brings us to the end of the course now besides these there will also be a detailed handout an op-amps and one one phase locked loops that you can refer to hope you enjoyed the lectures thank you for listening I also like to end by thanking the imperial star for facilitating, the recording and editing and so on. They have come during all days including Saturday's in order to do this it is a lot of work and I would like to in particular mentions Sergio Francis for going through the painstaking job of editing all my lectures.

Thank you have fun.