Analog integrated Circuit Design
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Lecture - 56
Low Dropout Regulators;
Continuous-Time Active Filters

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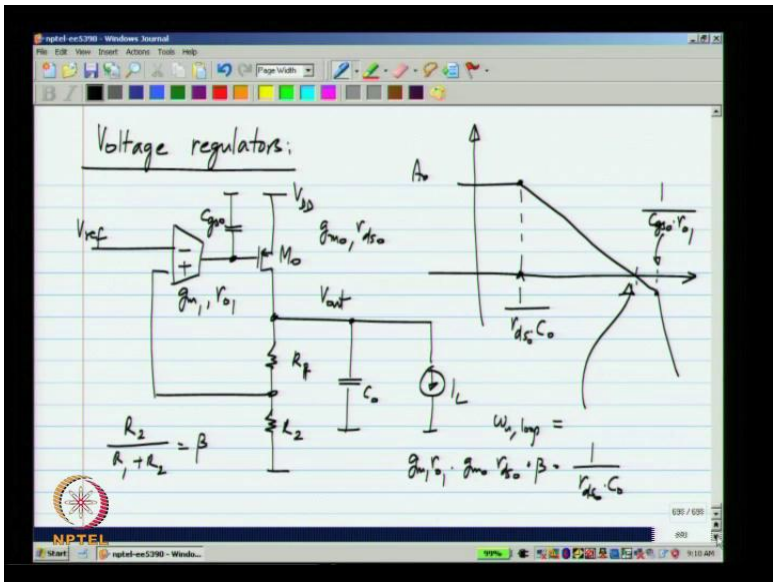

Hello and a welcome to lecture fifty-six of analog integrated circuit design, we are discussing voltage regulators and stability constraints will continue from that point, we have the transistor M0, which is usually called the past transistor we have a feedback voltage divider. So, that we can get the required output voltage and a reference voltage that comes from a ((Refer Time: 00:51)) reference load current we have an output capacitor that is required in order to limit the transience when IL steps up or steps down, and one of the other imported polls is caused by c g s0 the capacitance of transistor M0 is amplifier n the feedback loop is said to have a trance-conductance g m1 and an output resistance r o1.

And this M0 as some g m0 and output resistance r d s0 at the operating point. So, we evaluated the frequency response and saw that the dominant for likely to be from the output node this is A0 this is d c loop gain and this poll will be at approximately one by r d s0 times C0 it will have a minus 20 degree per decade val of, and for stability the poll

introduced by this c g s0 must be beyond the unity loop gain frequency, and this poll is going to be at one over c g s0 r o1, and the unity loop gain infrequency will be at n0, which is g m1 r o1 g m0 r d0, and this ratio R2 by R1 plus R2 I will call this beta times the value of the whole, which is one over r d s0 C0.

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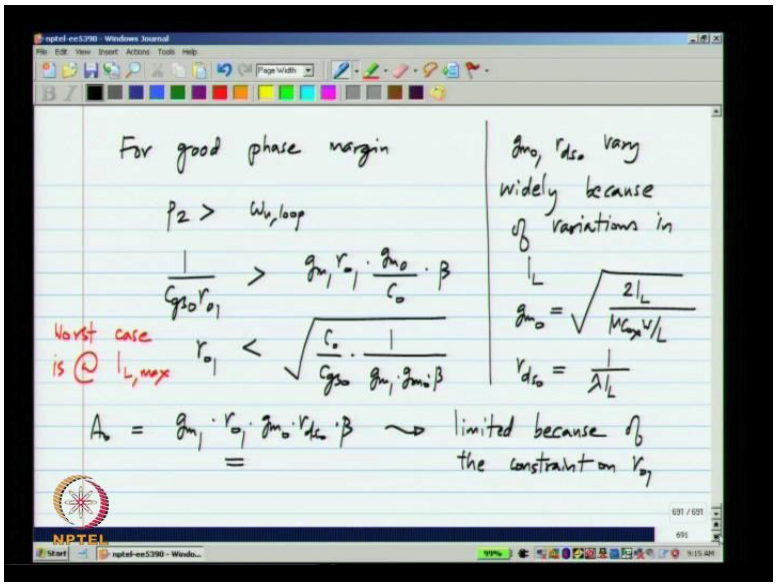

And we know that for good enough phase margin was stability we would like p2 to be more than omega u loop here I will not specify how much more, but I will just work with any qualities. So, this basically says r o1 less than some value, which happens to be. So, now, because the value of r o1 is limited we can only have a certain d c loop gain is g m1 r o1 g m0 r d s0 times beta, and because the value of r o1 has upper limit we can only haves a certain value of d c gain it limits the dc load regulation we saw that the load regulation basically is represented by the closed loop output resistance of a circuit, which is r d s0 divided by one plus d c loop gain, d c loop again will be limited, because the output resistance of the amplifiers r o1 has to be limited to a certain value, if that value becomes very high the poll associated with c g s0 will move low frequencies, and the phase margin will be very poor.

And also the other thing is that in a normal amplifier we have the operating point and more or less we can think of signals as a small variations around the operating point even with the amplifiers that operated with fairly large signals many of the crucial parameters can be still considered constant, but in a voltage regulator that is not the case the

coefficient current flowing in the voltage regulator must be very small, and the load current can vary all the way from zero to some very high values. So, this means that the value of g m0 and r d s0 that is the small signal parameters of the transistor M0 can very, very widely.

So, g m0 would be related to if the transistor obey squire law and r d s0 is lambda L they all different kinds of variations that is r d s0 is one over lambda IL. So, r d s0 as inverse proportion inverse relationship with IL and g m0 as the squire root dependence on IL, but the bottom line is gm0 will increase and V d s0, which is the reciprocal of r d s0 will increase with increasing IL, if look at this condition has to be evaluated at the worst-case, and the worst case is at the maximum value of IL, because that is when g m0 will be maximum.

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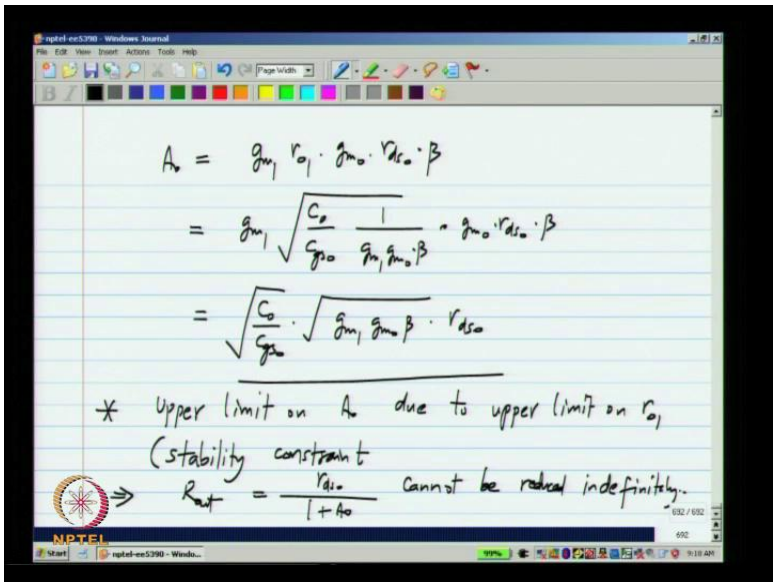

Now, if you expand the relationship for A0 will get g m1 r o1 g m0 r d s0 times beta, which is basically g m1 square root of c0 by c g s0 times one over g m1 g m0 times beta, which times g m0 r d s0 beta, which basically translates to squire root of c0 by c g s0 times square root of g m1 g m0 beta times r d s0 again you see that the worst case of this is for high values of IL for large values of IL g m0 will larger, and r d s 0 will be smaller, but gm0 as a squire root dependence on IL whereas, r d s as a direct dependence on IL. So, this A0 if you look at this constraints will reduce with increasing IL for a given gm1 now, of the other question is why cannot, we just increase gm1.

Now, that is possible, but depending on the amplifier structure it will be limited, because you would like to limit the kaizen current in the amplifier that is, because there is a wastage current you would like the total current to be almost equal to the load current. So, under those constraints it becomes further to increase gm1 now, there are possibilities you can have slower amplifiers with over all higher effective g m1 and. So, on in this case what I was as assume is that the amplifier is a simple differential type of trans-conductors. So, under those conditions the worst-case was stability is when IL maximum and also the output resistance of the amplifier must be limited to some value, which means the d c loop gain limited, which in turn means that the load regulation is limited to certain extent. So, these other the constraints, which resulting from the stability constraints of this feedback loop interns out reality even more complicated than this.

Now, this value of IL can be very large; that means, that the value of C0 as to be also very large now, as you know the capacitor as there is no such thing as a pure capacitor it will always have a serious resistance under serious inductance, and how much serious resistance you have really depends on the physical size of the capacitor, and larger the value of capacitor will larger the physical size, and you get a larger effective serious resistance it is termed as s r or effective series resistance. Now, if you look at the equal ant circuit of a capacitor ideally it is supposed to be like that in reality you will have effective series resistance and all the effective inductance, and this capacitance C.

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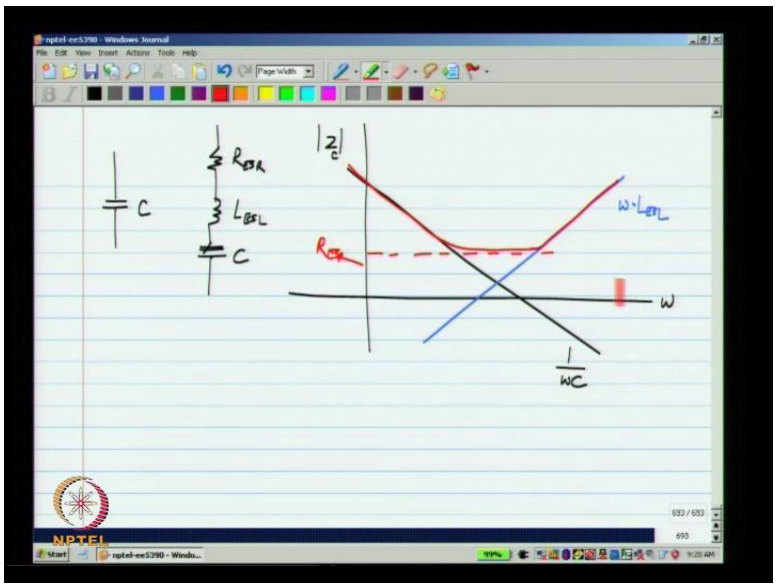

And if you plot the magnitude of impedance of the capacitor versus frequency ideally of course, it should drop-off a 20 degree per decade, and go on in indefinitely as you go highly very frequency you get very low impendence that is the purpose of using a capacitor, but in reality what happens is that you will have some effective serious resistance. So, it will limited to this value and you will also have effective serious inductance whose impedance actually increases with a frequency this corresponds to one over omega c and this corresponds to omega times LESL. So, overall impedance looks something like this or a you see a flat regions are not depends on related values of the effective serious inductance and effective series resistance, but this is where the capacitive this is, where its resistive this is, where its inductive.

So, although the large capacitor beyond a certain frequency the impedance does not reduce now, this introduces complications because here we have this RSR let us ignore the effective serious inductor for now, and considered the only series resistance in that case what happens is the again from this point to that point will get modified.

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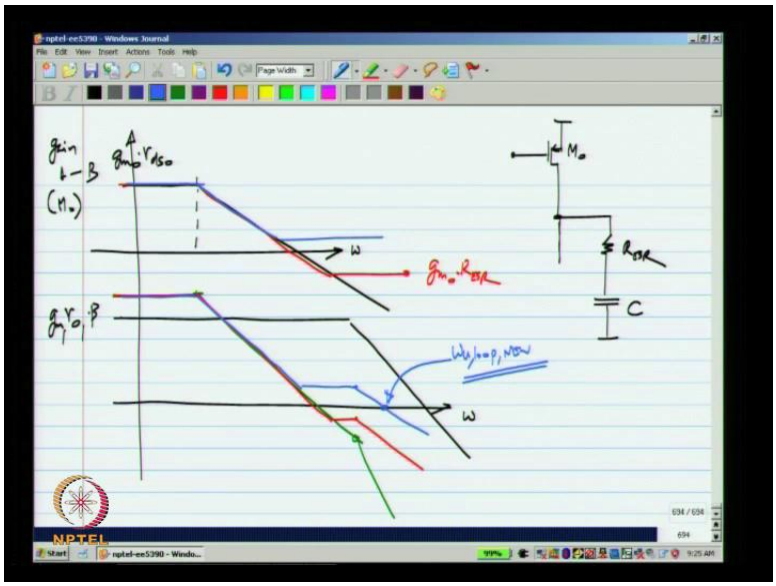

Let me redraw the gain from A to B through the transistor M0 we earlier saw that it has the dc gain of g m0 r d s0 and pole at one over r d s0, and c o and it has a first order pole of in presence of the effective series resistance, let us say this is M0 and we have RSR and I have ignored other load that appears here. Now, this M0 is loaded by the resistance and the series combination, and the series combination is equivalent to the capacitor at

low frequencies the capacitance reactance is much higher than the resistance value, but as you go to higher frequencies the capacitance reactor will becomes the smaller than the effective series resistance, and again it is dominated by the effective series resistance.

So, for certain USR it may look like this, where this value is given by essential even by g m0 times RSR now, the value of USR increases you could even have stuff like that, where g m0 times RSR becomes more than one that is also possible now what happens the gain of the other part, which is g m1 r o1 times beta well be half some shape like that. Now, the overall transfer function in absence of any effective serious resistance could be exactly as being had earlier. So, it could be like that let me show this poll at a higher frequency. So, in absence of any effective serious resistance the loop again magnitude response will look like that one.

Now, if you draw it corresponding to the red curve over here and at this point it becomes flat, and if you draw it corresponding to the blue curve. In fact, you see this with this model the gain is not going below zero degree. So, of course, this is clearly not acceptable let me show the poll as well. So, it looks like that and with a blue curve it will look like that one. Now, what is happened is although there is the dominant pool response over there, because of the effective serious resistance the unity loop gain frequency is pushed out to a higher frequency this is now the new unity loop gain frequency. Now, for small values of the effective serious resistance the unity loop gain frequency is the same as what we calculated without the effective serious resistance, but as the effective serious resistance is increases its possible that the zero will moven within the unity loop gain frequency, and the actually unity loop gain frequency will moved to a higher frequency.

Now, many things can be happened here first of all the other parabolic polls that we have ignored. So, far can be now became the new loop gain frequency and degrade the phase margin. So, this effective series resistance can cause problems for stability by increasing the gain at higher frequencies. So, this is a problem. So, it depending on the circuit structure you have you will have an upper limit on the effective series resistance for, which the circuit is stable.

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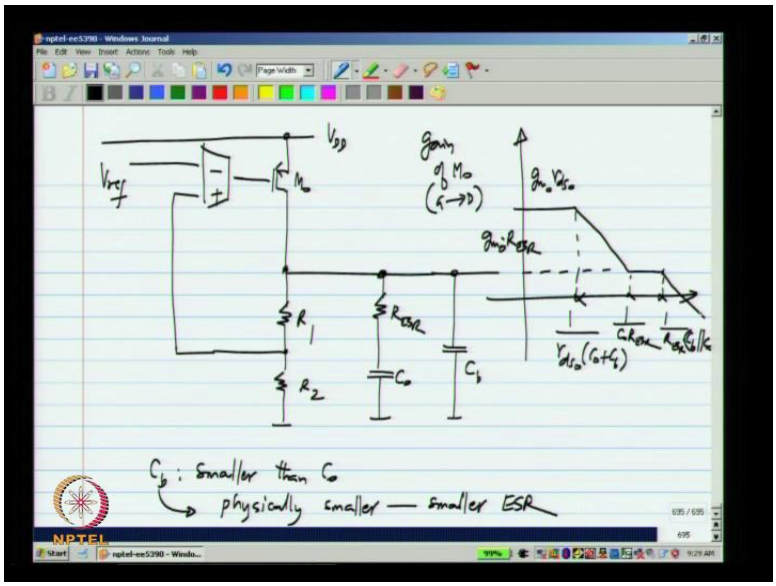

So, what is normally done is that we have the effective series resistance for this capacitor and to make sure that the effect of the effective series resistance is that high-frequency the impedance is does not reduce. So, what is V c done is to have another bypass capacitor, which is smaller much smaller than C0. So, C b physically smaller and has a smaller effective series resistance will assume that the effective series resistance of C b is negligible. So, this is what is usually done.

So, in this case what happens is at very low frequencies the d c gain is given by this g m0 times r d s0, that is he d c gain on due to this amplifierM0 and has you go to higher frequency there will be a poll due to this C0 plus C b r does not come in to picture, and then at some higher frequency there will a zero, because this RSR start dominating the reactance of C0. And finally, at even higher frequency the reactance of C b becomes smaller than the resistance of RSR, and the responses dominating by this capacitance.

So, again if I draw the magnitude response of the gain through the device M0 I will say gain of M0 what it means is from the get to drain of M0 will have the usual g m0 r d s0 and the first poll will be at one over r d s0 C0 plus C b, you can evaluate these things by yourself, and then it will start rolling of, and then again a constant and this constant value of gain is given by g m0 times r s r, and the value of zero will be at one over on C0 R USR, and it is some higher frequency this will start for enough at that frequency is basically one over RUSR times C b in series with C0. So, all these things you can

evaluate by yourself this is the gain profile of gain through m0 so then, if you look at the overall response and the gain of the amplifier let me show it like that that is gm1 r o1 one times beta.

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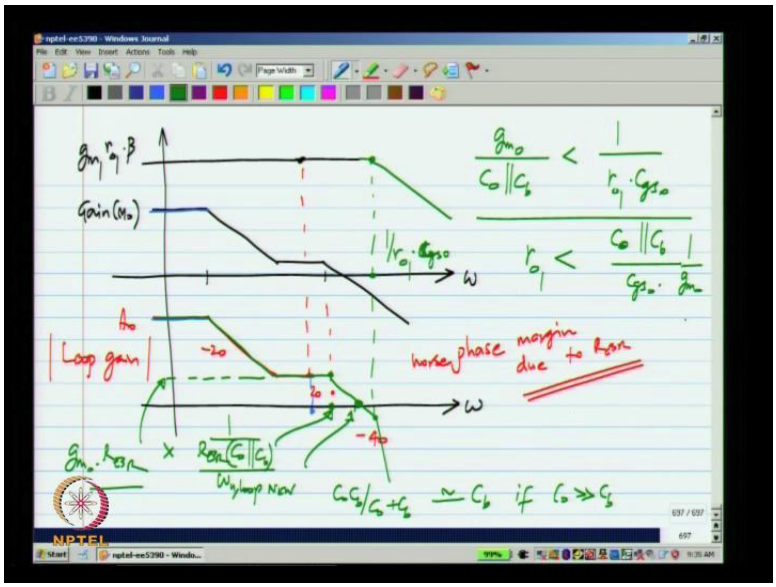

So, the overall response is given by the d c loop gain then it draws of like that then it can become a constant, but here we have another poll. So, it does that and here we have ((Refer Time: 22:20)) wave pool. So, it can do that one. So, clearly you can see that when they gain crosses unity the slope is minus 40 degree per decade; that means, that phase margin is degraded to a very poor values this is the magnitude response of the loop gain. So, what is happen is that.

Now, first of all let me instructive on the same plot draw what could happen, if there was no USR then we would simply have response there could be like that, and here this response would go that the way I drawn it the second poll is just at the unity loop gain frequency, but the first margin here will be lot better than a phase margin there. So, basically the effective serious resistance will degrade the stability of the circuit we will place a another capacitor across the main capacitor. So, that you can maintain a low output impedance at very high frequencies also, and because of that there is an even more severe constraint on the output resistance of the amplifier basically. Now, we see that the poll of the amplifier here must appear beyond on the unity loop gain frequency;

that means, this poll has to pushed out for further what we should have is a picture of this sort not like this, but something like sufficiently far away.

So, that instead of this curve we should get even with the high ESR, if you want to a circuit to be stable we should have the poll some over their this is the poll of the amplifier and this can see is one over r o1 times c g s0, and it as to be greater than this omega u loop new, and how much is that it is given by this gain, which is g m0 times RSR times this particular times this particular poll, which is given by one over RUSR C0 in series with C b this symbol means this value is C0 C b by C0 plus C b, and it approximately equal to C b, if C0 is much more than C b.

So, this unity loop gain frequency is new nothing, but the product of this quantity and that quantity, and that is equal to g m0 divided by C0 series with C b, and this has to be smaller than one over r o1 c g s1.

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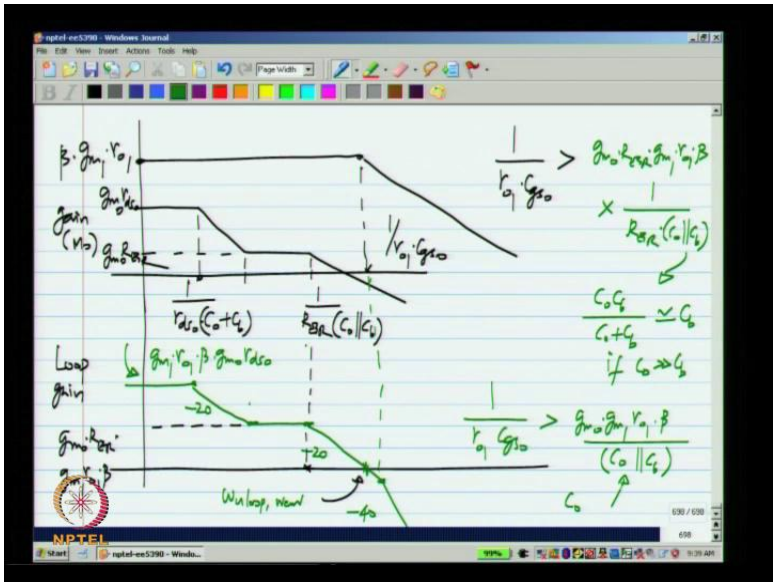

And this is more severe constraint than what we had previously say draw the magnitude response for the case, where it is going to be stable gain through M0 would again do this is g m0 r d s 0, and this value is g m0 times RESR, and this is one over r d s0 C0 plus C b other pole is one over RESR C0, and see with this C b and I will show the other amplifier as having a pole at a very high frequency. So, that it was guarantee to be stable this is the pole of the amplifier and this is one over r o1 c g s0 and the d c gain here is g

m1 times r o1. So, the combined response that is the loop gain magnitude response would be we are that is all.

So, it is minus 20 degree per decade there minus 40 and this is the new unity loop gain frequency this is minus 20, and this value is g m1 r o1 times beta g m0 r d s 0, and this value is g m0 RESR times g m1 r o1 times beta, and this pole is basically given by one over RESR C0 and series with C b. So, the pole at the out of the amplifier one over r o1 times c g s0 as to be greater than the new unity loop gain frequency I will call this omega u loop new, and that is given by the product of this gain and this pole value that is g m0 RESR g m1 r o1 times beta times one over RESR Co in series with C b this symbol means Co C b by C o plus c b and is the approximately equal to C b, if C o is much greater than C b. So, you have one over r o 1 c g, s0 that which has to be more than g m0 g m1 r o1 times beta divided by C o in series with C b, we can see that this is the much more severe constraints then before we had C over here.

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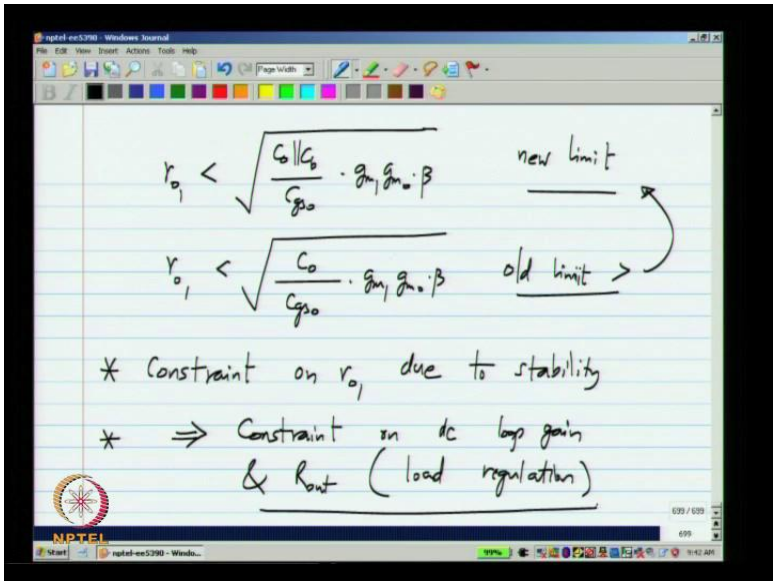

So, if I right it as a constraint on r o1 had to be smaller than square root of c g s0 by C0 in series with C b and g m1 g m0 times beta now, previously we had r o smaller than c g s0 divide by C0 and series with C b divided by c g s0 times that, where as a previously we had C0 by c g s0 times g m1 g m0 times beta now, C0 is much more than C b. So, the holder limit was greater than the new limit.

Basically the point here is that, because of the effective series resistance of the capacitor C0 at the output we are force to put a much smaller capacitor in shant with it at the output. So, the high frequency impedance again goes down with frequency, but the problem is that the pole now also most to higher frequency the unity gain frequency most of also higher frequency with the sufficiently high effective series resistance; that means, that the output resistance of the amplifier that is used for the feedback loop as to have a smaller output resistance this further limits the d c gain. So, this one of the chief constraints and designing the voltage regulator in an effective way we are only looked at the basic voltage regulator there are lot more elaborate topologies in which you will use more complicated amplifier's in feedback.

But the main constraint is that you are allow to use a very small quiescent current in the amplifier that kind of limits your options you cannot have very small output resistance at all frequencies you try to make a very low output resistance at d c by a realizing a very high d c loop gain, but the loop gain will be constraint by stability this implies that is the load regulation. So, all these things have to be taken into an account while designing the voltage regulator.

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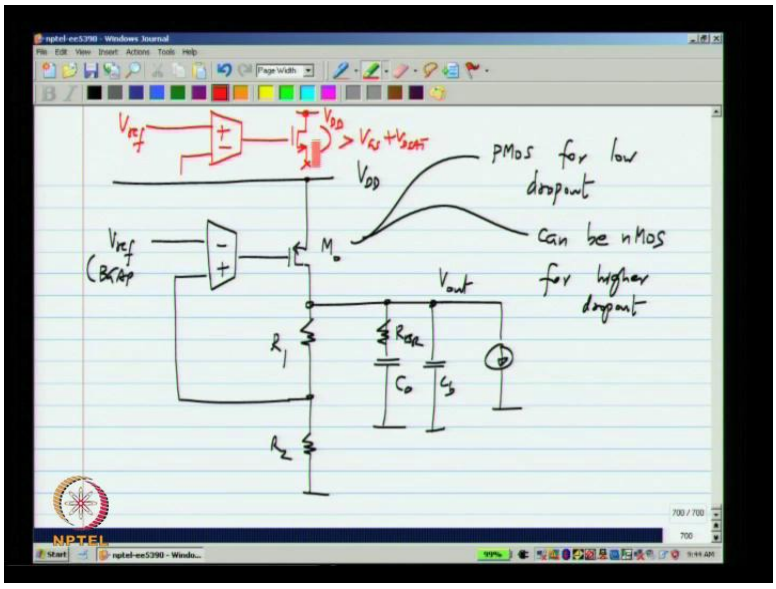

So, finally, we have the voltage regulator topology this comes from band gap there are a number of ways of realizing this amplifier we look at a very simple example and also this transistor M0 this as to be p-MOS for low drop out that is, if you want the drop out

to be of dropout 100 and 200 mile volts than this as to be p-MOS device, but if dropout is allowed to be higher because of whatever constraint you have large difference between VDD and V out for instance this can be an n-MOS also, if it as n-MOS then what we will have is instead of this will have it like it that the p-MOS part will be replace by whatever I have shown here, and because there is no inversion from the get to source of the n-MOS the sins of these amplifiers will be reverse now this voltage as to be one VGS below that, and this itself will be below VDD.

So, the dropout here will be greater than some VGS plus VD sat. So, we will need at least one volt or show between VDD and this one, but for dropout that are one volts are greater you can use the n-MOS pass transistor, and that can have some advantages because the output the d c output resistance can be lower because you're looking into the source of the transistor, which inherently as a low output resistance of the one over g m and that is further reduced by feedback now, will look at the just one example of realizing the feedback amplifier.

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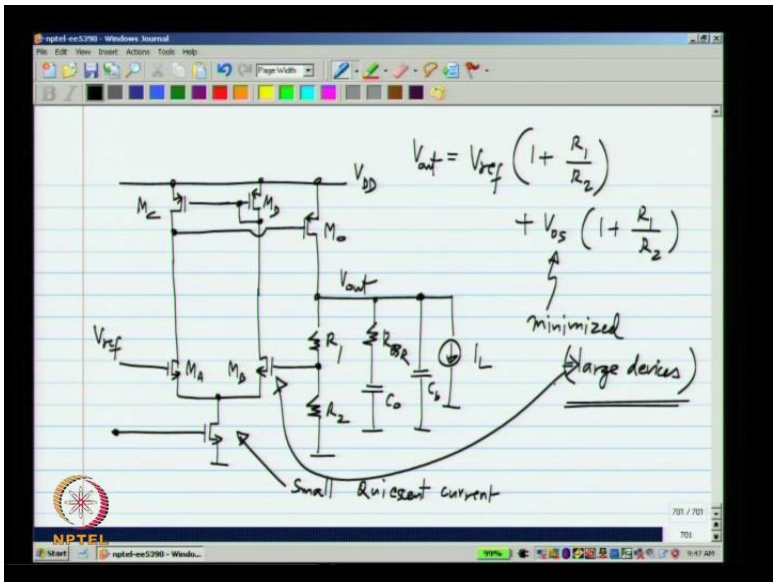

So, the simplest thing that we can do is the realize single stage op-amp this is biased with some current mirror and we apply V ref for their assuming that this is 1.2 volts there is enough rooms to accommodate this n-MOS differential pair otherwise you will have to use p-MOS, and then hold up the signals. So, this is the voltage regulator for efficiency you should use small quiescent current and also the output voltage here will be V ref

times one plus R1 by R2, but also it includes the offset of the amplifier that is used. So, it will be V os times also one plus R1 by R2, so for accuracy this as to be minimized. So, for this it means that you have to use large devices not only this, but also these all of them contribute to the offset. So, that is the standard way of reducing the input referred offset of any amplifier and that as to be done as well one of the important criteria of a voltage regulator is its accuracy, and in order to maintain accuracy you have to use large devices they are lot more refinements to this voltage regulator, which we can see in the literature in the direction of increasing the power of a rejection ratio, and improving the loop gain and. so on and so forth.

So, that is brings us to the end of references and voltage regulators the next topic that will deal with is filters that is another class of analog circuits that is use for selecting certain frequencies and rejecting other frequencies there are essentially two kinds of analog filters that are frequently realized one is continuous time filters, which basically operate on continuous time signals and other is switch capacitor filters or discrete time filters. Now, again as with the recent blocks that we discussed we will not going to great detail about the operation and design of filters will just outline how to design them, and point out some major issues.

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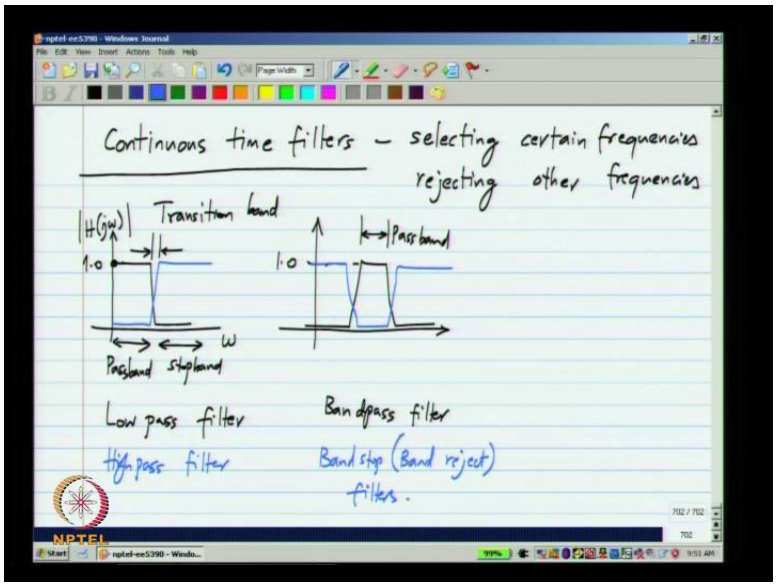

These are basically use for selecting certain frequencies that is selecting signals of certain frequencies and rejecting other frequencies, and broadly there are four classes

based on which one you select, and which one you reject the transfer function magnitude is what I am drawing here verses omega in this case it allows low frequency signals, and reject high frequency signals I will show this as one, and whatever is allowed is called the pass band, and whatever is removed is called the stop band, and whatever is in the middle, where it has to change from allowing something that is the high magnitude response to a rejecting something, which is a low magnitude response this is called the transition band, and this type of filter which as a high magnitude at low frequencies that is allows low frequencies signals is known as low pass filter, and there is type that rejects both low and high frequency signals, and allows some intermediate frequency signals this is the pass band and this known as a band pass filter.

And there are filters there are complimentary that is something at reject a low-frequencies, and allows the high frequencies and such a thing is known as high pass filter and there are also filters that reject certain band, but allow higher and lower frequencies, and those are known as band stop or band reject filters.

So, essentially these are linear time in variant systems, that is some linear circuits, which are frequency dependent they have capacitors and possibly inductors in them, and they have a certain transfer function that is certain transfer function between the input and output, which behaves like this now, there are number of steps involved in the design of a filter. So, first of all you will have a specification of which frequencies to accept frequencies to reject and by how much that is the amount of attenuation, and stop band based on these things you select a certain type of filter.

There are many different types of filters, and depending on a the steepness of the transition band that is how quickly you want to go from allowing the signals to rejecting the signals that is over what frequency range should you have the transition you will decide the type of the filter, and the order of the filter, and from there you go to some proto-type realization.

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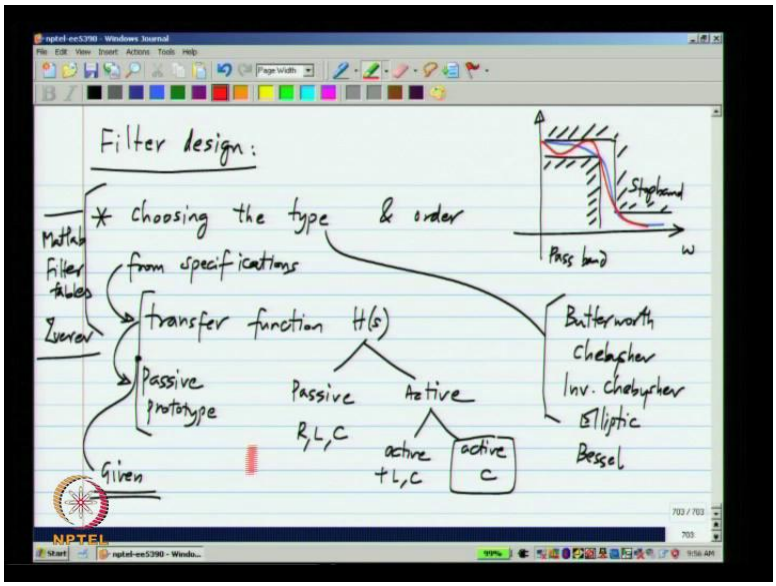

And finally, realize the filter and active form. Will only with dealing with the certain part of this whole processfilter designs involves, which is basically usually decided by a normal specifications looks like this, if you see books you will be given something of this sort that is this will be the pass band and this will be the stop band, and you will be given some region, where you can have your response, your response can look like that or your response could look like that and so on. So, exactly which one it follows depends on type of the filter basically one of the crucial things is the range of frequencies over, which it has to change from a low attenuation that is passing the signal through high attenuation that is rejecting the signal. So, based on this you choose the type and order essentially you choose the transfer function of the filter.

This transfer function H of s can be realized in many forms passive or active and in passive case in general you will need R L and C in active filters you could use a active elements plus L and C or only active elements and C. So, we will look at only this particular type of filters, which is realized using active elements that is transistors and capacitors, and also where entirely skip the discussion of how to derive the type of filter, and order of filter from the specifications and so on, we assume that the transfer function of filter as known to us and there is something known as the proto-type realization that is also known to us, from this there is something known as passive prototype a large class of active filters as synthesized starting from the passive prototypes.

So, we will assume that these things are given and work from these to get our filter topology now just as a quick mention of this that type of filter could include butter worth chebysher, inverse chebysher, elliptic and bessel and so on, and there could be other types as well the process of doing these things, which we are not treating can be done with mat lab or with some filter tables there is an extensive book of tables published by an author named were. So, one of these things we assume is the source of the transfer function H of s and passive proto-type, and from these will go on to synthesize or filters I will first quickly take an example of filter, which is a low order that is second-order, and then go from there to see how we can generalized to higher-order filters.

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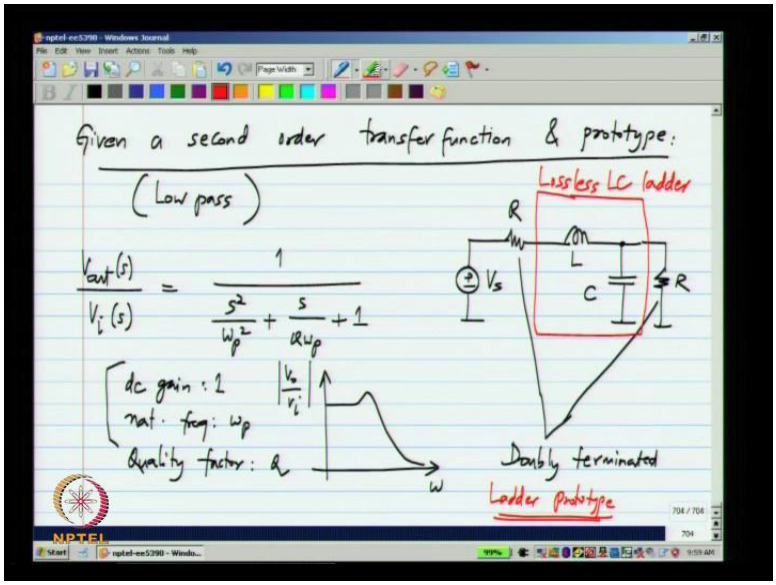

I will also assume that the filter we are interested in is the low pass filter it turns out that the most often low pass and band pass are used these are the two filters that is we will discuss in this course. So, what is that mean to have a second-order transfer function and prototype the transfer function of second-order low pass filter is given by one by s square by omega p square plus s by q omega p plus one for this as a d c gain of one, and a natural frequency of omega p and a quality factor of q, and this is what we have to realize, and in general if you plot the magnitude of V0 by Vi versus omega you will see something of that is all.

Now, typically you will also know the passive prototype, which can realize this and it can be in the form of this R L C circuit this is a very common form of the prototype were

you have these two termination resistances, which is why it is called w terminated, and you have lost less LC ladder between the terminations, which is why this is known as the ladder prototype. So, what will do is we take this ladder prototype and try to synthesize it in active form when we say try to synthesizes what we mean is there are certain relationships between voltages and currents in this ladder filter will try to do it with active elements and capacitors, and then later we will generalized it to higher-order filters it turns out that any higher-order filter can be decomposed into a cascade of second-order filters that is, if you have high-order polynomial you can factor turned into second-order polynomials or if the polynomial is of an odd order number of second-order polynomials, and a first-order polynomial.

Now, that it turns out gives us two ways of realizing higher-order filters you can first factor out the higher-order filter into a number of lower-order filters number of second-order filters and possibly a first-order filter you can realize each of those second-order filters, and first-order filters and put them one after another that is one way, and another way is you start with the higher order ladder that is ladder, which as lot more L's and C's than just a two I will shown here and synthesized that directly.

So, based on these will show you how to synthesize higher-order filters and point out some important steps in the process of designing filters now there is an extensive literature, and filter design both active and passive. So, refer to those things for detail what we do in this course are meant to be just guidelines of the important steps involved in active filter design.

Thank you, I will see in the next lecture.