**Analog Integrated Circuit Design**
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Lecture - 55
Fractional Bandgap Reference;
Low Dropout Regulators

Hello and welcome to lecture 55 of analog integrated circuit design in the previous lecture. We discuss the bandgap reference in great detail. It provides very stable voltage reference that is independent of process variations and temperature it gives you zero temperature coefficients at a particular temperature. So, that the voltage variation over the temperature range, where interested in that is about 0 to 100 degree c is small enough. In this lecture, we will look at a slight modification of the bandgap reference that enables us to design, it for low supply voltages and then go on to voltage regulators, which are another crucial part of biasing circuit. They provide supplies for other circuits bandgap reference that we had goes like this.

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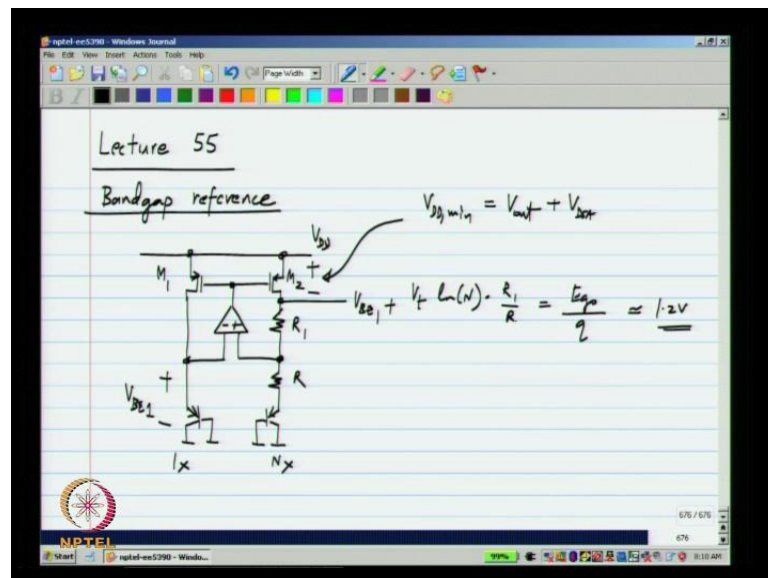
Perhaps I will show it with transistors p m p transistors, which is the common thing to use in a cmos process, and this is the output. If everything has been designed correctly this output, which is V BE 1 plus V t log N times R 1 by R, if this is this as an area of 1 this is an area of n equals E g naught by q, and this is independent of temperature and we

know that this is 1.2 volts. So, the minimum supply voltage with, which circuit can operate is the voltage that appears here, which is 1.2 volts plus the voltage required across m 2 to keep it in saturation reason and typically, we need a 200 mile volts across a transistor. So, the lowest supply voltage is about 1.4 volts.

Now, this is all right if you have a supplies higher than this. Let's say 1.5 volts are higher, but these days you have to operate many circuits for the for lower supply voltage, such as 1 volt or 1.2 volts. So, the circuit cannot really be made, but we can slightly modify this circuit, so that we can get a temperature independent reference with the smaller supply voltage. Of course we cannot get a 1.2 volt output voltage from the smaller supply voltage, but instead of 1.2 volts we get a fraction of it, which is also temperature independence it will be just fine.

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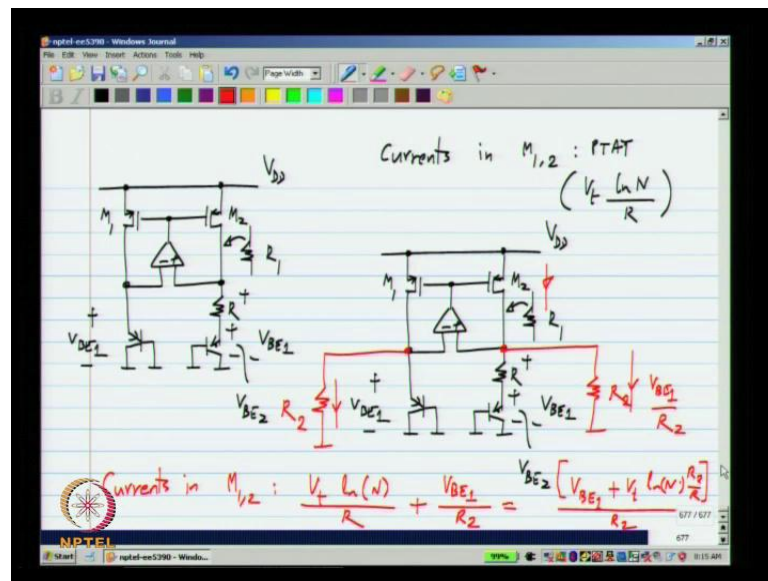
Now, if you go back to the evolution of the bandgap what we did was? We had the pit hat cell in this V B 1 is available in these 2 places and this is V B 2 and to add pit hat voltage to this. We recognize that the currents in these 2 branches are proportional to absolute temperature and add a resistance in series. So, this is R and that is R1. So, if you place this resistance in this branch. We get V B 1 plus pit hat voltage and the final output is the bandgap voltage. So, now, all we have to do is to add V BE to this pit hat voltage now, this can be equally well done in the current domain.

First now, we recognize that in this particular circuit currents in m 12 are proportional to absolute temperature there are equal to V t log N divided by R. So, instead of adding voltages that is instead of adding V BE to a voltage that is proportional to absolute temperature. We can take the current that is proportional to absolute temperature and add a current, which is proportional to V BE 1. So, we know that the voltage here and there are both VB 1. So, if we add a the same resistor R to the 2 sides of the circuit what happens is the currents in this will be V BE 1 by R both of them the current in m 1 and m 2 will still be equal to each other, but they will consist of the proportional to absolute temperature, which are flowing in this bipolar transistors plus this current, which is proportional to V BE 1 flowing in the resistors.

So, in this particular circuit currents in m 12 or the sum of pit hat current and oh. Let, me use a different symbol for this R 2 pit hat current and a current that is proportional to V BE 1 and we can write this as V BE 1 plus V t log N times R 2 by R divided by R 2. You see that the numerator of the same form as before it is a voltage, which is the sum of a bay symmetry voltage drop and a proportional to absolute temperature voltage drop by adjusting their ratio R 2 by R. We can make this temperature independent that is make it equal to the extrapolated bandgap voltage E g naught by q. So, the current in this will be then independent of temperature, and we can replicate this current and pass it through a resistor to get a voltage that is independent of temperature.

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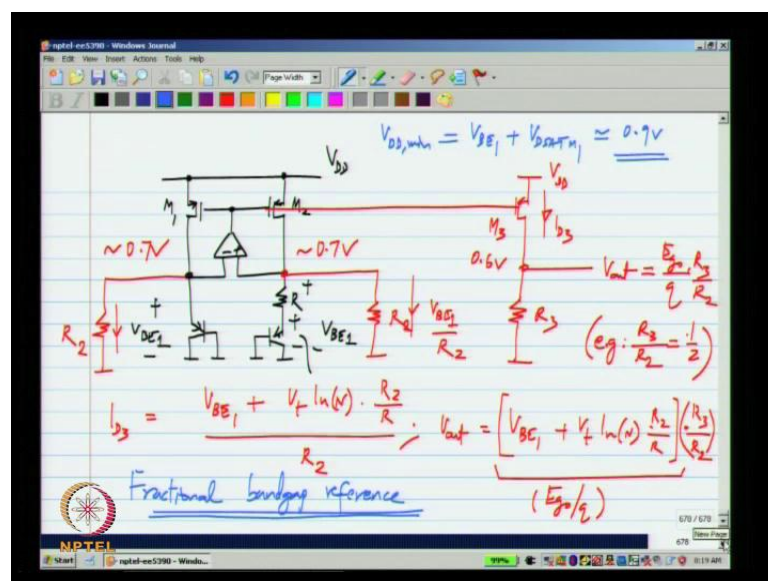
So, what we then do is have a resistance R3 over here in the current in this, if a call this m 3 ID 3 is V BE1 plus V t log N R2 by R divided by R2 and therefore, the output voltage is this times R3. So, if this R2 by RS adjusted correctly that term in brockets will be the extra polite band gap E g not by q and if is said this R3/ R2 ratio to be smaller than 1, what we get here will be a fraction of the bandgap voltage for instance. We can set R3 by R2 to be let us say half then the voltage that we get here is 0.6. Now, everywhere in the circuit here we have V BE, which is about 0.7 volt here also. It is the same it is about 0.7 volts and here it is 0.6 volt. So, the minimum voltage that is required, which was the main point of a modifying the circuit is V BE1 plus VD sat m 1, which is approximately 0.7 plus 0.7 volts, which is 0.9 volts where as earlier we need at 1.4 volts minimum supply to build up bandgap circuit.

Now, we need only 0.9 volts this circuits, which was basically an adaptation of the original bandgap circuit. In order to operate with a low voltage is called a fractional bandgap circuit. The principle is very simple, instead of adding the bay symmetric voltage and the proportional to absolute temperature voltage in the voltage domain. You add them in the current domain and this circuit is called a fractional bandgap reference. Now, this circuit is also self biased like our circuits, which generated currents for constant g m and so on.

So, this will also need a start of circuit in the principal is exactly the same you can look at the known at, which the voltage should be V B1, if it happens to be 0 you can pulls some extra current from the some points in the circuit, which will enables the circuital start up and as usual you should make the start up circuit week enough of. So, that once the circuit is start up the start up circuit drops over the picture. Now, trouble of more points about bandgap, whether we take the fractional bandgap are the regular 1. Let me take this 1 for now, as with the propositional to absolute temperature sell m 1 and m 2 have different values of V DS the drain.

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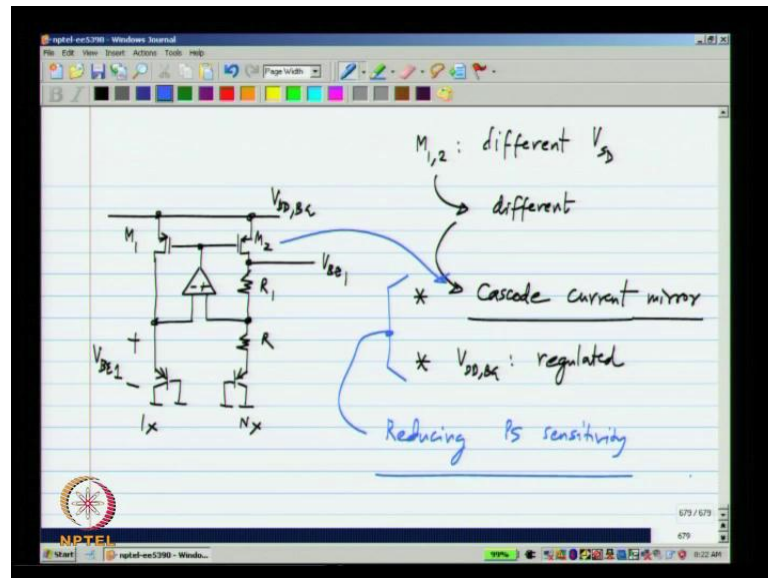
Source voltage these means that the currents in m 1 m 2 will be different now this will cause some errors in the bandgap voltage as well as it will make the circuits sensitive to v d d because as v d d increases the v d s of m 1 and m 2 will change in different ways. So, as usual the way to combat this is to use cascade current mirror that is you make an m 1 and m 2 instead of simple transistor cascode that is 1 possibility another possibility is that the supply voltage here is regulated, that is you make sure that this voltage does not very too much now this does not have to be tightly regulated, because this already rejects the effects of power supply to some extent, because from the ideal analysis the output voltage is independent to everything is when you put the channel and pond relation effects in the current mirror m 1, and m 2 that you see some effects.

So it already rejects the effects of supply variation to some extent. So, even if that v d d b g which is the supply for this cell if crudely regulated that should be good enough. So, both techniques are used sometimes you use cascode sometimes you use regulation. And of course, you can use a combination, if you wish of this could be made cascade. So, these are the 2 ways of reducing power supply sensitivity.

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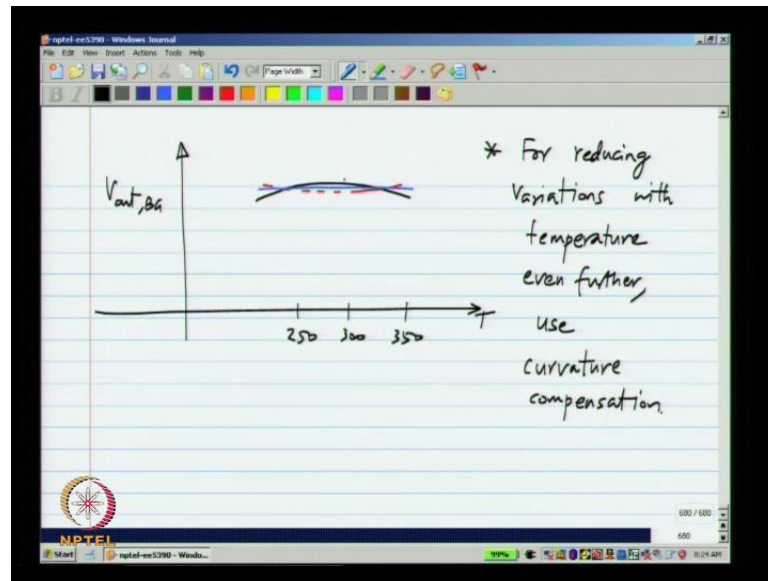
And finally, if you make the bandgap reference and measure its output voltage versus temperature you will see something like this. So, maybe this would be in the desired range of temperature. So, somewhere it will have zero temperature coefficient and it will have a curvature of this 1, now just like we added the positive and the negative temperature coefficients proportional to absolute temperature voltage.

And the bay symmetry voltage they can also get we can also try, and correct the curvature of this temperature dependence for that you will generate ah currents which have the opposite kind of temperature dependence by using appropriate combination of pit hat currents and constant currents and perhaps temperature coefficients of resistors and if you add to this a small a voltage which as opposite temperature coefficient, then the resulting voltage would be more constant a it will have some curvature which can be further corrected and so on. So, for reducing variations with temperature even further 1 would use a, what is known as curvature compensation if you go through the literature you will see a number of papers entitled curvature corrected bandgap circuits and so on.

So, if you see sometimes they have curvature correction first-order or even second order to get the output voltage to be as precise as possible over temperature. So, that concludes our discussion on bandgap reference, there are extremely widely used.

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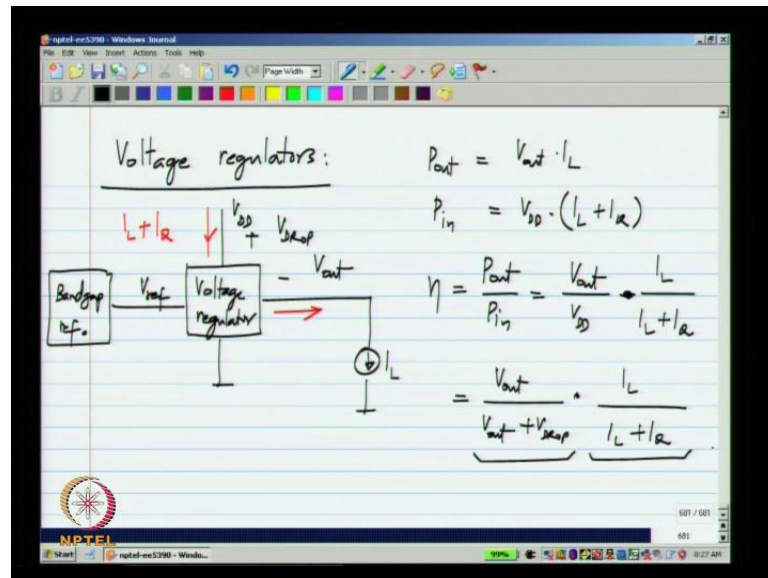
And they provide references for voltage regulators which is what we are going to discuss next, now what is a voltage regulator it has some supply and its require to supply constant voltage v out in spite of variations in v d d, this you would have see in very often if you have build some short of circuit. Then you would get the d c source from somewhere, but you will further regulated using voltage regulator first of all to get the voltage to the level that you want and also minimize any variation in the voltage that.

You are supplying to your circuit now this will lead a reference because this by the itself will not be able to hold the voltage accurately. So, it will usually use the bandgap reference which we have already discussed and it will be connected to a load which I will model using the current source i l, now a current flowing through the supply now you will actually be a current flowing out with which is i l plus some current that is consumed in this circuit I will call it i q the kaizen current in the voltage regulator and also the output voltage is v out.

So, the power that is driven out power that is delivered to the load is v out times the load current and the power that is drawn from the supply voltage v d d is v d d times i l plus q. So, the power efficiency theta p art by p in equals v art by v v d times i l by i l plus i q, which can be further written as this difference between v art and v v d, that is considered the drop across the regulator that is from the input to output of the regulator, I will call it v drop and that is now clearly to maximize the efficiency of the circuit to minimize the

value of v drop and minimize the value of i q that is you minimize the drop across the voltage regulator as well as you minimize the kaizen current drawn from the regulator circuit now sometimes. Of course, the input voltage v d d and output voltage of the regulator r specified in this case you have no choice, but to take whatever v drop you have and the efficiency will be in the best case we have divided by v d d, but in those cases where you have the choice of the input voltage or the output voltage you minimize the drop.

So, that you get the maximum efficiency that responsible this is pretty obvious now the voltage regulator it is suppose provide a constant voltage output with a very low output resistance essentially it is a voltage control voltage source its input is the reference voltage and the output is the output voltage which appears at the port which has a very low output resistance. So, now, we have already made many amplifiers which has low output resistance in feedback feedback is 1 of the ways shunt feedback is the way to get low output resistance, now there are certain characteristics of the voltage regulator that make it different from a regular amplifier.

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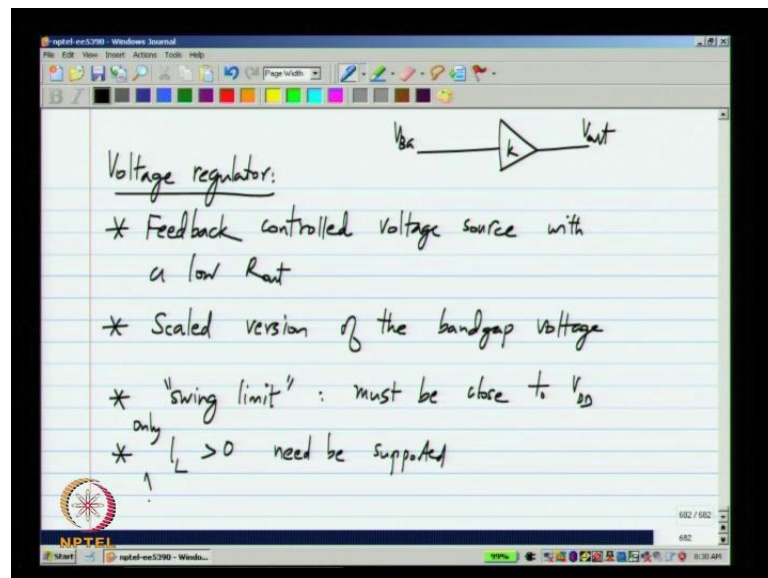
Basically feedback controlled voltage source with a low output resistance and it basically will be some scaled version of the bandgap voltage. Essentially it is like taking the bandgap voltage and putting it through some amplifier k in getting the output voltage, but there are some particular characteristics of the voltage regulator a 1 of the things is

that the low dropout means the swing limit of the amplifier the upper swing limit must be close to supply voltage v d d and also normally you are required to support a load current which is more than zero that is normally this is powering some circuit that is drawing a power drawing current. So, you are only required to be able to support a current in this direction you do not need to make this regulator work for negative current unless you're talking about some special circumstances, and there are some other desirable features of a voltage regulator we have already talked about a load dropout if possible now this is for a few different reason.

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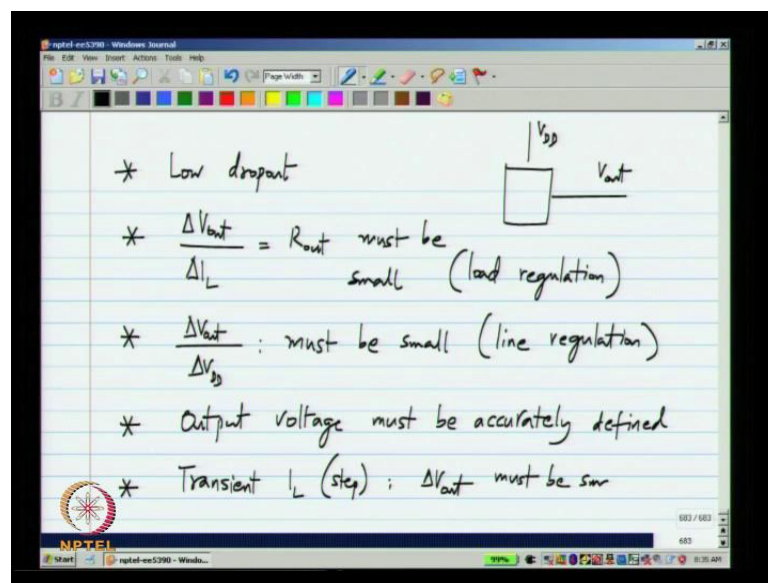
Let us say your output voltage is fixed that is you would like to have an output voltage of three point three volts now you would like to operate it from any voltage that is higher than three point three volts we cannot really operated from a lower voltage on a three-point three volts, but you would you need a higher voltage, but you would like that difference to be as small as possible right. So, maybe your operating it from a battery and you would like the regulator to work even when the battery has drained out quite a lot. So, that it voltages reduces.

So, that is 1 of the reason why you need a low dropout beside efficiency, you would like the regulator to be supplied with the voltage that is as widely variable as possible or put another way if a v d d is given value then sometimes, you make a variable voltage regulator that this v out a variable by some parameter of the circuit and you would like to

v out to have as much a range as possible; that means, that v out should be able to go as close to v d d as possible ok.

Now, the output voltage really should be absolutely constant, but in reality it would not it will first of all change with the load current in the fractional change of v out with a load current, which is basically the small signal output resistance of the regulator must be small. And this parameters is called load regulation we are required to proved a regulated voltage and load regulation a talks about how well regulated, is it is in the presence of variations in the load and delta v out by delta v d d this is known as line regulation that is if v d d changes the v out should not change, it should be whatever value we wanted it to be that is 1 of the purposes of using the voltage regulator.

So, you can take a voltage which is not well regulated, but provide a constant output voltage this must be small and this is refer to as line regulation how well the output voltage regulated against variation in the line voltage and the output voltage must be accurately defined that is another requirement. And finally, sometimes there is a step changes in the output current that is the output current changes and the transient of v out should be small as well here this parameters delta v out by delta l talks about the steady state, that is let say you would change the i l very slowly much does v out change that is what the dc output resistance represents. Now sometimes the load current can jump this can happen when you switch in a load or switch out a load, and then at that point the output voltage should not fluctuate considerably.
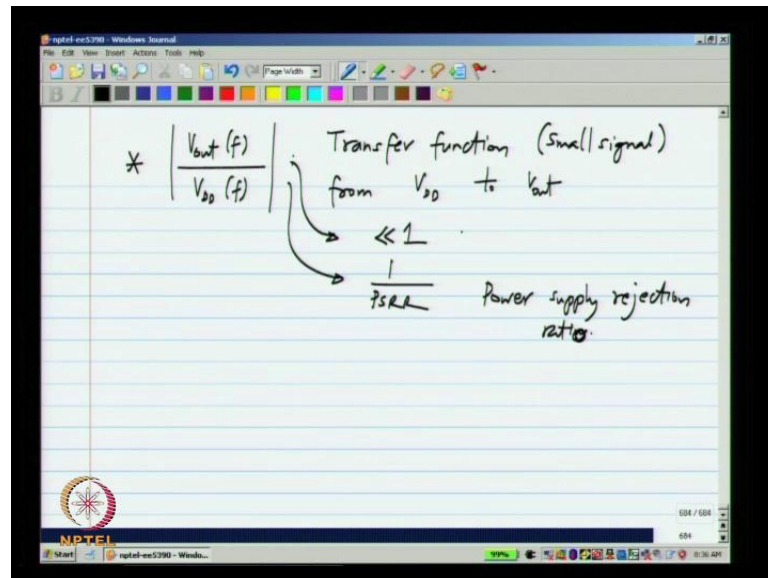
So, in addition to this you also have this parameters v out of f by v d d of f this is this refers to basically transfer function of course, for the small signal from v d d to v out naturally this number must be much smaller than 1, and the inverse of this this basically this is refer to as 1 over v s r r where p s r r refers to the power supply by rejection ratio. So, all here we talked about line regulation delta v out by delta v d d and that again is the static parameter that is for dc the same thing is measured for higher frequencies and that is called power supply rejection, and this is also important even if you have i frequency variations on v d d you would like to minimize them on the output line v out and this can happen, because of the variety of reasons first of all you have a number of circuits power from the main supply.

So, the main supply will have some variations, which are related to currents drawn from that supply now if you have a very sensitive especially some sensitive analog circuits like the oscillators you would like to regulate its supply voltage. So, oscillators supply should not have any variations ideally. So, you use a voltage regulator and this parameter power supply rejection ratio characterizes much variations, you have in the output of the regulator for a given variation at the input at different frequencies the parameters of interested different frequencies, because circuit such as ring oscillators are sensitive to noise at some frequencies that is some frequency noise matters more than the others. So, you would like to measure this power supply rejection at a wide varieties of frequencies.

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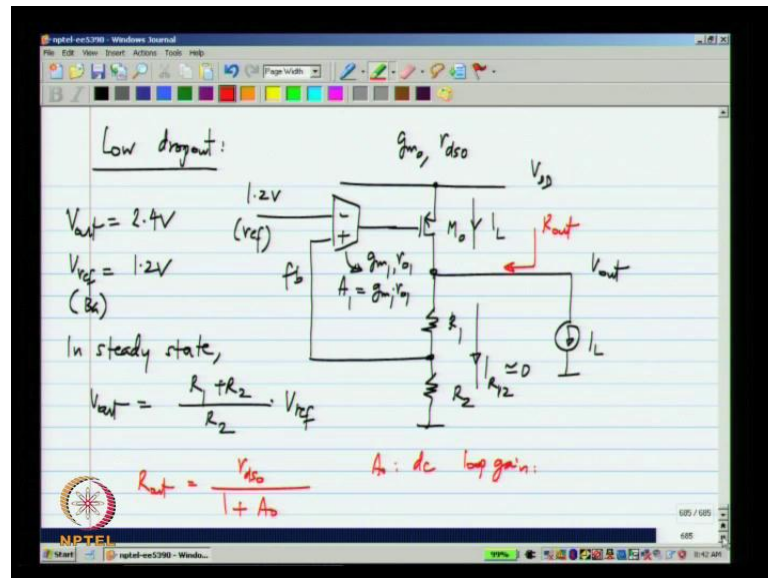
So, first of all if you need a load dropout, that is we have our supply line and we have the output line and v out should be able to reach as close to v d d as possible the best thing, we can do is to have a single p mos transistors between v out and v d d let me call this m zero. Now this p mos transistors as to be driven in some way that the output will be maintained at the desired voltage. So let us say v out happens to be it is 2.4 volts and the reference is 1 point 2 volts from a bandgap.

So, you have to multiply this by 2 and provide the output and the load current is drawn from the output voltage. So, what you do you want to generate 2 point four volts from 1 point 2 volts. So, you can divide the output voltage and compared it to the reference voltage 1 point 2 volts integrate the difference and drive the gate of the p mos transistor m naught, and you go on changing the gate of the p mos transistor until v out becomes exactly equal to 2.4 volts or basically this feedback voltage becomes equal to 1 point 2 volts.

So, now the integration is implicit somewhere basically the gate source capacitance where not will integrate the current that is coming out this trans conductor and if you look at the sense of feedback you should have this to be plus and that to be minus. So, this is the basic voltage regulator in steady-state v out will be r 1 plus r 2 divided by r 2 times zero. So, this is fine and also if you evaluate the small signal output resistance let us say that your operating with a certain load current in, let us assume that r 1 and r 2 are

very large what matters is the ratio of r 1 by r 2 to define the output voltage. So, let us say that the current flowing through r 1 and r 2 is negligible this is just for a simplicity. So, the transistor m naught will be operating with kaizen current which is equal to the load current and that operating point it has a certain trans conductance g m naught in a certain output resistance r d s naught. So, what is the dc output resistance looking back into the circuit I would not show it, but you can very easily analyze this circuit and see that it will be r d s o divided by 1 plus a naught were a naught if the dc loop gain in this corresponds to let us say the dc gain of this amplifier is a 1.

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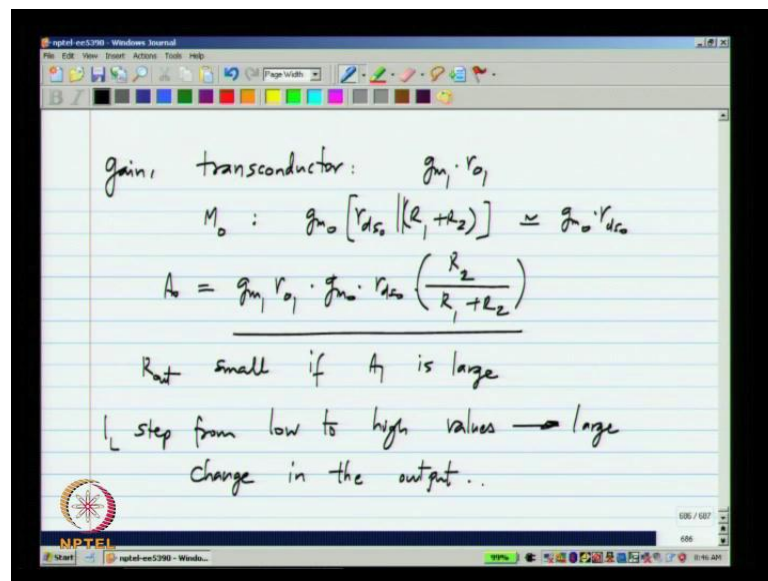
Let us say this as a trans-conductance of g m 1 and an output resistance of r o 1. So, this a 1 will be g m 1 times r o 1 and we have assumed r 1 and r 2 to be very large. So, the loop gain is the gain of this trans-conductor times the gain from this point to that point and the gain from here to there is simply gm zero times r d s zero, the trans-conductor as a gain of gm 1 r o 1 and the transistor m zero as a gain which is gm zero times r d o zero parallel r 1 plus r 2 and I have assumed that r 1 plus r 2 is much larger than r d o zero that will be g m zero times r d s zero.

Now, we are usually justified in ah neglecting r 1 plus r 2 in comparison to r d o zero that is because the regulator when it is designed for very high currents will have a very large mosfet m naught and very large current will be flowing through it now if this is not the case you can go back and put r 1 plus r 2 in all the calculations in the qualitatively there

will be similar. So, the loop gain a naught is nothing but g m 1 r o 1 gm zero r d o zero times r 1 by r 2 by r 1 plus r 2 and if this number is made very large the output resistance will be small. So, it appears that this circuit will do the job by itself, but it is not enough, this is because 1 of the conditions was that if i l changes like a step especially if it goes from a value to a high-value when a i l is at a very low value the most transistor m naught will be operating with a small current.

So; that means, that it will have a high-value of r d o zero and a low value of g m zero now when a i l steps out to a high current what happens? Is it take some time for the gate voltage of the mosfet m naught to change, that is because the gate of the mosfet m naught as a large capacitance and it has to be charged from this trans conductance gm 1 to be able to change it we also have this additional condition that the kaizen current dissipated in the circuit should be small, so that means, that the kaizen current used for this trans-conductor g m 1 must be small.

So, we cannot have a very fast response for this amplifier. So, it means that the moment that i l is stepped out to a high-value the output resistance does not change immediately that is the feedback that does not respond, and if you look at the output voltage it will step down by a large value basically what I am pointing out here is that r out is made small using negative feedback. So, if r out is very small you would expect that if a i l steps up by a large value then the output voltage will be a small step it'll be equal to delta l times r out, but because r out is made small using negative feedback, and it takes sometimes for the negative feedback to respond the moment i l changes the output voltage will step by a large value and it will slowly settle down to the small value given by delta l times r out.

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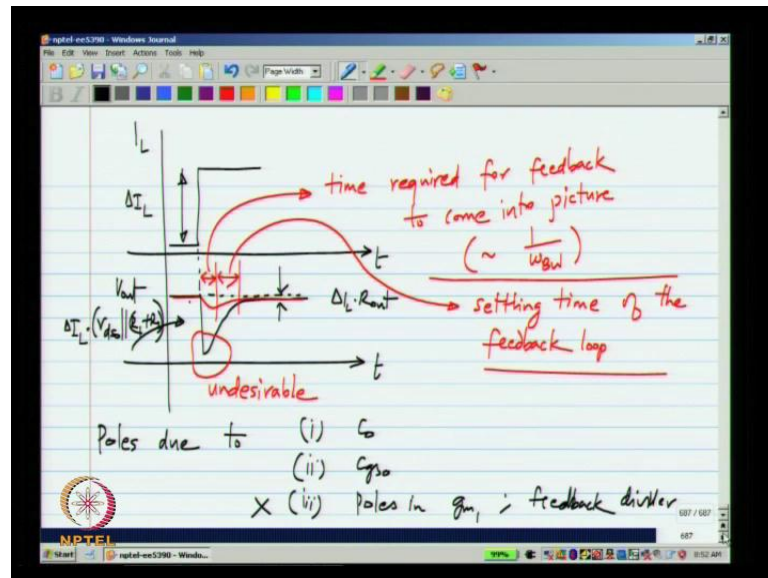
This is what you would see that is a i l steps up from a small to large value and output voltage let us say supposed to be here and just after the step essentially, it is still saying the old value of r out. So, to speak and r 1 plus r 2 also it will step down by large value which if this is delta l this would be delta l times r d o zero. Parallel r 1 plus r 2 and then the feedback kit son in, it will take some time they'll be slowing and settling of the feedback and finally, it will settle down to the right value and after it settles down the difference between the original and this 1 will be equal to delta l times r out which is rather small, but the transient voltage dip will be very large and this is clearly undesirable.

So, what is normally done is to have a large capacitor here. So, what happens is in steady-state this output capacitors c naught will be charged to the output voltage and if you have a current step the charge will be drawn from the capacitor the current will be drawn from the capacitor and the output voltage does not change all that much how much it changes depends on the size of the capacitor for by using a very large capacitor you can reduce the change. So, instead of having this large dip what will happen is that the output voltage will start to reduce as a ramp and it will go on reducing until the feedback effects kit son and it'll do that. So, roughly speaking this is the time required for feedback to come into picture and this is related to the inverse of the bandwidth of the amplifier.

And after that it take some time to settle and that is related to the settling time of the feedback loop. So, it is very common to use and output capacitor which is very large along with the voltage regulator otherwise the regulator will not be able to perform well when there are transient in the load current. Now it turns out that introducing this capacitor introduces complications in the negative feedback system because as usual the negative feedback amplifier has to satisfy its stability criteria, now this large capacitor introduces some pole and possibly a zero, as we will see later and we have to take into account this things while designing the overall amplifier its bandwidth and so on.

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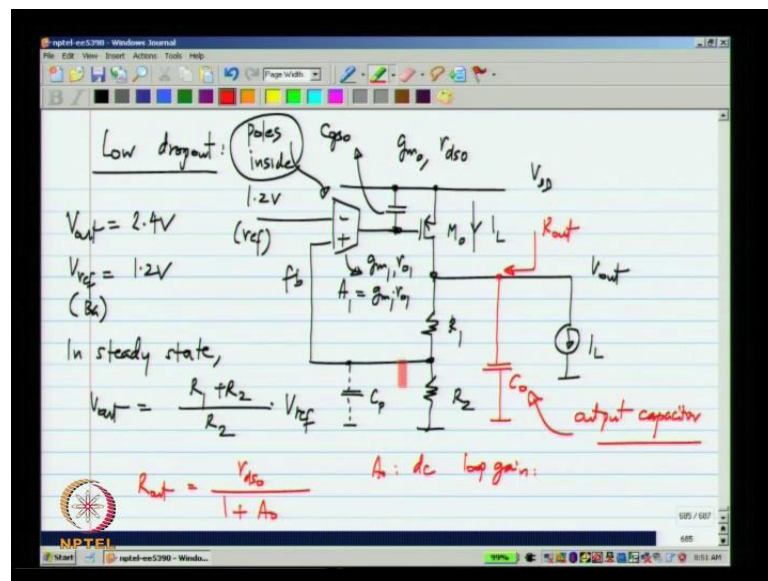
So, now, we have to worry about stability of this negative feedback system first of all there is 1 large capacitor that is definitely going to be present and that is the c g s of m zero and any parasitic capacitance at this node I have also absorbed into the c g s of m zero. So, this will definitely be there. So, at least you will have 2 poles, but in general you may also have poles inside the trans-conductor, and you will have some parasitic capacitance here which along with r 1 and r 2 will make the loop gain have another pole, but the dominant once will be at the gate of the transistor m naught and due to the output capacitor c zero the feedback resistive divider and so on. So, even ignoring this we have at least 2 poles and we can analyze the response of this 1.
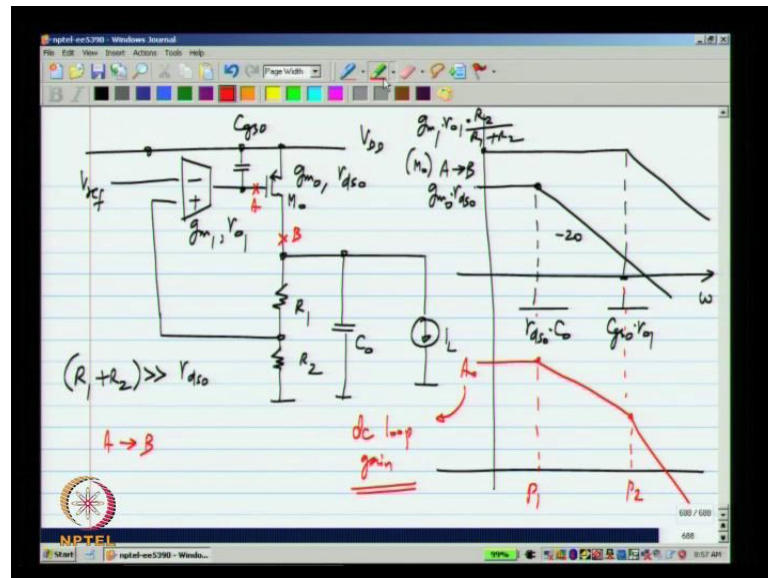
So, ignoring everything else will have will consider only these 2 in reality you also have to consider all the other poles which you do by simulation usually. And let us say this as trans conductance of g m 1, and output resistance r o 1 and this is as a trans conductance of gm zero and then output resistance of r d s zero. And will continue to make the assumption that r 1 plus r 2 is much more than r d s zero a value of r d s zero depends on the load current just for simplicity I have assumed that for all values of load current r 1 plus r 2 is much more than is much more than r d o zero, this is just to simplify the expressions, but instead of r d o zero you can always put r 1 plus r 2 parallel r d o zero. And you will get the more accurate result in case r 1 plus r 2 cannot be neglected like this. Now what will be the loop gain function of this system if you look at the function from a to b the transfer function from a 2 b will have gm zero times the impedance here which is r d o zero parallel that 1, and because c zero is very large the pole associated with this node is likely to get a low frequency.

And that will be tend to be the dominant pole of the system. So, from a to b will have response like this with a dc gain gm zero times r d o zero and the pole will be at 1 over r d o zero times c zero, and it will roll affect twenty degree per decked this is the transfer function from a to b in and the dc value would be gm zero r d s zero by the way earlier in the course we have analyzed the frequency response of many of this thing in great detail by writing out the expression and so on. I am assuming that your already familiar with that if not please go back and review those things. So, here I will not go into detail

calculation I will write down things by inspection if you have sufficient experience with this kind of analysis you will also be able to do the same, otherwise you can write on the expression. And make sure that there are consistence with what I am writing over here this is the transfer function from a to b through the transistor m zero.

And if you look at from b back to a through this voltage dividers gm 1 and output resistance in this capacitance will have another low pass function, and the dc gain of that will be gm 1 r o 1 times the voltage divider ratio r 2 by r 1 plus r 2 and the pole associated with this node it has a capacitance c g s zero and this resistance r o 1 in parallel. So, this will be at c g s zero r o 1. So, the overall response would have a dc gain that is product of the 2 d c gains it will have a pole here and another pole there and do that this p 1, and let me call this p 2 this will be the dc loop gain now clearly for stability we would like to have this p 2 far enough away.

So, that when the loop gain magnitude crosses unity we have a role of it minus twenty d b per decked this we know from stability analysis. So, the constraint is that the pole p 1 must be sufficiently at high frequency. So, that at the unity loop gain frequency we have twenty d b per decked slope or in other words we have a sufficient phase margin right. Now the way I have drawn the magnitude plot this is not the case.

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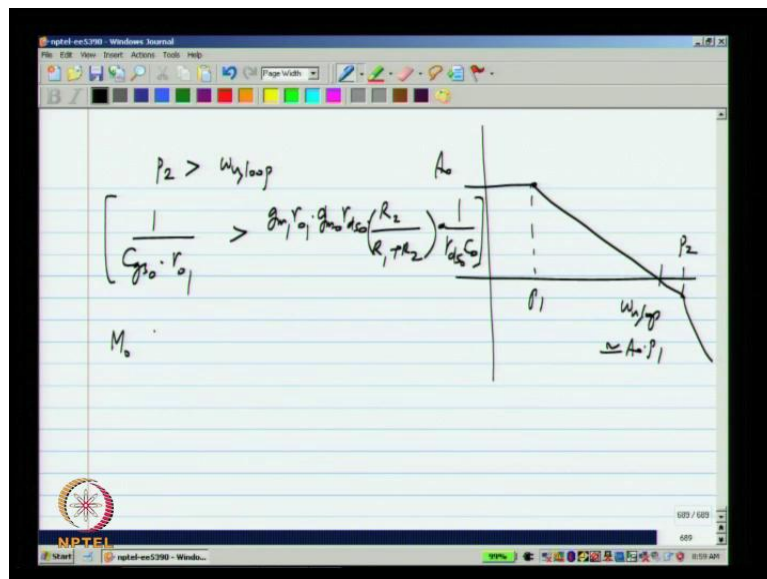
So, this means that p 2 has to be pushed out further, and p 2 is 1 over c g s zero times r o 1 and this is to be greater than omega u loop, which if it is designed well it would have a

single pole type of response and p 2 somewhere over there and this omega u loop will be approximately a naught times p 1 where this is p 1 and that is a naught and a naught we know is g m 1 r o 1 g m zero r d o zero r 2 by r 1 plus 2 d c loop gain times p 1 which is 1 over r d o zero c g s ok's is the constraint now the most transistor m zero is designed for carrying a certain load current. So that means, that it will be a very large device. So, it will have a given c g s. So, from this expression will get a constraint for the output resistance of the amplifier stage r o 1, which translates to a limiting on the dc gain, and this limits the line regulation will discuss these issues further in the next class.

Thank you .