Analog Integrated Circuit Design
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Lecture - 53
Bias Current Generation

Hello and welcome to lecture 53 of Analog Integrated Circuit Design. We have studied the number of circuits blocks in this course so far and in all of those cases, we assume that, there are bias currents and voltages available. In the next couple of lectures, what we will do, is to see suitable ways of generating those biased currents and bias voltages.

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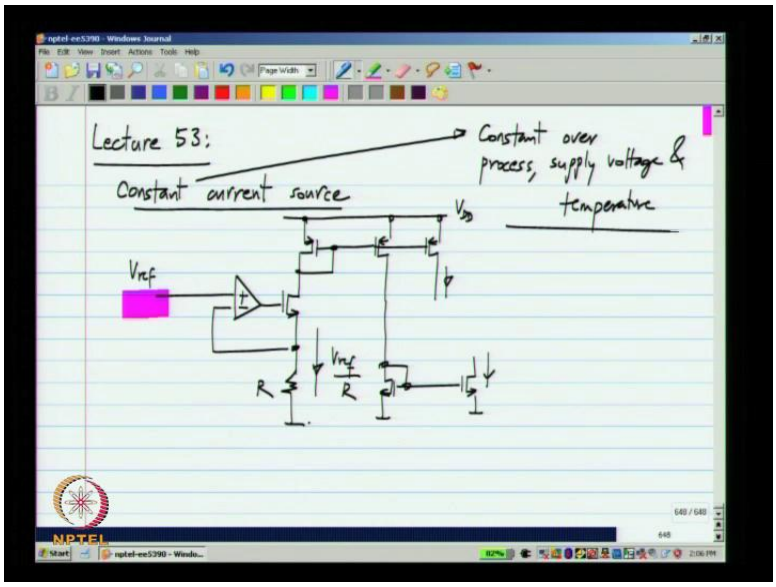

Now, first will assume that, if you want a constant current source, it is available. Now, one way to do that is, if we have a constant voltage, basically convert the voltage to current using the circuit of this sort. I want to explain, how to come over this one, but this is the very simple circuit, so this circuit is very simple. In negative feedback, the voltage at the source of the MOS transistor equals V ref. So, the current through this is V ref divided by R and if V ref is constant and R is constant, this current will be constant.

Now, how to get the constant V ref, we will not discuss now, we will discuss it later and this constant current can be mirrored to a number of places using current mirrors. If you have see MOS current mirrors, we can replicate it as many times as we want and this will push current and if you want to pull current, we can further mirror this using an NMOS

transistor. So, this is how to generate a constant current source and we can replicate it, what it needs is the constant voltage source, we will later see how to do that.

When I say constant, what I mean is, it must be constant with variation of temperature and supply voltage and process and so on. So, supply voltage will vary by some amount, if you for instant use the battery, the battery voltage will be high in the beginning then, drop down to some constant value and then, become low as it gets discharge. Also if you use a voltage regulator as well, there will be some tolerance in the output voltage. And temperature of course, can vary based on the ambient temperature and the power dissipated on the chip. And finally, there are process variations, so that means that, the component parameters are different in different process quarters.

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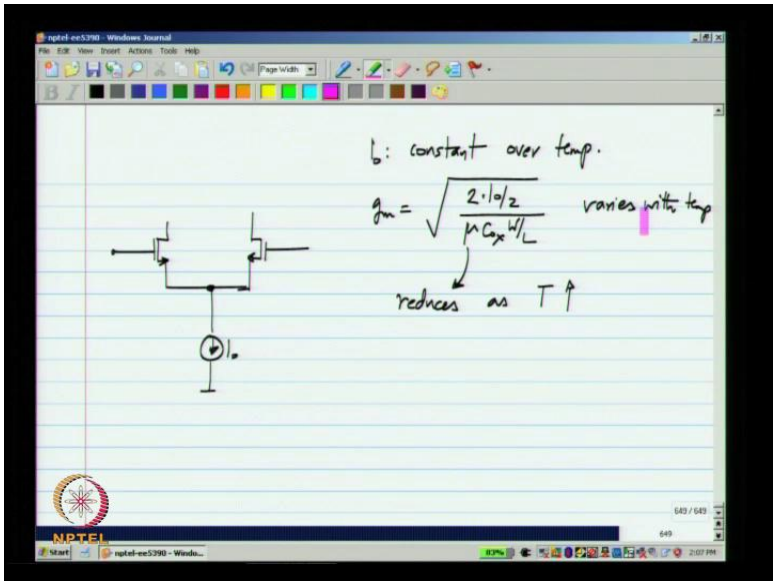

Now, the next thing is that, one of the use of the current source is to bias a differential pair or a transistor. For instance, if we bias a differential pair by this with I naught, the g m the trans conductance of this differential pair depends on I naught. Now, one of the interesting thing is to design this in a way, that keeps the g m constant. So, what I mean is, if I naught is constant over temperature, what happens is that, g m which is square root 2 times I naught by 2 for this case, divided by mu C o x W by L, this does vary with temperature, this is because, this reduces as temperature increases.

So, if you do this what happen is, at low temperature you get high g m and at high temperature you get low g m. Now, this may not be desirable, for instance now in an

opamp, the unity gain frequency depends on the trans conductance of the first stage and it may be beneficial to keep that constant over temperature. So, one of the thing is to we able to design the currents of I naught such that, the g m of the MOS transistor will be constant over temperature variations. So, we will see how to do this and for this, first we will look at a differential pair, may be by using by polar transistor, because that makes it simpler to explain. And after that, we will see that, that exactly the same circuit what for MOS transistor as well.

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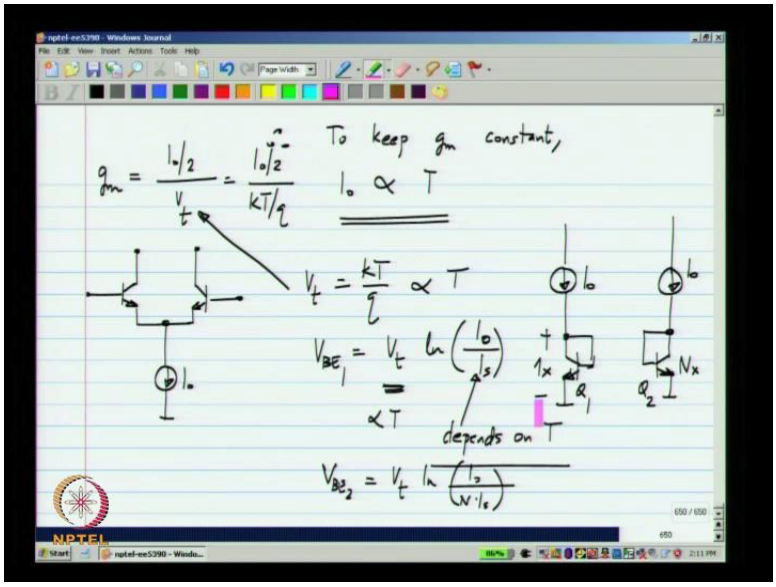

Now, g m of each of these transistors is the collector current divided by the thermal voltage. Therefore, to keep g m constant, I naught must be directly proportional to the absolute temperature, this thermal voltage is K T by q, which is proportional to absolute temperature. So, if the biased current is also proportional to absolute temperature, the ratio will be independent of temperature.

Now, how do I get the quantity that is proportional to absolute temperature, again this quantity V t this gives us the clue, this quantity the thermal voltage is K T by Q and this of course, is proportional to the absolute temperature. So, we can use this to try and come up with something that is proportional to the absolute temperature. We do know that, the base emitter voltage of a bipolar transistor or the forward bias voltage of diode is V t times natural algorithm of the collector current divided by the saturation current.

So, in this we have a term that is proportional to the absolute temperature, so let say that, I have a bipolar transistor biased to the current I naught then, this V B E will be V t times logarithm of I naught by I s. Now, this part is proportional to the absolute temperature, but this also depends on temperature, in fact it depends very strongly and temperature as we will see later. So, this by itself it is not useful, but if we notice this, we have V t times log of something.

Now, if we pass the same current, so another transistor, so let us say the area of the first transistor is Q 1 and the area of the second transistor is some N, N times that of the first one. Basically we do this so that, the saturation current of this is different, it will be N times that of the first transistor. So, V B E 1 will be V t ln I 0 by I s and V B E 2 would be V t natural algorithm I naught divided by N times I s, because the saturation current of Q 2 is N times the saturation current of Q 1.

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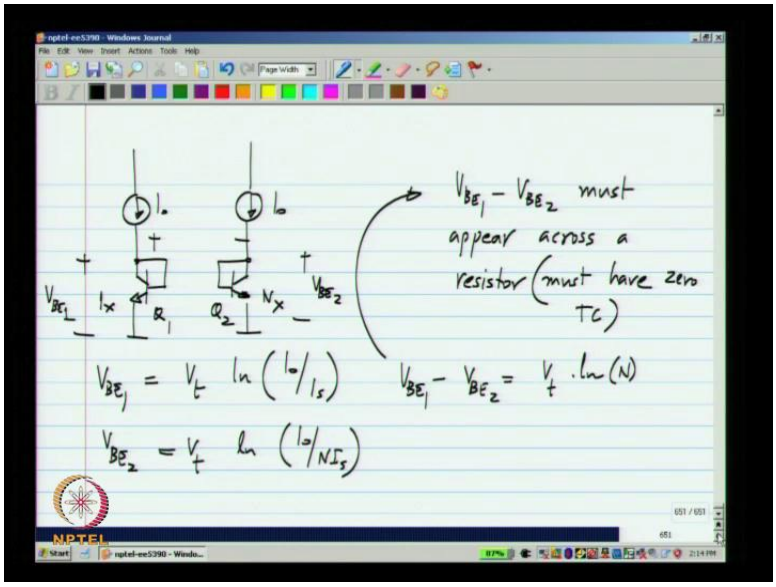

Now, if we take the difference between the 2 base emitter voltages, it turns out that, we will get exactly what we want. So, V B E 1 is V t log I naught by I s, V B E 2 is V t log I naught by N I s and the difference V B E 1 minus V B E 2 would be V t natural logarithm of N, which is the constant that is, the simply ratio between Q 1 and Q 2. As usual, for accurate realization of ratios, we will make Q 2 N units of Q 1, if you use 1 unit for Q 1, may be we can use 8 units for Q 2, so this N will be 8 and accurately realized.

So now, you have a voltage which is proportional to absolute temperature and if this voltage appears across the resistor, which is constant then, the current will also be proportional to the absolute temperature. Now, how do we do that, V B E 1 minus V B E 2 must appear across a resistor and obviously, the resistor must have 0 temperature coefficient that is, it must be independent of temperature. That of course, will not be realizable exactly, but we should try to have resistor, which has very low temperature coefficient.

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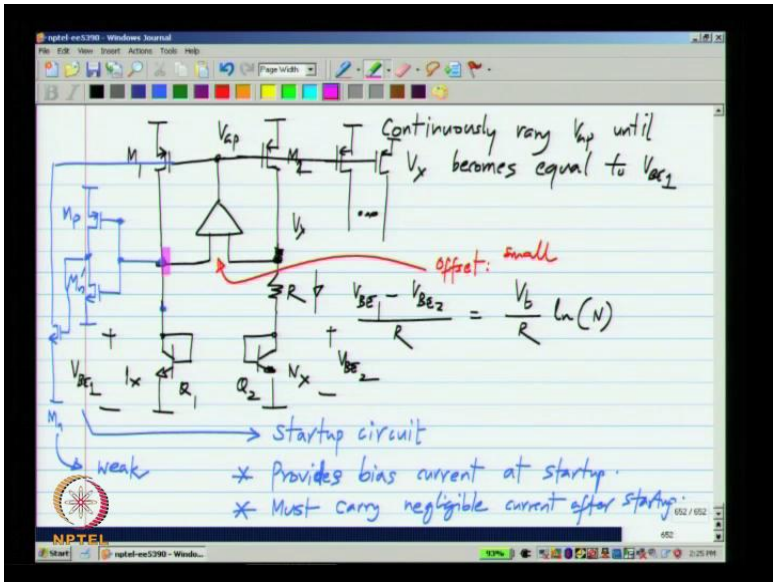

Now, how do we do this, so we have V B E over there and V B E 2, if I connect the resistor here and the voltage here happens to be V B E 1 then, clearly the current in this will be V B E 1 minus V B E 2 divided by R, which is V t by R times natural algorithm of N. So, the goal is to have V B E 1 over here, so one of the ways of doing this is, let me drive a current into this and continuously adjust the current until the voltage here becomes exactly V B E 1.

So, the reason we do this is that, finally we have to be able to replicate this current as well. So now, if we have adjusted this current source by some means, by some means meaning, we have to adjust the gate voltage of this until the current in this is such that, the voltage here becomes V B E 1. And we can also make multiple copies of this current by copying the source gates voltage of this transistor one to other identical transistors.

So, and how do we do this, we compare V x with V B E 1 and if V x is different from V B E 1, we have to adjust V G P.

So, we integrate the difference between the two, so using an opamp and drive V G P and we have to do it until V x becomes equal to V B E 1 and we have to adjust the signs of this opamp so that, the circuit design negative feedback. So, with this arrangement, that is possible, we have done this for many things. Now, the other thing is that, the difference between these two voltages, V B E 1 and V B E 2 will be equal to V t ln N if the currents in the two transistors are the same.

I am not shown how to bias the transistor Q 1, but the current in this has to be exactly same as that. Now, the current in this has been adjusted to the right value, if everything is working properly. So, we can replicate to that into another p MOS transistor and bias it, now M 1 and M 2 are identical, so the currents in these two transistors will be exactly identical. And also because, the gate of this is driven by integrating the difference between V x and V B E 1, V x will be equal to V B E 1.

So finally, when the circuit reaches steady state, the current in this equals V B E 1 minus V B E 2 by R, which is V t by R times ln N. Now, this has a certain snakes following it is own tail quality to it that is, we bias the second branch using the first branch. And then, the first branch itself is biased by replicating the current from the second branch on to the first branch, so this kind of circuits are known as self biased circuits. As you see, there is no current source here, no other currents source that biases of the circuits.

If the circuits reaches the right steady state, the current will be equal to V t by R times ln N in both the branches. Now, one of the problems with these circuits and in fact, this happens rapidly with the bias circuits is that, it has two possible states, one possible state is what I just showed you, the other state is when both the currents are 0. If both currents are 0, V B E 1 and V B E 2 will both be 0 and the gate voltage V G P can be V D D, this is possible.

If that possible, all transistor are off and the circuits will be in steady state, clearly that is not the operating point that you would like to have, you would like to have the operating points, where the currents in both are non zero. If it is non zero then, the only possibilities for them to be V t by R times ln N. So, what is done in this circuits is to make sure that, when you switch on the circuit, it starts up properly. You provide a

starting current that is, if some voltage is struck to V D D or ground you make sure that, it increases above that.

Once it increase above that, the circuit will reach the correct steady state and at that point, the extra current should becomes 0 or negligible. So, one way to do that is, so let us say we find that, this voltages is V D D and this voltages are at 0. Now, if we pull down the gate voltage of this transistors what happens is, M 1 and M 2 will carry some current and these voltages will be lifted above ground. Once it lifted above ground, the negative feedback comes into picture and entire circuit reaches the operating point.

There is couple of ways to do this, in some circuits a pulse is available at start up, using that, this voltage can be pulled down momentary. Now, we will assume that, no such pulse is available, in that case what you do is, you have to pull the current using the n MOS transistor. And if you make this gate voltage high, it will pull the current, so what can be done is, circuit of this sort. Now, this p MOS transistor will pull the gate of the n MOS transistor high, if it is gate is at 0.

Now, we saw that, if the operating point is 0 then, the base symmetric voltage here will be 0, V B E 1 or V B E 2, so we can take the signal. So, if this happens to be 0 at start up, this p MOS transistor will pull the gate of n MOS transistor up, let me call this M p and M n. M n gates will be pulled up and this will draw a current and once this draws a current, this V G P will pull down and these two will push current into the bipolar a transistor and this voltage will be lifted up.

Now, what must also happen is that, if this voltage is lifted up to the sufficiently high value then, this M n should not drawing any current and that can be ensure by connecting it up like that. Essentially we have a CMOS inverter structure here, so if this voltage reaches sufficiently high value, which is 0.7 volts or so, this transistor tends to pulls this node down and deactivate M n. Now, of course all these things have to be adjusted by simulation, the sizes of all these things.

This M n will be rather weak that is, it will carry a small current to begin with and that current should become even smaller when this voltage goes to the appropriate value. And let me call this, I mean dash, the M p and M n dash should be sized such that, when it reaches the appropriate value, overall process corners, the current in M n becomes

negligible. So, this is the example of, what is known as a start up circuit, it provides some biased current at startup.

This is to ensure that, you do not get stuck with the zero operating point and must drop out to the picture that is, must carry negligible current after start up. So, that is the role of the start up circuit, lot of this reference circuits will be self biased, because you are using the reference to generate some biased current or biased voltages. And that is used in the references itself and such circuits need this start up. There are more elaborate kinds of start up that you can think as well and you can also find them in the literature.

So, what we have here is a circuit, which provides a biased current, which is proportional to the absolute temperature. And if you bias a bipolar transistor differential pairs or a bipolar transistor using this, it is trans conductance will be constant with temperature. So, what we do, we can replicate these currents any numbers of we want and views both bipolar and MOS transistors here. Our dominant technology is MOS, but if necessary these current sources can also be realized using only bipolar transistor.

And this opamp also is realized using either CMOS or bipolar, depending on the process that you have. Now, one of the things is that, the offset of this should be small, because ideally these two voltages are made equal by the action of the negative feedback. But, in reality, there will be a difference between them, equal to the offset, so that will cause in error in the current. So, you would like the offset to be as small as possible so that, the error will also as small as possible.

Now, one of the other things to be considered is that, unlike in many other circuits, in this circuit, the opamp has feedback to both terminals, both of the input terminals. So, we have to figure out the signs of the opamp so that, the overall action is of negative feedback. And that can be done a very easily, just as usual by breaking the loop and applying a test voltage and so on.

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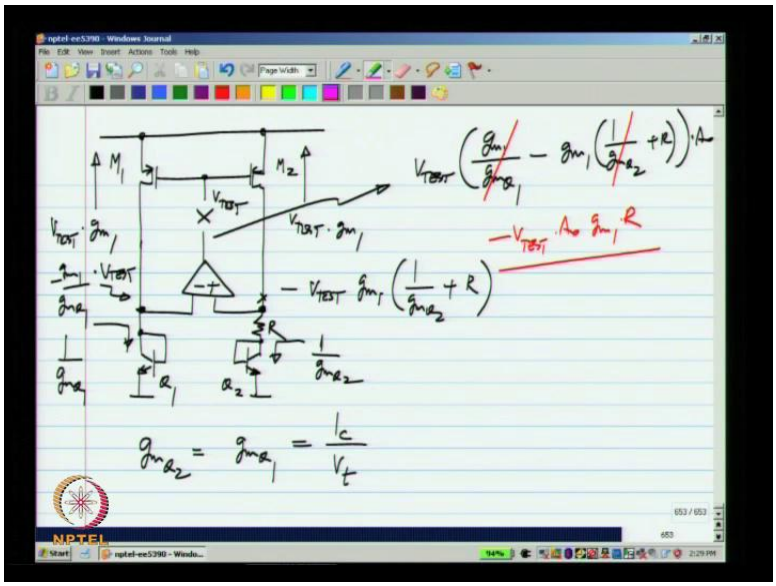

I have chosen to break the loop at the output of an opamp and I will apply it as test voltage V test. I will assume that, these two are identical of course, M 1 and M 2, so the incremental currents in both of them will be V test times g m 1 and the incremental voltage here will be V test times g m 1 times the impedance looking down and that is nothing but, 1 over g m of the transistor Q 1. So, the voltage here at this point will have minus g m 1 by g m Q 1 times V test.

And similarly here, we have R and the impedance looking down there is 1 over g m Q 2, the voltage that appears here is minus V test g m 1 1 over g m Q 2 plus R. Now, depending on which one is greater, we have to assign the signs appropriately and that depends on the relative values of g m Q 1 and g m Q 2, but these two transistors are biased at the same currents. So that means that, g m Q 2 equals g m Q 1, the g m of a bipolar transistor depends only on the collector current and the expression is I c by V t for both.

So, you can clearly see that, this g m 1 by g m Q 1 is some number and here we have g m 1 times 1 over g m Q 1 plus R. So, the gain from V test to this point is more negative than the gain from V test to that point. If you make the signs of opamp like this then, the voltage here would be V test times g m 1 by g m Q 1 minus g m 1 1 over g m Q 2 plus R times the gain of the opamp.

And because the two bipolar transistor g ms are equals to each other, this part will cancel out with that and will be left with minus V test I naught g m 1 R, implying that there is negative feedback with this particular configuration of the opamp. So, this is something also that happens repeatedly with biased circuits, you may have opamps with feedback to both the inputs .That is very simple to analyze, all you have to do is, again break the loop appropriately and look at the small signal gain after breaking the loop and make sure that, the loop gain is negative.

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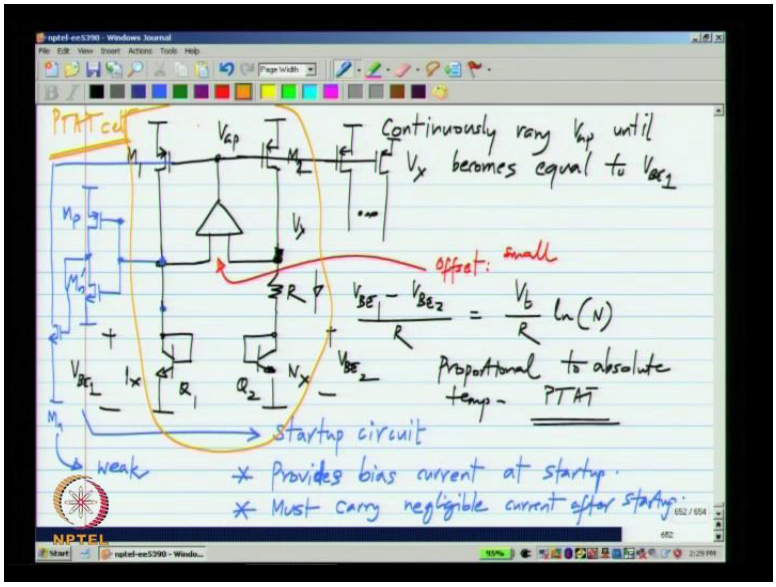

So, the circuit that we have here has a current that is proportional to absolute temperature PTAT, so this is many time called a P TAT cell. So, this part of the circuits is a P TAT cell, so this is way of generating a current that will make sure that, the g m of bipolar transistor will be constant with temperature. Now, what can do with MOS transistor, it turns out that, exactly the same circuits will go work with MOS transistor as well. The expressions are different for the current in MOS transistor and current in bipolar transistor. Now, even for MOS transistor in strong inversion saturation region, exactly the same principle watch.

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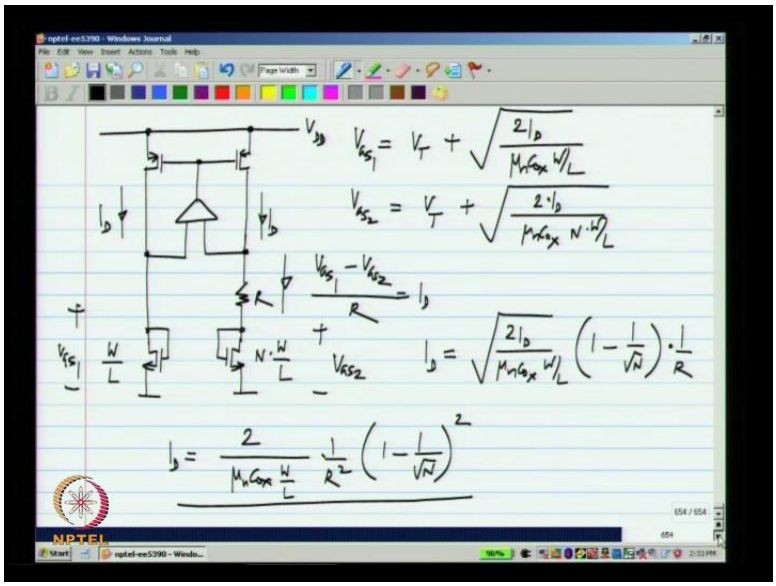

Let us see this has a certain W by L and this has N times W by L and we will assume that, it is operating at a operating point, which is different from 0. This is V G S 2, this is V G S 1 and the current is V G S 1 minus V G S 2 divided by R. Now, what is V G S 1 that is, V t threshold voltage plus square root of 2 I, whatever I is flowing here, let me call it may be I D, 2 I D by M n C o x W by L. And V G S 2 is the same threshold voltage plus square root of 2 times I D by M n C o x n times W by L. I also saw that, I d equals the different between these two voltages divided by R.

So, I D comes out to be square root of 2 I D by M n C o x W by L 1 minus 1 over square root of N. The first term comes from V G S 1, the second term from V G S 2 times 1 by R and if you solve for this, I D you can easily see is 2 by M n C o x W by L 1 by R square 1 minus 1 over square root of N whole square. So, you can adjust N to be let say 4 or something and then, you will get some number over here.

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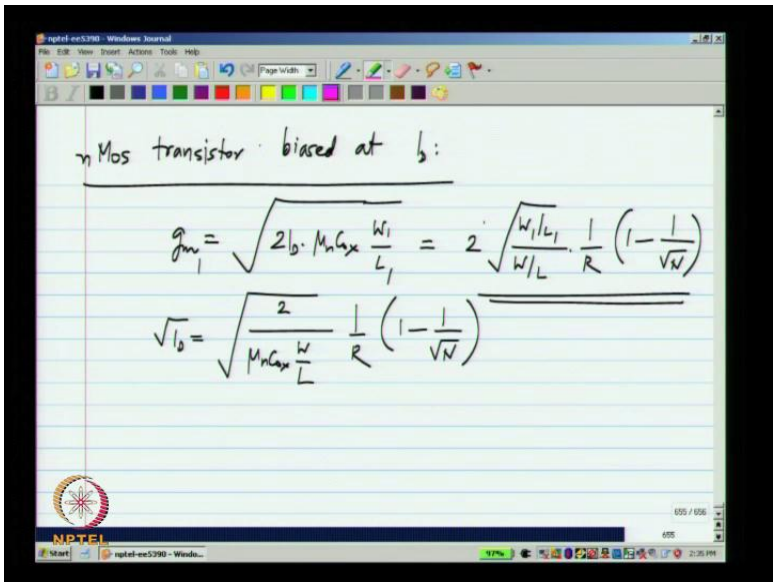

Now, the point is that, if you bias the MOS transistor using that, by the way here we are talking n MOS transistor, because this V G S difference, that we have taken with the n MOS transistor. With the p MOS transistor, we will have mu p here and it will be different. n MOS transistor biased I D, it is g m will be square root of 2 I D M n C o x and I said W 1 by L 1, to distinguish from other transistor. And what is I D, we know that, square root I d equals the square root of this quantity, which is so g m 1 will be, the mu n C o x will go away, that is the important part here.

Assuming as before, that R is independent of temperature, you see that this g m 1 is independent of temperature, it is related to the ratio of aspect ratios, that will be independent of temperature. The transistor will be well matched and this number, which again depends only on matching, N is the aspect ratio of two transistors used this side. It turns out that, exactly the same circuits that works to establish a constant g m in bipolar transistors, also works for MOS transistors. Now, it is the assume that, the MOS transistor are operated in strong inversion saturation. If the MOS transistor are in a weak inversion that is, sub threshold region then, the MOS transistor behaves as same as bipolar transistor. It will have the exponential I V relationship and then, also it works, so this circuits also works for MOS transistors.

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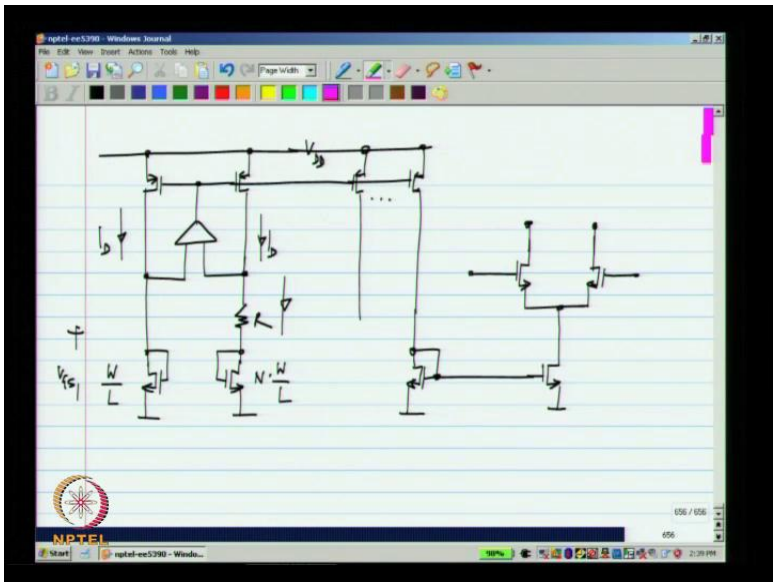

But, there is a slight problem with this, now anything else that we want to bias, we can also replicate this currents and use it as many times as we want. And if you want to pull current, we can further mirror it with the an n MOS transistor. But, one of the problems is, let us say I want to bias a differential pair with this kind of a current. I can do scaling as well, the currents in this do not have the exactly same as this, it can be scale version of that.

For that, I can use scaling in the current mirror, now nominally this transistors will have exactly the same characteristics of those transistors and everything works the same. But, in reality what happens is that, there will be body effect in this, there is no body effect in that and so on. You will see that, the g m of this will be slightly different from the g m of this one and the tracking will not be perfect. So, that is one of the issues with this one, also we derive this relationships using square law that is, the transistors are in strong inversion saturation and so on.

We also know that, as we go to shorter and shorter technologies, the transistor do not exactly follows square law. Any deviation from square law will also cause deviations from this behavior that is, the g m will not be proportion to 1 over R, as we have predicted by the expression we derive. So, there is an alternative circuit, which is more fundamentally sound and that is the then, that utilizes just the definition of g m. What is

g m after all, if you apply a small signals to a differential pair, the current will be g m times the small signals input.

So, in those cases, where you stabilize the trans conductance of the differential pair, you can use better circuit than this, which will keep the g m constant. And that will be independent of square law and independent of, whether they are in strong inversion or not. And also it turns out that, it is not so effected by body effect that is, you make sure that, the transistors that you use in the biasing cells have the same body effect as the transistors that you used as a differential pair, now how do we go with doing that.

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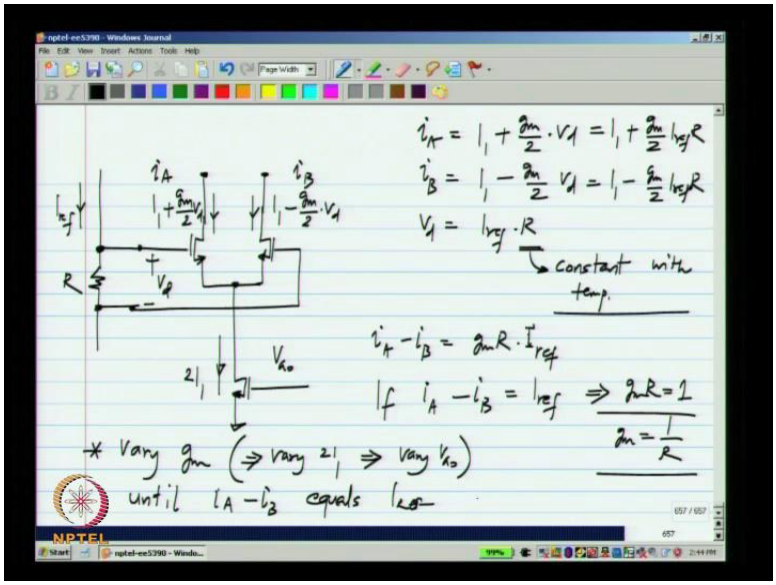

So, let say the differential pair is biased to the certain current 2 I 1, that is the tail current, in cohesion condition, each of these currents will be equal to I 1. And if an increment V d is applied then, the current in the left side will be I 1 plus g m by 2 V d and here it will be I 1 minus g m by 2 times V d. And let say that, I generate the V d by passing a reference current I ref, I am not shown the complete circuit yet, but I ref through R.

So, this V d will be simply equal to I ref times R and let me call these two drain currents i A and i B, i A is I 1 plus g m by 2 times V d, i B is I 1 minus g m by 2 times V d and V d itself is I ref times some R, again this R is assumed to be constant with temperature. So, this current will be nothing but, I 1 plus g m by 2 I ref R and this will be I 1 minus g m by 2 and I ref R. Now, if you consider i A minus i B that is, g m R times I ref and if you make i A minus i B equal to I ref that means, that g m R is 1 or g m will be 1 by R.

Now, what it mean is that, I have to change the trans conductance of the differential pair until this g m R times I ref, which is the output differential current of the trans conductor equal the reference current I ref. In those conditions, obviously g m times R is 1 or g m will be equal to 1 by R. As we have said, R is constant with temperature, so g m also will be constant with temperature. And as you notice in this case, we have not use anything of the particular characteristics of the MOS transistor.

We have a simply assume that, it is operating in a small signal regime so that, the differential output current can be written as g m times the differential input voltage I ref times R. So, as long as that is valid, this circuit will work, now what we have to do is, to complete the arrangement so that, the trans conductions of the differential pair is varied until it is output differential becomes equals to I ref. We have to vary g m and how do we vary g m, by varying the tail current to I 1 which means, I have to vary to I 1, which in turn means that, I have to vary this V G naught, until i A minus i B equals I ref.

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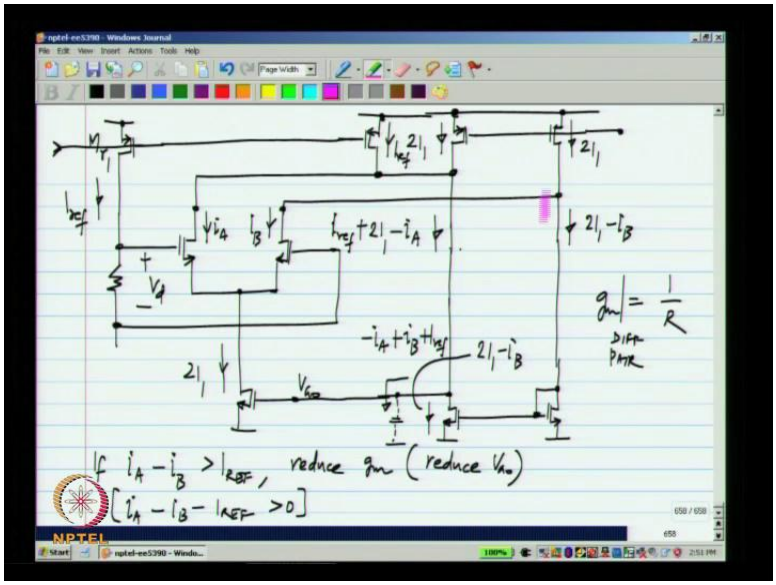

So, we will see how to do that, I have to arrange it such that, if i A minus is i B is more than I ref, I have to reduce g m which means, I have to reduce V G 0. And similarly, if i A minus i B is less than I ref, I have to increase g m and increase V G 0. In other words, this same condition written differently, so we have to be able to take this term here, i A minus i B minus I ref. So, let us say I ref is provided by some MOS transistor, I will call

this M r 1 and anything else connected with the same source gate voltage will also provide the same current either.

So, what I will do is, I will first fold this currents, the reason I have to do that is because, finally I have to provide a control to the n MOS gate. So, I will use the folded cascade structure and this biased currents will be 2 I 1, it will be the same as this one. And by using appropriate current mirroring arrangement, I can make sure that, the current here is same as the current ref. All I have to do is, to bias this gate appropriately so then, what happens, at this point I will get 2 I 1 minus i A and here I will get 2 I 1 minus i B.

Now, using another current mirror arrangement, imagine the parasitic capacitance here so that, we can see which were voltage will go. If I use another current mirror like this what happens is, here I get, this current will be 2 I 1 minus i B as well, it simply the same as that current, so current of minus i A plus i B tends to flow in this one. Now, what happens is, this voltage will increase or decrease depending on, whether this current is positive or negative.

Now, this is close to what we want, but not exactly the same, what we want is the extra term of I ref. We want this voltage to increase or decrease based on i A minus i B minus I ref and that is very easy to arrange. All I have to do is, I have to add the current, which is I ref which means that, I simply have to bias it from the same voltages that one, so here I will get 2 I 1 minus i A plus I ref. So, the current here also be minus i A plus i B plus I ref.

Now, what happens, if this term is more than 0 that is, i A minus i B minus I ref is less than 0 then, this voltage will go on increasing. And similarly, if this term is less than 0, this term will go on reducing and you see that, that is exactly the directions that we wanted. So, you can go through the synthesis yourself and make sure that, it is in the current directions, so all I have to do is, to connect it here. Now, what happens, this voltage will reach the steady state, it will stop varying only if this term equal to 0 that mean that, i A minus i B equals I ref and that is exactly the condition that we want.

So, what the circuit does is to make sure that, the g m of the differential pair, remember this is not working on the g m of the just transistor, but it is for the differential pair equals 1 by R. Now, earlier I said that, first of all this is not sensitive to, whether the following square law, because we not used that anywhere. All way we assumed is that,

this differential voltage V d is small enough so that, the output current of this differential pair can be represent as something being linearly related to V d.

So, it has been operating in the small signals region, that is easy enough to arrange or the other thing is that, finally what we do is, we will replicate this current to I 1 and may be scale it and use it in another differential pair. One of the problems with earlier arrangement was that, this transistor whose g m is stabilize to something inversely proportional to R are operating with 0 V S B, whereas this transistors are not operating with 0 V S B.

So, really operating with different body effects, whereas here and it can make sure that, the common mode input of this differential pair is the same as the common mode input of the differential pair I am using. So, this transistor and the actual transistor that are used, will be suffering from the same body effect or will be suffering from body effect to the same extent. So, there will be no difference induce by body effect either, so this is the much more robust way of realizing the constant g m differential pair that is, differential pair whose g m is constant over temperature.

So, I just couple of more details that will filling quickly, we need to know what we do with this node and also how generate this sources. Because, we do not want to be biasing with some other eternal sources, again we use the principle of self biasing.

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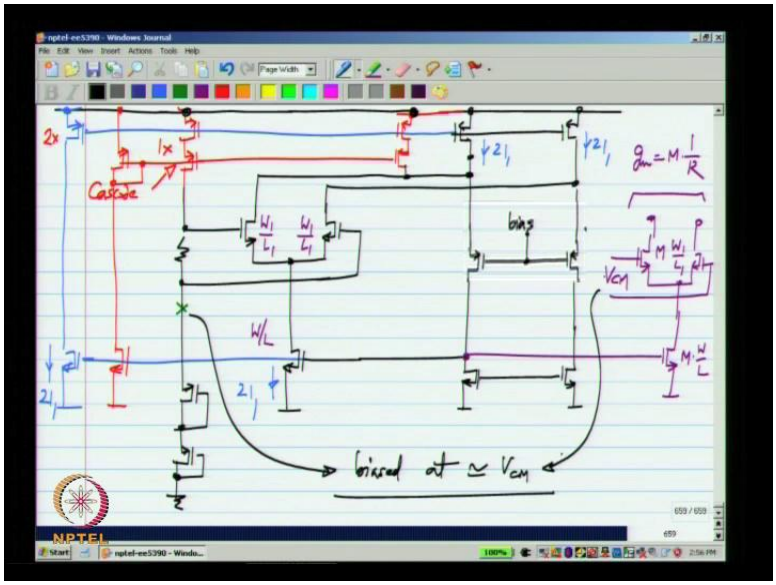

Let me redraw this quickly, this is the differential pair whose g m is being stabilized and this is the folded cascade arrangement, so what we do is, we use self biasing. So that means that, finally when this current is 2 I 1, this will be 2 I 1 and these currents also be 2 I 1. So, this I have to add, the current sources I ref, now it is possible to do like this that is, you make I ref also equal to I 1. Say, this is 2 X and this is 1 X and this is 1 X and so on, so I ref can be made equal to I 1.

But, one of the important things is that, the current that is injected and the current that is injected here, should be matched very well, there cannot be any error between the two. Because, finally we are realign on this current being exactly I ref for the negative feedback to settle to the correct operating point. So, we may have to use accurate current sources here, so it could be that, you will use cascade. So, in this particular place, you can use cascade arrangement, instead of a simple current mirror.

So, all the upper rails are V D D of course, here you use the cascade, the cascade bias can also be generated, we have discuss it earlier in a different context. But, they can also be generated from some arrangement, where this transistor has much smaller aspect ratio than the other transistor so that, this gate voltage is lower than that gate voltage, that is possible. And finally, we have to fix the voltage at this particular node and that is fixed such that, the common mode voltage of this differential pair is similar to the common mode voltage of the differential pair we are trying to bias.

So, let me draw that, so let me just show a representative differential pair, if this has W by L and this has W 1 by L 1, you could be using a scaled version of it that is, M times W by L and M times W 1 by L 1 over there. Then, the g m of this would be equal to M times 1 over R and this differential pair will be operating with some V c m. So, what you do is, you use whatever biasing arrangement that is possible, for instance you can simply use a diode connected transistor one or two of them.

Basically, the point is, to bias this at a approximately the V c m of the differential pair that you are using so that, the differential pair whose g m you are locking to 1 over R and the differential pair that you are using are operating at around the same condition. That is why, we come up with bias currents, which will bias the transistor such that, their g m is constant with temperature.

And this is very important in certain application, many times in filters and so on, where you would like the characteristics not to vary with temperature. We will continue on these things and also see, how to generate voltage references in the next lecture.

Thank you.