Analog Integrated Circuit Design
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Lecture - 52
Phase Locked Loop

Hello and welcome to lecture 52 of **A**nalog Integrated Circuit Design. We have looked at the transfer function in phase lock loop in some detail, we saw how the phase noise of V C on the reference appear at the output and we also saw, how random noise from charge and loop filter appear at the output. So, we can now figure out what the overall phase noise of the phase lock loop looks like. It of course is dependent on the exact parameters used in a particular implementation, but we can say something about the general nature, that you will see in all phase lock loops. So, after discussing that, we go on to some implementation of oscillators.

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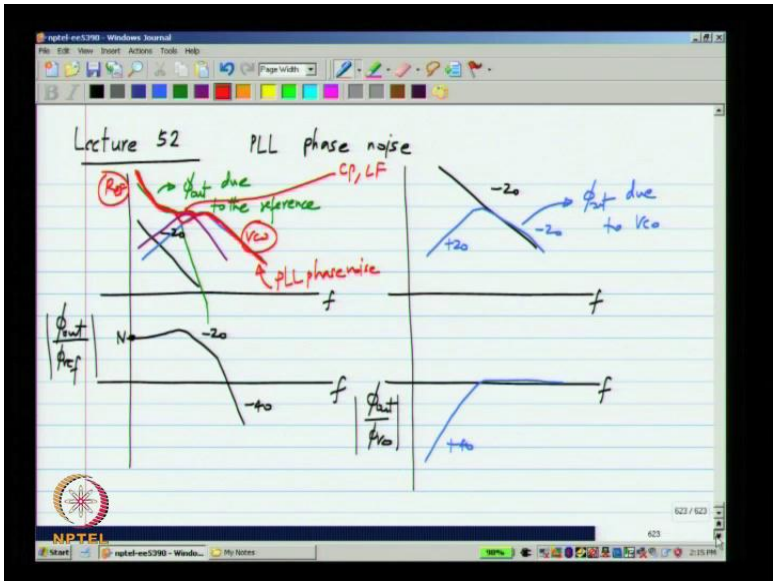

The phase noise of the reference oscillator will have 1 over f square frequency dependents that is, minus 20 dB per decade if you plotted verses frequency. And if you plot the magnitude of the transfer function from the phase of the reference signal to the phase of the output signal, that could be a low pass function, which would look somewhat like that. And the exact shape depends on the parameter chosen, but we except

that it will have some minus 20 dB per decade region then, minus 40 and then, even more if you have higher slopes.

And this point has a gain of N, now of course all of this are plotted on log scales, so the contribution of the reference phase noise to the output will be N times higher at low frequencies and there could be some peaking as well. And then, after that, it quickly drops out, so this is the output phase noise due to the references. Now, if you look at the V c of phase noise, that will also have a minus 20 dB per decade dependence, but usually the V c of phase noise is much much higher that is, much worse than the reference phase noise.

It is very common to use a crystal oscillator for a reference and that has the very high quality factor and therefore, a very low phase noise, whereas the V c o will have a higher phase noise. One of the application were PLL, is to clean up the V c o's phase noise and the transfer function between the V c o of phase noise and the output, the magnitude would be something like this, it will be 0 dB and within the band width, it will rise at plus 40 dB per decade.

So, when the V c o's phase noise is multiplied by the magnitude squared of this transfer functions what we get is, something of this sort. Beyond the bandwidth of the PLL, it follows the V c o of phase noise and below that, it drops of at minus 20 dB per decade as it approaches low frequencies. So, this stuff now is phi out or S phi out due to the V c o, if you put these two together, it is common to see something of this sort.

And the overall phase noise would be dominated by the reference at low frequencies and by the V c out high frequencies and it dependents on the charge from point the loop filter, they could also be contributing somewhere in this region. For instance, the loop filters noise could do that in which case, the overall phase noise would follow that as well. So, this is the phase noise of the PLL and it is dominated by the V c o in this region, the reference in the region and it could be dominated by the charge pump and the loop filter in the intermediate region.

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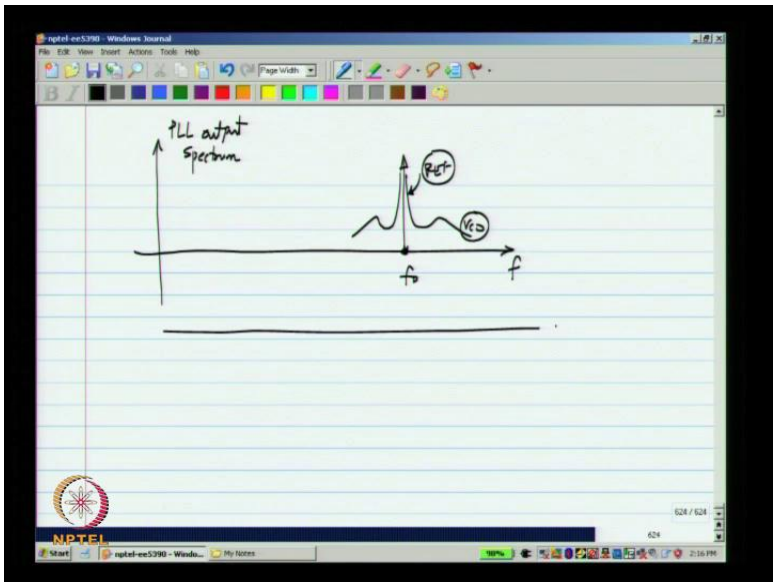

So, if you plug in any signal generator, which uses a PLL into a spectrum analyzer, it is very common to see a sharp peak corresponding to the periodic signal and phase noise, side bands like this were, here it is dominated by the V c o. And here it is dominated by the reference and of course, on the upper and lower side, you will have exactly the same things replicate. This by the way, is the spectrum of the voltage or current, which has this as the phase.

So, when you have an opportunity to play around with this signals generator and as a spectrum analyzer, you can plug it into the spectrum analyzer and set it to the approximate bandwidth so that, you can see the picture like this. Now, what we will do next is to see, how the voltage control oscillator can be realized. We have looked already at, how to realize the charge pump and the phase detector and the realization of the frequency divider will not going into the detail here, but it is a digital counter and there are many ways of making that. Our first we will look at, how to make the V c o, there are few different ways. We will only touch upon some representative topologies and also say something about, how their phase noise would be.

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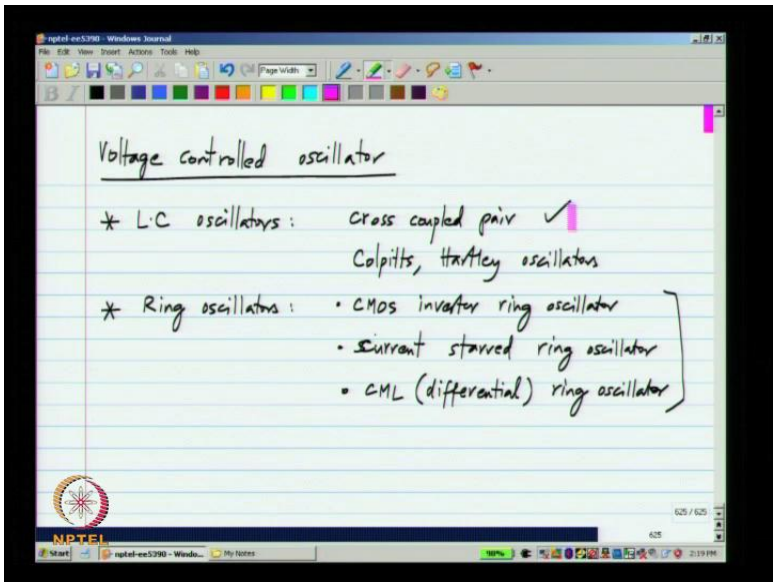

Now, there are two types voltage controlled oscillator, one which use a passive inductions and a capacitor as the resonator and these are known as L C oscillators. And there is number of varieties, one we chooses the crossed coupled pair, this one I will discuss in some detail and the others more traditional varieties like the Colpitts and Hartley oscillators. It turns out that, in CMOS technology, the cross couple pair oscillator is the most popular, so that is the only one that will discuss here.

And then, there are ring oscillators, which do not have passive inductor, but which use a number of amplifier stages to realize the delay line. And in this, there are numbers of varieties, the CMOS inverter, ring oscillator, the stuff that is most the commonly known and there are some variants like a current starred ring oscillator and also the CML differential ring oscillator.

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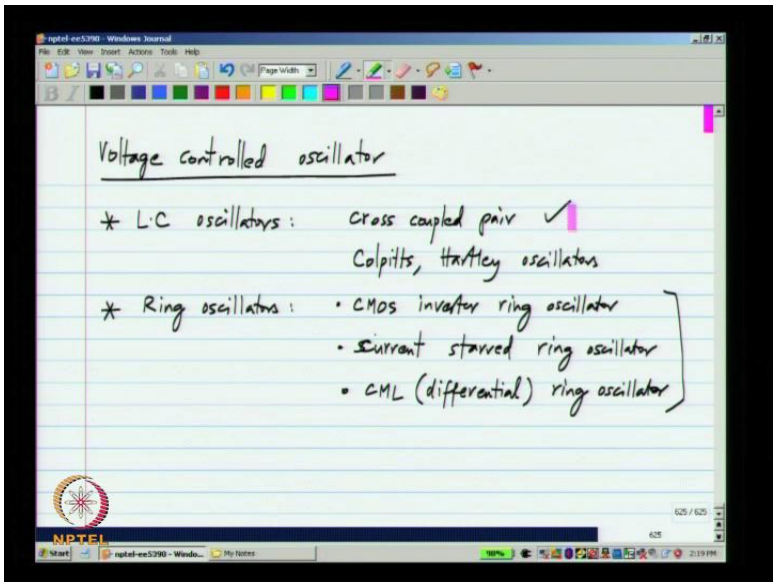

First coming to the cross coupled L C oscillator, the principle of all L C oscillators is the same, you connect an L and C in parallel. And if the inductor and capacitor were completely loss less and if you have an initial condition on say the capacitor voltage then, you will see a sinusoidal oscillation at a frequency 1 over 2 pi square root of LC. And this will be sustained indefinitely across the capacitor, because no energy is loss from the system.

Of course, no real inductor or capacitor is loss less, so there inductor will have some loss, because of a series resistor and many other factors, similarly the capacitor will have some losses. So, if you do a set up an L C in parallel and establish initial condition of the capacitor, eventually it will die down. So, the principle of a L C oscillators is to in one way or the other, connect the negative resistance across the L C bank so that, the loss which is represented by some positive resistance is cancelled by the negative resistance that you connect outside.

Of course, the negative resistance is negative resistance only in the increment sense and it is made using transistors. Now, first a quick word about representing the loss of inductors and capacitors, typically the inductor will have some loss because of the resistor of the wire itself. You know that, inductor is made using wire, which is wound around and there will be some serious resistance R s and because of that, there is some loss.

Now, if you look at the impedance of this between these two terminals, it will be R s plus j omega L. And if you look at the admittance, it is 1 over R s plus j omega L, which can be written as R s minus j omega L by R s square plus omega square L square. So, it is a combination of two elements in a parallel, which have some complex impedance. Now, the quality factor of this, which is the imaginary part of the impedance divided by the real part of the impedance is nothing but, omega L by R s.

And you know that, the quality factor is related to, if you apply a sinusoidal across this, peak energy stored in the inductor to amount of energy lost in every cycle, it is related to that one. So, as R s becomes smaller and smaller, this approaches an ideal inductor and quality factor will be infinity. Assuming that the quality factor is sufficiently large, much larger than 1, this basically means, omega L is much more than R s. This admittance can be approximated by R s by omega square L square minus j over omega L.

In both cases, I have neglected the term containing R s in the denominator, when I compare it well omega L. And what is this, this is the combination of a resistance and a negative susceptance or basically inductance in parallel. You can write this as 1 over R p minus j over omega L or plus 1 over j omega L. So, exactly the same thing can be represent as L in parallel with R p and what is the value of R p, this is omega square L square by R s.

So, it is dependent on frequency, but were you are interested in only a single frequency or a narrow band frequency, this can be replace by that particular frequency omega naught. It is only in that situation that, this kind of representation and interchange between the series and parallel is useful, otherwise the resistance becomes dependence on frequency. But, let say an oscillator, you are interested in just a single frequency that is, the frequency oscillation and some narrow range around it. So, you can evaluate this quality factor at the desired frequency and the parallel resistance will be square of the quality factor times the series resistance, which is basically given by Q square times R s.

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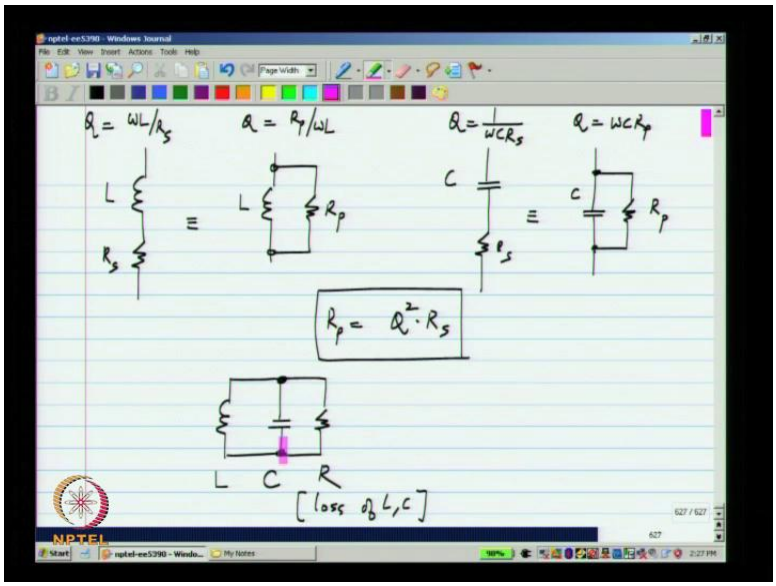

So, in general, both the capacitor and the inductor can be represented with, either a series resistance or a parallel resistance that is, loss in the capacitor can be represent with, either a series or a parallel resistance. And the relationship between the two is given by the square of the quality factor that is, R p is Q square times R s. And this makes sense, because in the series combination if you set R s is equal to 0, this becomes an ideal inductor and in the parallel combination, if you set R p equal to infinity, it becomes an ideal inductor.

So, the quality factor of this is given by omega L by R s, the quality factor in terms o R p would be given by R p by omega L. Similarly, quality factor here is given by 1 over omega C R s and here it is given by R p by R p times omega C. So, in all cases, you should look for the extreme case, where Q equals infinity that means, an ideal element. If Q is infinity, this will go away, similarly if Q is infinity that will go away and so on and in all cases, the series and parallel resistances are related by this.

The reason that I mention this is, there are many sources of loss, both the inductor and capacitor will be lossy. What we will do is, we are simple lump all them into single parallel resistance across the parallel L C network. So, I could have L with some losses and C with some losses, I will represent the loss of both L and C with respective parallel resistances and combine them into a single parallel resistance R, this represents loss of L

and C. Now, clearly if you set up an initial voltage across the capacitor, it will die down and it will this sustain for some cycles and it eventually die down.

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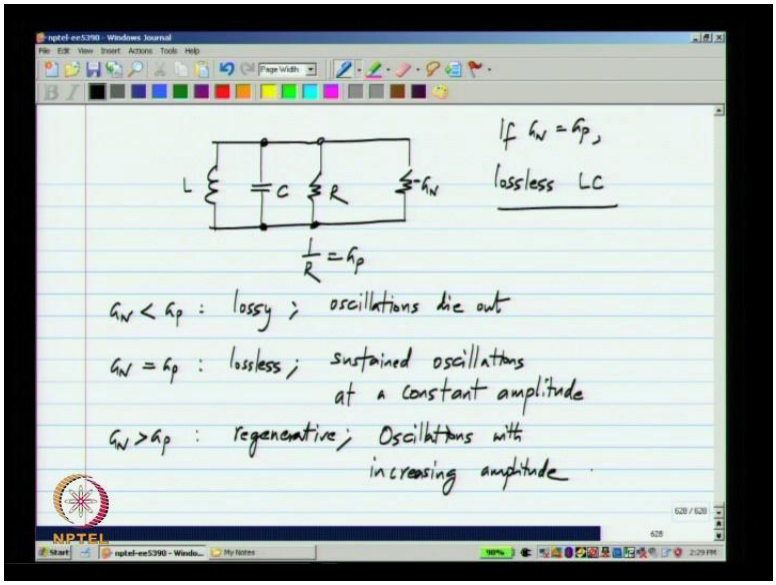

So, what we do, I will call this 1 over R is the positive conductance G P and if I connect the negative conduct minus G N then, if G N equals G P, I will have only L and C in parallel that is, a loss less L C. So, what happens in this case, if G N is smaller than G P then, the net conductance will be still positive, so it is still lossy and oscillation die out. And if G N exactly equals G P, it is loss less and you will have sustained oscillation at a constant amplitude.

And if G N is greater than G P, it is actually regenerative and you will have oscillation with increasing amplitude. Now, if the circuit were exactly linear that is, both L C and R and also the negative resistance are all linear then, if you make a G N greater than G P, what happens is, you will have exponentially increasing amplitude of the oscillation across the capacitor. But, of course in reality, the negative conductance G N is realized using an active circuit, which will have it is swing limits.

So, the amplitude will increase lesser from very small values and then finally, reach the swing limits and reach steady state. And there will be oscillations of some fixed amplitude, that depends on the swings limits of the amplifier and the particular details of the amplifier. Now, what happens is, although G N equals G P will give rise to

oscillations of a constant amplitude, in practice the oscillator are designed with G N greater than G P.

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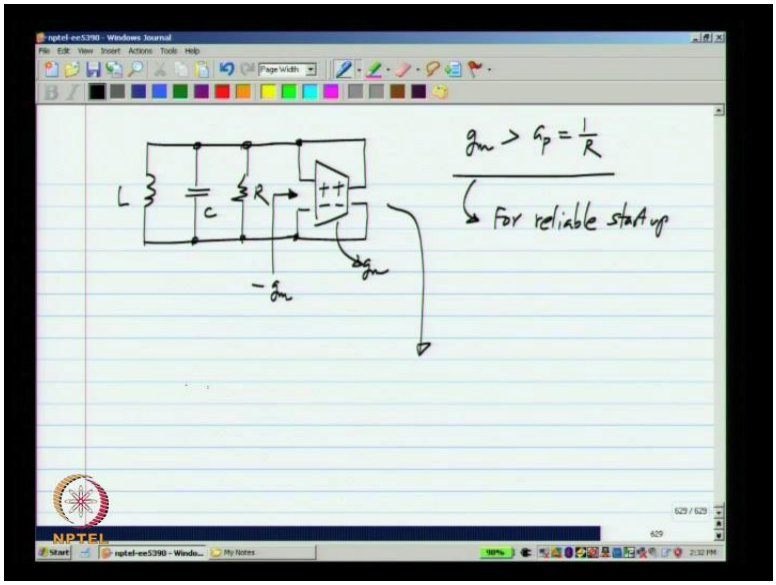

Now, how do we realize the negative resistance, essentially one easy way of realizing it is, using a trans conductance in positive feedback. If the trans conductance value g m, this will be minus g m, now what should the value of g m be, g m is usually deigned to be sufficiently greater than G P, which is 1 over R. This is because, this g m is evaluated at the certain operating point and as you have oscillations, as you go away from that operating point, the value of g m tends to reduce.

So, we would like to have a sufficiently large g m so that, oscillations will starts and will attain a certain amplitude and it also for reliable start up. We know that, first of all, the value of R is not know exactly and this value of g m also varies with process and temperature and so on. With all those variations, the circuits should behave like an oscillator that is, if you set it up with an operating point and apply a small disturbance, you should have growing oscillations. So, typically you make the negative conductance, may be let say twice or something like that compare to the positive conductance, to have a reliable start up. And so that, the oscillation reaches the saturation value of the amplifier, in this case the trans conductor.

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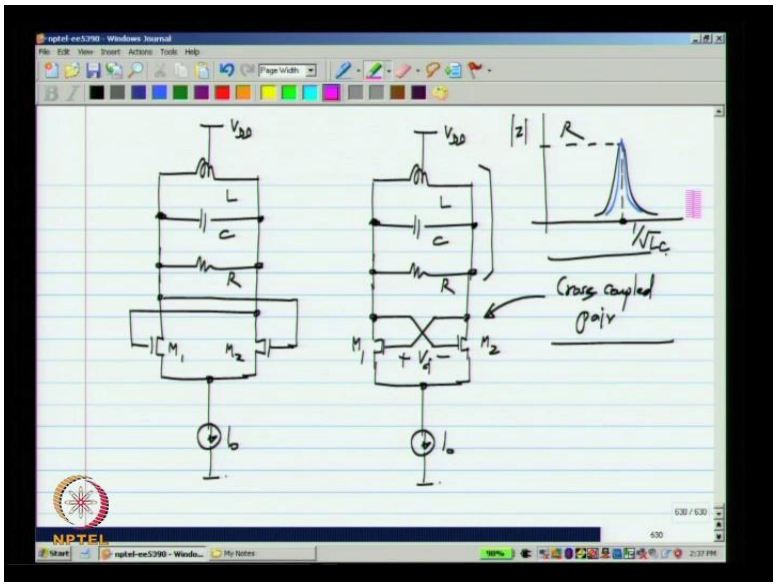

This can be realized using a differential pair, there are many options, but I will draw L C and R like this and I need to use a differential pair M 1 M 2, which is connected in positive feedback. And the drains of these have to be biased at some high voltage so that, they remain in saturation and that is most conveniently done by using a center tap inductor and connecting this to V D D. So, because of this, now the operating point here and there will be both V D D and very frequently, the topology is drawn with the transistors facing the other way.

So, this is the cross coupled pair and this is the lossy L C tank and we have a certain tail current I naught. So, if you assume that, let say somehow it starts of with the slight asymmetry with this voltage being slightly higher than that one. What happens is, you have this voltage is higher, so the in current M 2 will be higher than the current in M 1, so that will pull these node further lower. So, the current in this will be further lower and so on, so there is positive feedback and the oscillation will start.

Another way to evaluate it is, assume that the circuit is at operating point that is, both the drains are exactly at V D D. In that case, you evaluate the small signals equivalent circuits, what you will see is exactly what we had earlier, a parallel combination of L C, a positive conductance and the negative conductance that exceeds the positive conductance. Now, if there is the small disturbance, you will see that, the natural response of the such a circuits is exponentially increasing sinusoid.

So, the sinusoid will eventually increase and reach the swing limits of the amplifier, now what will be the amplitude of the signal that we get from an oscillator like this, that can be evaluated very easy by making some assumptions. Now, we will first see that, this is the differential pair M 1 M 2 and if the differential voltage sufficiently large, so let say, if the differential voltage in this directions V d is sufficiently large, all of this I naught will go through M 1 and nothing will go through M 2.

And similarly, if V d is sufficiently large in negative, all of the current will go through M 2 and nothing will go through M 1. Now, this V d is nothing but, the voltage across the capacitor, the voltage across the design in tank. We will assume that, the amplitude of this is so large that, if V d is positive, it is large enough to divert all the current I naught through M 1 and if V d is negative, all of the current is diverted through M 2. We will also assume that, the quality factor of this is very high that means that, you know what the impedance of parallel L C tank looks like.

It has a peak at the resonant frequency, which is 1 over square root L C and the peak value will be nothing but, R. So, what it mean is, if you inject currents at different frequencies then, you will have the maximum amplitude of the voltage at the resonance frequency. So, we will take this to the extreme and say that, across this L C tank, there will be only a sinusoid at the resonant frequency, no other frequencies will be present to the significant extent. That is, we know that, if the quality factor is larger, this becomes shaper and shaper. We will assume that, the voltages across this is a perfect sinusoid of this frequency. In reality, there will be harmonics, but we can ignore this strength of those harmonics if the quality factor is sufficiently high.

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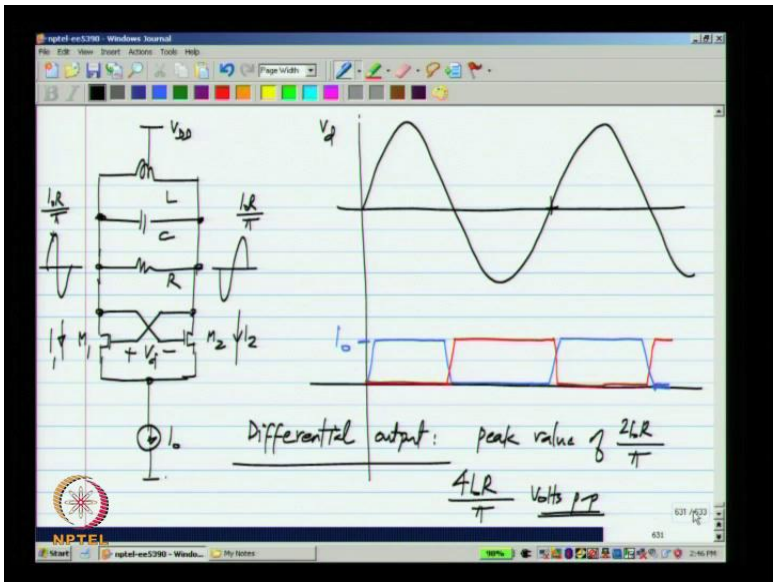

Now, with these assumptions, let me plot V d, which is the difference voltage like that and let say, that is a sinusoid at the resonance frequency. That is because, this high quality factor L C tank will not allow any other waveform to exist across it and this is the oscillation that we would expect from a loss less L C tank. Now, what happens to the currents, let me call the drain current of M 1 as I 1 and drain current of M 2 as I 2. The drain current of M 1, like I said when V d is very small, actually the drain current of I 1 would be proportional to V d and so on.

But, we will assume that, it simply very quickly reaches I naught and then, falls back to 0. If V d is positive, I 1 will reach I naught and if V d is negative, it will be 0, in reality it will be a little smother than this, but this is the reasonable enough assumption for calculating the amplifier. And similarly, the current I 2 will do the opposite, it will be complimentary to this. So, with this simplifying assumption, it becomes very easy to calculate the amplitude of the oscillation across this L C tank. That is because, now all we have is passive L C R network driven by this current pulses.

So, this entire thing here at the bottom can be replaced with this blue current like that and the red current like that. The blue and red wave forms are given here and how do we calculate the amplitude, again a very convenient way is to split L C and R into two parts, L by 2, L by 2, 2 C, 2 C and R by 2, R by 2 and ground the central points, this is V D D, which is same as small signals grounds. Now, this is the reasonable thing provided that,

the waveform here and the waveform there are anti symmetric and that turns out to be the case in this particular circuit, so you can analyze this.

Now, the advantage of this is that, we have two separates circuits, this blue current source driving left side of the circuit and the red current source driving the right side of the circuits. And you see that, the parallel L C R tanks on each side have the same resonance frequency and same quality factor as the original L C R circuit, it is just that the impedance level is scaled down by half. So now, how do we calculate the amplitudes, this is the square wave, I naught is the square wave and across the L C tank, we will assume that, we will have a sine wave.

That is because, the square wave will have the fundamental sinusoid and it is harmonics, but the quality factor of the tank is high enough, that you only have the fundamental and nothing of the harmonics. So, the voltage across this V 1, even it would be a sinusoid in phase with the square wave current that is injected into it, because at the fundamental frequency, these two reactants is cancel out each other and we have only a resistance and it offers no phase shift.

And how much is that current, that current is nothing but, the fundamental component of the square wave and the peak value of that is given by 2 I naught by pi. The peak to peak value of the square wave current is I naught and the peak to peak value of the sine wave current will be 4 by pi times that. You can remember the results on Fourier series that you would have studied earlier, similarly on the other side, this I naught which is the square wave, will cause a voltages across this, which is a sinusoid.

That is because, again this I naught will have the square wave fundamental and it is harmonics and all the harmonics are sorted out by the capacitor. And we will have only the sinusoid across this resistor V 2 and what will V 2 look likes, V 2 will be another sine wave, which is in phase with the red square wave. So, this is V 2 and that is V 1 and the total voltage across the tank is V 1 minus V 2 and that will be simply a sinusoid of twice the amplitude.

V 2 will also have the same amplitude, the current in this will have the amplitude 2 I naught by pi, amplitude of V 1 will be the fundamental components of the current, which is flowing through the resistor times the value of the resistor, which is 2 I naught by pi times R by 2. And V 2 will have exactly the same amplitude, 2 I naught by pi times R by

2 and V 1 minus V 2 will have an amplitude 2 I naught R divided by pi. So, what happens is, on each side, we will have a sinusoid, the two sinusoids will be out of phase of each other, 180 degree out of phase of each other.

And the amplitude of that will be I naught R by pi and the amplitude of this also will be I naught R by pi. And the differential output will have a peak value of 2 I naught R by pi, where I naught is the tail current and R is the equivalent parallel resistance that represents the loss of the entire L C tank. When reality, because the way forms smoother, it may be slightly less than this, but this is the close enough approximation, when the quality factor of the L C tank circuit is very high or sometimes it is common to give the peak to peak value.

So, this is how the cross coupled L C oscillator works and it gives some amplitude, so based on the L C that you have, you calculate the loss R. And based on the amplitude that you want, you choose the tail current I naught and based on the g m that you need to have, which has to be larger than the positive conductance, you choose the sizes of the transistors.

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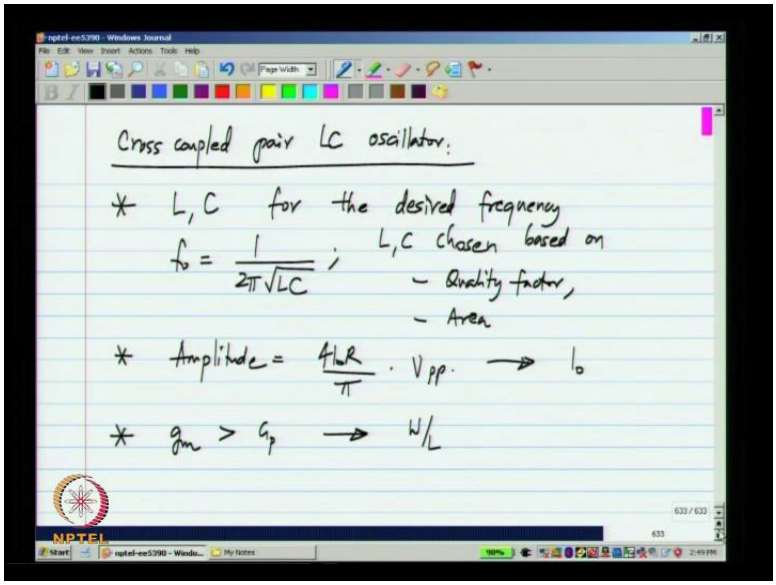

So, you choose a certain value of L and C for the desired frequency, now given the frequency, only the product of L C is constrained. You can choose different values of L and C, f naught will be 1 over 2 pi square root L C, so it only influence the product. But, how do you choose the value of L and C separately, choose it based on the quality factor,

area and so on. So, if you try to realize a very large L, you run into difficulties, you may not be able to realize with a high quality factor.

And also what we have not discussed is that, every inductor comes with it is own capacitance, the self capacitance, the patristic capacitance between different parts of the inductor and that will limit the frequency, at which the inductor can be used. So, if you go to higher frequencies, you can only use a smaller inductor. And also if you use a larger inductor, you end up using a larger area. In fact, inductor are the some of the biggest components on a integrated circuit.

So, based on that you have to choose it, again if you choose a very small inductor, you may again run into difficulties with quality factors and so on. So, based on the process that you have and the varieties of inductor available, you choose something that gives you high enough quality factor and based on that, you can choose the capacitance value. And the amplitude is 4 I naught R by pi, volts peak to peak and this will a give you roughly the value of I naught that you should use.

And finally, the values of g m must be greater than G P, sufficiently greater than G P for reliable start of and this gives you the size of transistor that you must use. Now, so far what you have is an oscillator, it is not yet a voltage oscillator, it just fixed frequency oscillator. Now, a very common way of varying the frequency of an L C oscillator is to vary the C. Of course, the frequency depends on L and C, you have to vary one of them, but it turns out varying L is too difficult and you have to vary the value of the capacitance C. And there are these devices which are varactor devices, which are either reverse bias diodes or MOS transistors, which realize a variable capacitance depending on some voltage.

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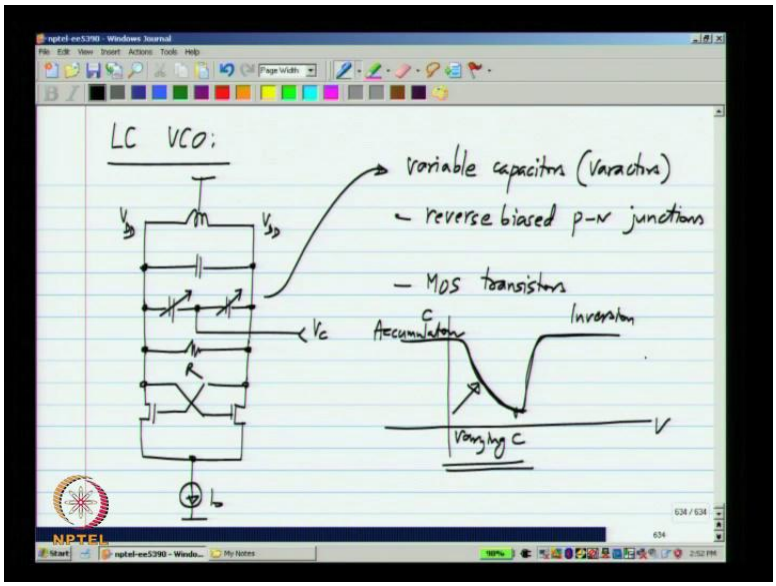

So, using those things, you will be able to make a variable capacitor, so if you connect the variables capacitor then, the oscillation frequency becomes variable with the capacitance value. You may have a fixed capacitance here, a portion of the capacitance which is fixed and you will have some portion that is variable. And for symmetry, you would always connected like this, you will have this R, which is not something that you connect, but simply represent the loss of all of the components you have and you have the cross coupled pair.

And we know that, the operating point here will be V D D and V D D, because of the inductor, so you connect this to some control voltage. So, across these capacitors, you will have V D D minus V c and it is a capacitance is a function of the d c voltage across it, you can vary the capacitance value. So, these variable capacitors basically known as varactors and they can be realized using reverse biased P N junctions. You know that, the reverse biased P N junction has a junction capacitance and it varies with the reverse biased voltage.

The larger the reverse biased, the smaller the capacitance, that is because the depletion region with goes on increasing and you have a smaller capacitance. And you can also realize it using MOS transistor and a MOS transistor, it has a C V curve, we want go into details of the this C verses V curve, which does something of that sort. This is inversion, this is accumulation and in this, you will have region where C is varying.

So, by using a MOS transistor in the appropriate region, you will be able to realize the variable capacitor, which basically behaves in a similar way to the P N junction capacitor, except that with the small voltages that we have now. A MOS accumulation capacitor is a better choice than a P N junction for realizing a Varactor. Now, again we would not into details of this, there are many variants of this one, in particular we could use a MOS transistor as it is that is, N MOS transistor or a P MOS transistor in n well. It turns out that, if you try to make an N MOS like structure inside an N well, that gives you the best choice for making varactors. So, most frequently these days, varactors have done by using N MOS transistor, it is not really transistor, basically N MOS structure in an n well.

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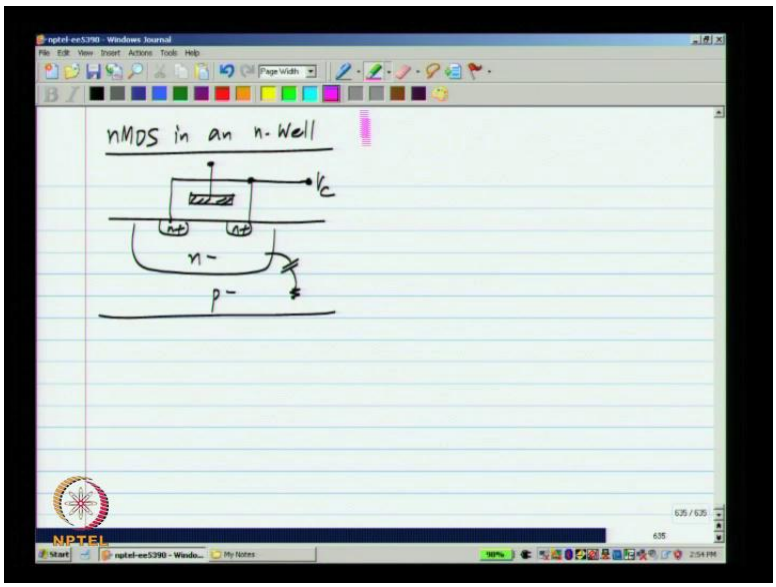

This is one of the terminal and this part is the other terminal and this part also has a large capacitance due to the capacitance between the n well and the P substrate. So, you try to connect these two voltage, which does not you have any signal on it that is, if this note should to be connected to be C in the oscillator that we have. We have a high frequency signals here and in this V c is d c voltage, so you connect these two part that has the d c voltage.

Now, there are many optimizations here in the lay out and so on, you can consult the literature for all of those things. We will very quickly go through other variants of the same oscillator, first of all there is the question of, whether to use P MOS or N MOS. We

have not discuss the phase noise of this oscillator at all, the phase noise of this comes from the current noise of the differential pair as well as the current noise of the tail current source.

Now, the differential pair contributes noise that is, very obvious, because it simply is driving the L C tank. The effect of tail current noise in the output is the very complicated, again you can consult the literature for it. Now, while optimizing this, people are come up with different topologies, which work well. But finally, you had to go to the simulator, simulate the phase noise and make sure that, it means all your requirements.

Now, first of all you can choose either an N MOS or P MOS transistor for the oscillator, as the trade of is as usual. N MOS will give you higher g m for the given current, whereas P MOS, it will be lower. And also the N MOS transistor will usually tend to have higher flicker noise, whereas P MOS has a lower flicker noise. These are some of the aspects that you have to consider before choosing N MOS or P MOS L C oscillator.

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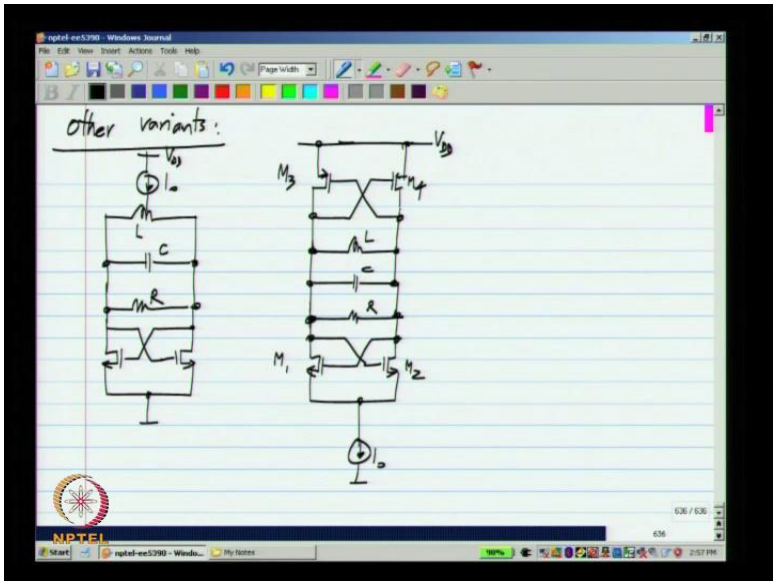

If you look at other variants, so one possibility is to use a current source on top, instead and have a cross coupled pair of common source amplifier and another possibility would be to have both N MOS and P MOS switching. We have P MOS cross coupled pair on top and the L C part of it, as usual I am showing R, because it represent loss, not that we connect the resistance there, I naught. So, here we have P MOS transistor in addition to

the N MOS stuff, this adds to the negative conductance and can give you a better performance as well, that is another possibility.

And sometimes these currents are removed entirely, now that is not a very good idea, because then the circuits becomes sensitive to the power supply. So, that is not the good idea, but sometimes you can remove the current source and operate it with a voltage regulator. So, that is the endless variety and you can consult many references in the literature for variants of V c os.

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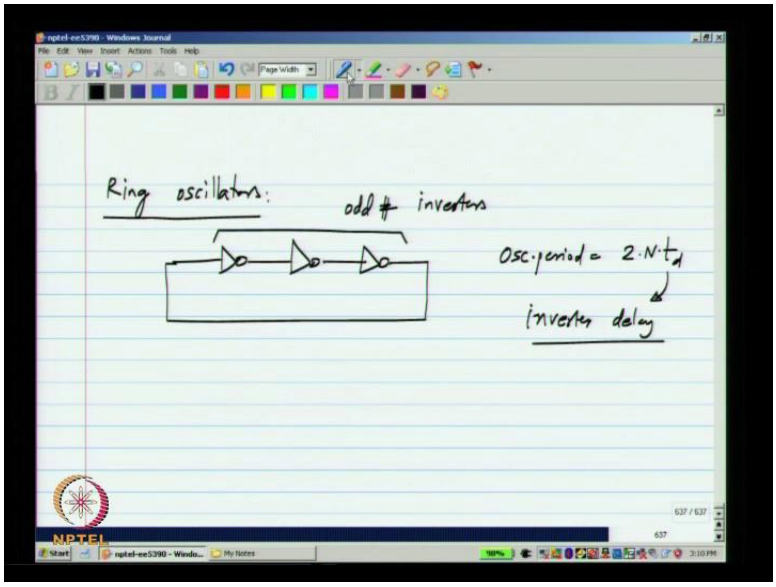

We have looked at L C oscillators, now we will look at ring oscillator which are another popular choice for oscillators on integrated circuits. Ring oscillator very simple, it is just an oscillator made with a chain of inverters, which acts as a delay line and if you have single headed inverter, you choose an odd number of inverters so that, you have the negative polarity. And then, you connected up so that, it is in negative feedback for d c and it oscillates and the oscillation period is 2 times N times t d, where t d is delay of each inverter.

So, this is a very simple thing, all that happens is that, if you apply pulse here, this should be inverted, but it will comes after some delay and this will rise after further more delay and so on. So, this gives you a sustained oscillation, now you need at least three inverters, if you have a fully differential structure, you could try to make it with two inverters, but sometimes it may not oscillate. Now, again our goal here is not to do

analysis of these inverters and their oscillations and so on. So, that can be done and you can refer to literature for that one, here I only show you the couple of variants of the ring oscillator.

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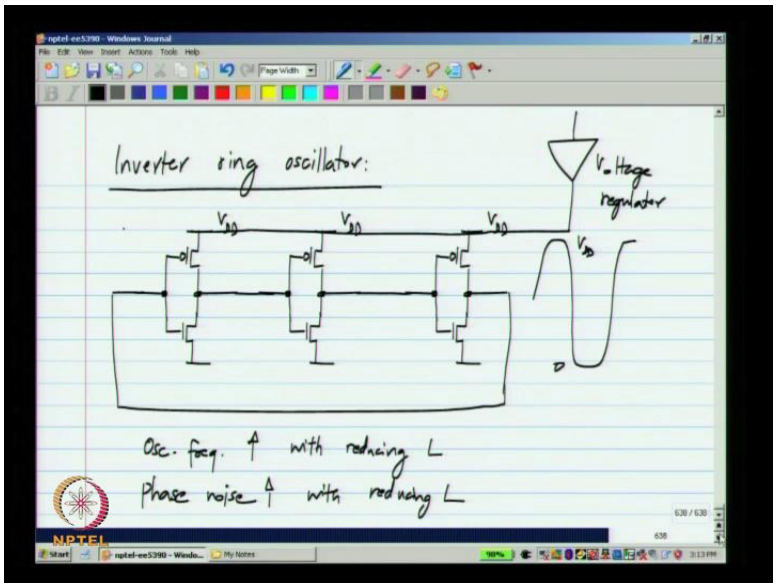

First is the standard inverter ring oscillator and this is simply a chain of a CMOS inverters in a ring. So, you connected up like that, you need odd number of stages as shown 3, but you could have lot more. And you basically choose the size of these transistor such that, you get the desired frequency of oscillation. If you make the transistor are shorter and shorter, the oscillation frequency increases, this is because the capacitance here decreases and the current driving increases, so that makes it faster.

But, also the phase noise also tends to increase with reducing L, this is because the flicker noise becomes more and more important as the L becomes smaller and smaller, so that is all that is there to it. And how do we control the frequency of this, in fact in this, there is only one control, which is the supply voltage itself and you can control the frequency of this using the supply voltage. In fact, the frequency of the ring oscillator is very very sensitive to the supply voltage, so you can cover a very wide frequency range by varying the supply of the ring oscillator.

So, the way this is usually used is by using a voltage regulator, which is controlled so that, you can control this voltage and control the frequency. And if you use large number of stages or even with three stages, the waveform here will be some square wave forms

that goes all the way from 0 to V D D. So, this is the nice way of generating this square waves, whose frequency can be varied by varying the V D D. Now, one of the problems with this is that, it is extremely sensitive to the supply.

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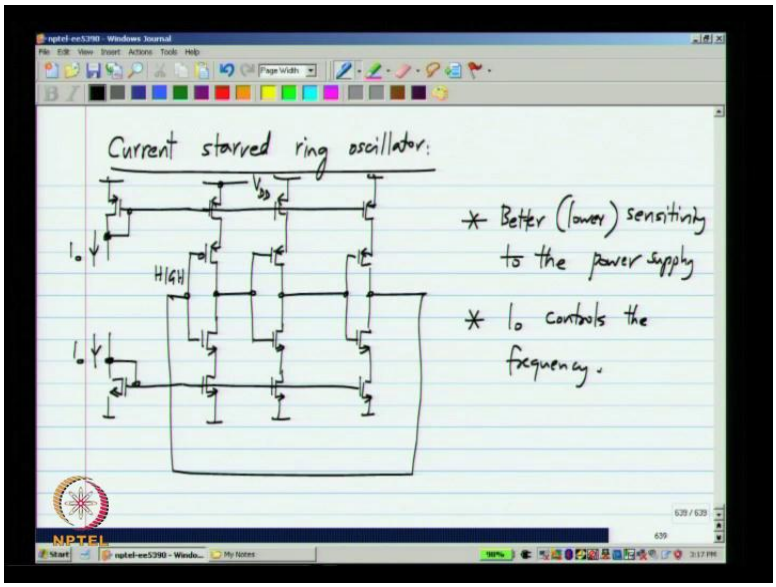

Now, to improve that, one of the variants of ring regulator is what is known as a current starred oscillator. The way this is made is the exactly same way as the inverter base ring oscillators except that, you try to regulate the charging and discharging currents. Now, this is the cell that is used in a current starring ring oscillator, where this is biased with the current mirror. So, let me call this some I naught and this will also be biased with I naught.

Now, compare these two, just the inverters, what happen is, you have some patristic capacitance of the output and if the input is tried to V D D. Let say this is high, what happens is, the P MOS transistor is off and the N MOS transistor is on and the current here depends very strongly on the high level that is, the V g s of the N MOS transistor. So, the discharging of this is what determine the delay and in the other polarity, when this is low, the charging of it through the P MOS and both are very sensitive to the supply voltage.

Now, that is sometime undesirable, now what happens instead in this case is that, you have a capacitor C and let say, this is tied to high level, may be V D D. Then, this P MOS transistor is off and the N MOS is on, but the actual discharging current is

determined by this current source. Assuming that this is in saturation, now it turns out that, this cannot be in saturation all the time, but in some crucial part of the period, it will be saturation.

So, the discharging current is regulated lot more in this compare to that one, so this oscillator is less sensitive to the power supply, compare to that one. So, you use multiple cells of the sort, so this is the three stage current starring oscillator. And the main advantage of this is that, it has better, it is lower sensitivity to the power supply and the control of frequency is through the current I naught.

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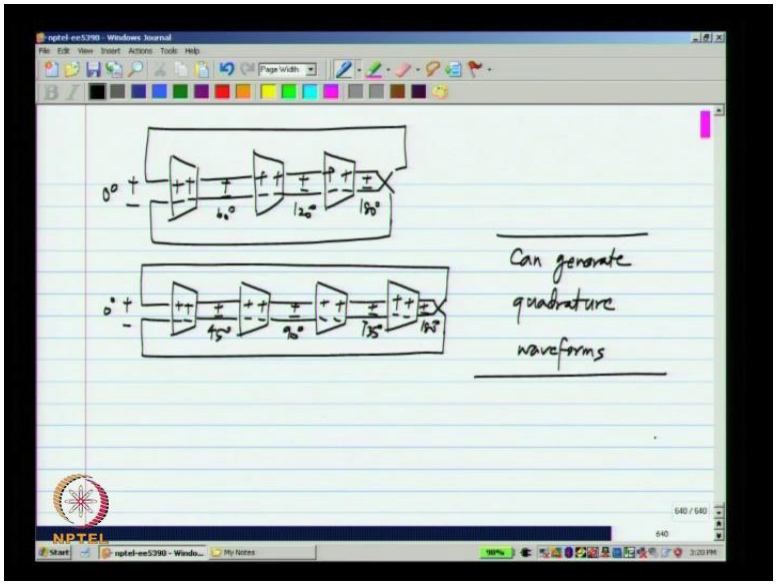

And another variant of the ring oscillator is differential version that is, you use differential trans conductors or difference amplifier and number of them in cascade. So, this is the three stage differential ring oscillator, with the differential version, you are not restricted to odd number of stages. The region we are restricted to odd number of stages is because, we had to have polarity inversion. So, we have to have an odd number of stages or number of inverters when we are working with single ended cells.

When we have differential cells, inversion can be simply accomplish by crossing a wire, so we are not restricted to an odd number of stages. We could also have four stages, now the advantage of something like this is that, the net phase shifted from here to there is 180 degrees. So, let say if the wave form of this is referred to as 0 degrees, the wave

form here will be 180 degrees with this being 120 degrees and this being 60 degrees with respect to the original.

Now, here with four stages what will have is, we have 0 degrees, 45 degrees, 90 degrees, 135 degrees and 180 degrees and this inversion by crossing the wire provides another 180 degrees and the loop is complete. When you are required to generate oscillations with multiple phases, so one of the popular requirements is to have quadrature that is, you have 0 and 90 degree also. So, in such cases, having an odd or even number of stages quite useful. So, with an even number of stages, you can generate quadrature wave forms, so this is something that can be done.

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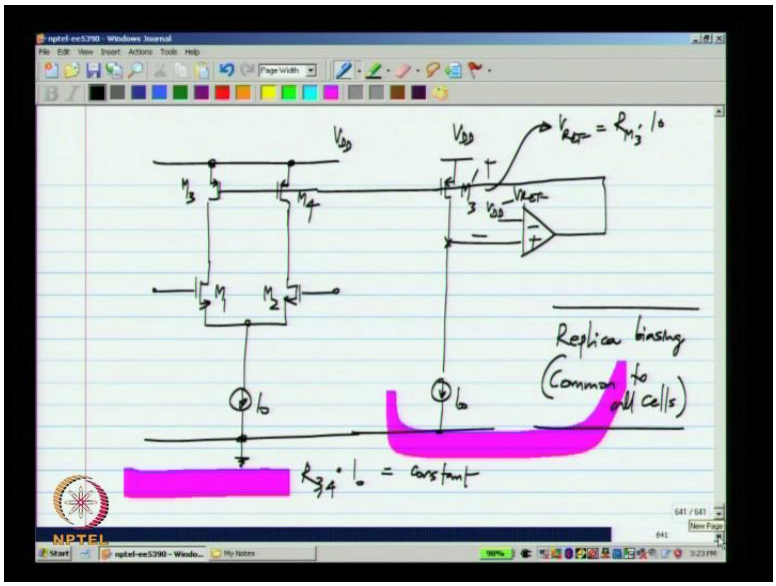

Now, how do we implement something like this, each of these cells is typically a differential pair divided by P MOS transistors in triode region. And we could use resistors then, the problem is that, the frequency is varied by varying the current I naught, which in turns varies the trans conductance of transistor M 1 and M 2. But, if the current I naught is varied, the amplitude of the output wave form will also vary and if I naught becomes too small, it may not oscillated all, it may not able to switch the next stage and if I naught becomes very large, this whole thing can go into triode region.

So, what is done is, to use a P MOS transistor in triode and the biased of the P MOS transistor is adjusted such that, let me call this M 3 and M 4. The resistance of M 3 and M 4 times I naught is some constant and this can be set using a negative feedback. We

use the replica of M 3 and M 4, let me call it m 3 4, may be M 3 prime and I can have this current I naught and the replica that over here. And what I can do is, compare this with some desired voltage, this is V D D and across this, I wanted to be some constant that is, V ref must be equal to the resistance of M 3 prime times I naught.

So, to this I apply V D D minus V ref and based on this error, I integrate the error and control this one. I have to control in a direction that has to minimize the error and that turns out to be, if I do this one. So now, what happens is, as I naught is varied, the resistances also vary, the product is the constant. So, the output wave forms will have a constant amplitude and it will be able to drive the following stage. So, with this, you can vary I naught to vary the output frequency, but keep the amplitudes constant.

Now, this is one cell, this part which is the replica biasing part, this is common to all cells, so it is possible to make a differential V c o using a technique types. So, that is a very brief overview of voltage controlled oscillators, we can have a L C oscillators, whose frequency is varied by using a varactor or a voltage variable capacitor. And we can have ring oscillators, so frequencies can be varied by either varying the supply voltage or some bias current.

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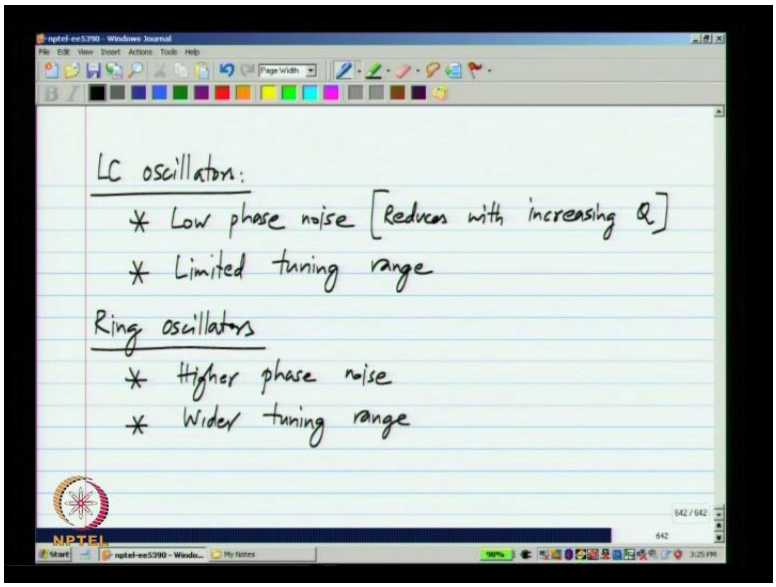

Now, just a quick comparison, L C oscillators will have a lower phase noise compared to ring oscillators. In fact, the higher the quality factor of the passive components of L and C, the lower the phase noise. But, it usually also has a rather limited tuning range, this is

because the variable capacitor cannot be varied over the large range. So, many large things are used like using banks of capacitors for tuning over a wider range, but in general, the tuning range is limited compared to ring oscillators.

And if you look at ring oscillators, we have a higher phase noise, but have usually a much wider tuning range. And there is a number of variants, which give you either a superior supply rejections or a higher operating frequency and so on. Now, with any oscillator, you would have to go the simulator and simulates it is phase noise, make sure that it is satisfactory. Similarly, oscillates it is amplitude and make sure that, it can drive the following stages and so on.

So, there we come to the end of an important topic of this course, which is basically frequency generation using phase lock loops and oscillator, which are a component of the phase lock loop. We have gone through a significant details of the phase lock loop as a system, but not at the circuit level. And I have not gone through the details of making the program over frequency divider, they are digital divider blocks and a details of that can be found in the literature.

Thank you, I will see you in the next lecture.