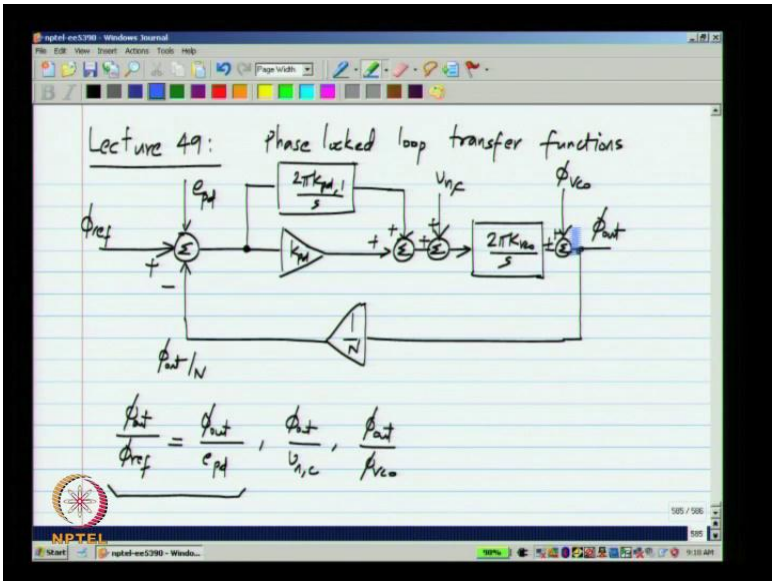
**Analog Integrated Circuit Design**
**Prof. Nagendra Krishnapura**
**Department of Electrical Engineering**
**Indian institute of Technology, Madras**

**Lecture No - 49**
**Type II PLL Transfer Functions; Implementation**

Hello and welcome to lecture 49 of analog integrated circuit design. We have now developed the type two phase locked loop which eliminates the problem of reference phase through. And we were evaluating the transfer functions between different points of the phase lock loop and the output. That is errors could be introduced at different points in the phase locked loop and we evaluate the transfer functions from those points to the output.

(Refer Slide Time: 00:33)



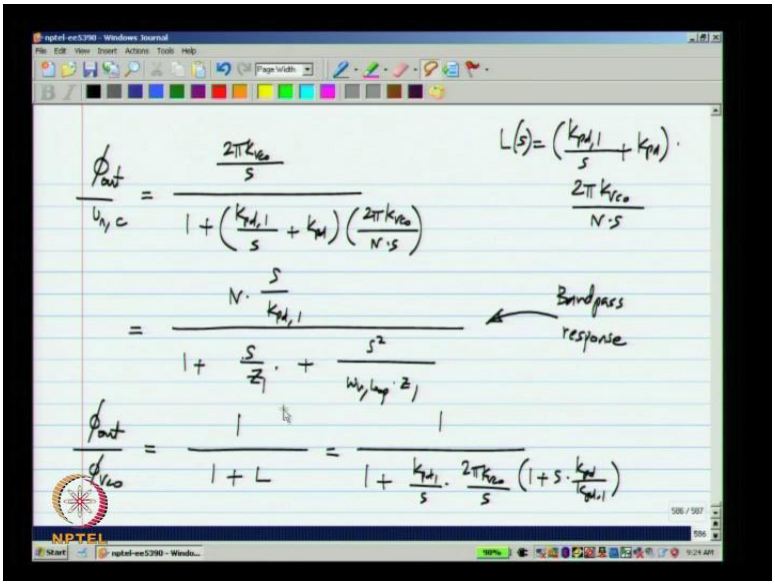

The phase module of the type two loop for incremental phases is like this. As I mentioned first of all we are interested in the transfer function between phi ref and phi out and also many errors of the phase detectors can be modular. And error that is injected over here that is let is the error e due to the phase detector. And some errors can be more or less being added at the control voltage. This will have dimensions of phase basically dimension less and this will have dimensions of voltage.

And finally the V co will have some inherent noise in its output phase which we will discuss later. But, for now we can imagine that they are added at the output of the V co.

So, we are interested in calculating phi out by phi ref phi out by e pd all in the Laplace domain and phi out by V n, c phi out by phi V co and so on. This we have already calculated in fact they are equal to each other they are added at the same point. Other things we will calculate by the way this e pd also could represent errors due to the frequency divider referred to its output.

The output error of the frequency divider will get added here the only difference will be the sign of the error. But, that usually irrelevant let me write down the loop gain function it is the part due to the phase detector times. The part due to the V co and the frequency divider and phi out by V n, c as usual is this forward path divided by the loop gain plus 1.

(Refer Slide Time: 04:02)




And this will come out to be the denominator will be the same as before and the numerator will be it will come out to be n times s by k p d, I divided by this entire number. By the way these transfer functions will be dimension less this also will be dimension less. And this should have dimensions of one over volts obviously because the output is phase and the input is a voltage.

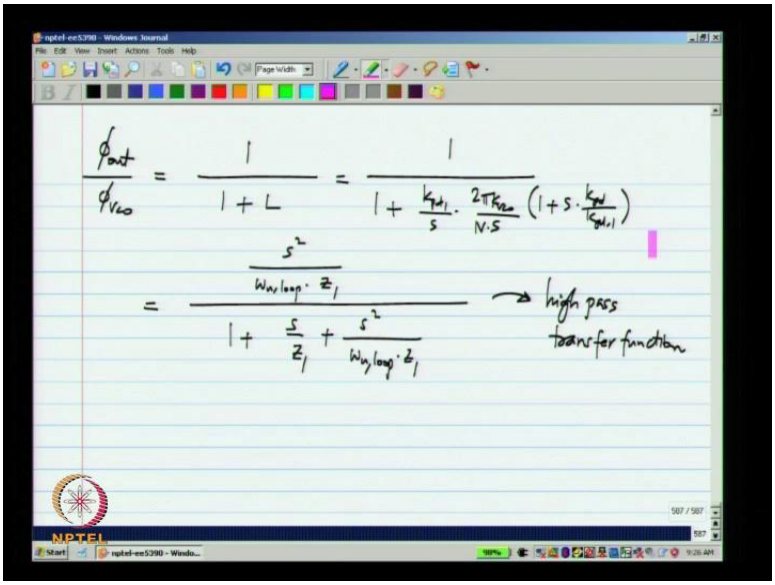
So, this is the transfer function from the control voltage any noise in the control voltage to the output phase and this you see as s in the numerator and second order denominator. So, this will be some sort of band pass response and the intuitive reason to the band pass response is as follows. If you inject something from here at very high frequencies the

loop gain is negligible and we have only the forward path which is an integrator. So, at high frequencies it just goes down to 0 at very low frequencies.

Where the loop gain is very high what happens is this is preceded by a very high loop gain. So, again the loop will not respond to the errors injected over here we know that the error injected over here will get suppressed by 1 plus loop gain. And you know that at very low frequencies this is preceded by a very high gain, so it will get suppressed. So, at very high and very low frequencies it is suppressed at some intermediate frequencies it will peak, so there will be a band pass transfer function.

Whereas from here to the output it will be a low pass transfer function at low frequencies it will be a constant because of the very high loop gain. And at high frequencies it will drop off because of the attenuation of the forward path. And finally phi out by phi V co will be 1 by 1 plus L which can be written as 1 plus k pd,I by s 2 pi k V co by s 1 plus s k pd by k p d, I.

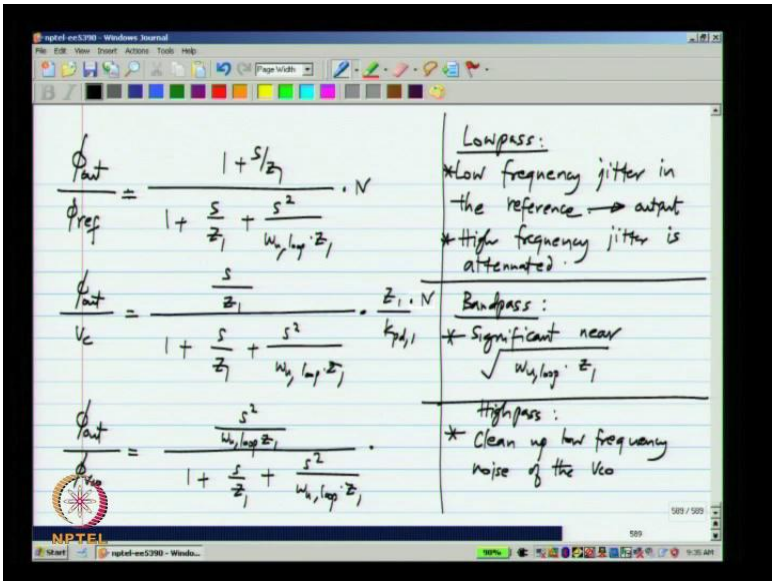
(Refer Slide Time: 07:49)




And this can be written with the same denominator different transfer functions with the same system will have the same denominator. And in the numerator we will have sorry there should be a n here in the numerator we will have, so now this is a high pass transfer function. So, again the reason for this is that this is preceded by a very high loop gain at low frequencies. So, it will be strongly suppressed at low frequencies and at very high frequencies where the loop gain becomes negligible this entire loop can be eliminated.

And you simply have phi V co going directly to phi out, so you expect that at high frequencies the transfer function will be one and that is exactly what you see over here.

(Refer Slide Time: 09:33)




So, if we put down all the transfer functions together phi out by phi ref is that and phi out by V c is and phi out by phi V co is that. Now while manipulating the algebra I am not shown every step of the algebra while deriving these expressions I am assuming that you can do this for yourselves. This is just second order transfer function manipulation all I have defined is this constants whom I have looped and z 1. So, that the transfer functions can be conveniently written down. So, I suggest that as usual you go through the derivation yourself and make sure that the answer you get matches with what I have shown here.

This what I will do now is to just take this n outside and this I will show as that one and this number is nothing but 1 over k pd and this I will leave as it is. Now, I am doing this just, so that we can compare the shapes without worrying about the exact magnitudes. So, what I will do is plot only these parts and for this one and this one they will be scaled up by some appropriate fraction. So, if I plot the magnitude response of these transfer functions what happens is this one you can see that it starts from 0 db only this part of it.

It starts with 0 db DC gain and then it is a low pass transfer function. So, it will do something of this sort it could do something like that. And it could also do something like that sorry I missed out the 0 in this transfer function. Depending on the location of

the 0 it could have some peaking it could do either this or something like that if you look at this part of it what happens is. It will tend to do something of that sort this is not the scale by the way and the last one.

The transfer function from the V co noise to the output will do something of that sort these are the transfer functions. And they are scaled by this appropriate factors I did not show the scaling factor. So, that I could plot all of them on the same dimensionless transfer function plot they will be the shapes and they will scaled up by the appropriate factors. Now, how would you design a PLL different parameters of a PLL.

What you have to do is just like what would do in an op amp or any other electronic circuit. There we had voltage noise and current noise and the output noise contribution was due to every noisy component in the circuit let us say mos transistors and resistors. You would calculate the transfer function from every moss transistor noise to the output noise every resistor noise to the output noise. And add up all the spectral densities to get the output here it is exactly the same thing first you have to determine what noise is contributed by different parts that is what is phi ref what is noise in V n,c.

And then what is the phase noise of the V co and these must be multiplied by the respective transfer functions. And you will get the output phase noise as some of these individual spectral densities and from that you can decide whether to optimize further. That is whether to reduce the contribution of some particular noise and that can be done either by reducing the noise source which usually implies an increase in the power dissipation or by manipulating the transfer function.

Now, we will not go in to great details of these calculations over here. But, once you understand the principles you will be able to do it yourself with some effort. So, phi out by phi ref is a low pass transfer function. So, that means that any phase noise or jitter in the reference at low frequencies it goes to the output and high frequency jitter is attenuated. Now, the PLL is in fact used for this kind of functionality sometimes you would like to attenuate the jitter of some signal.

You want clean up some signal in that case you use it as a low pass filter for the jitter let us say you have some source and you want to reduce its jitter. The PLL acts like a low pass filter for its jitter, so that is one application of the PLL alternatively. Let us say you have some jittery source and you want to be able to have another source which replicates

that, that is you want to able to follow the jitter at some frequencies. So, then you can adjust the parameters of your circuit, so that within the desired bandwidth the jitter of the jitter of the references followed.

Now, this kind of thing happens in clock and data recovery circuits normally here the input is not a periodic signal. But, it will be some data which will have some jitter and you may actually want to follow the jitter, so that you can decode the data correctly. Now, on the other hand like the earlier application where you want to clean up the reference where you want to reduce the jitter then would try to reduce the bandwidth as much as possible. So, that you effectively have a low pass filter of very low bandwidth which removes most of the noise of the reference.

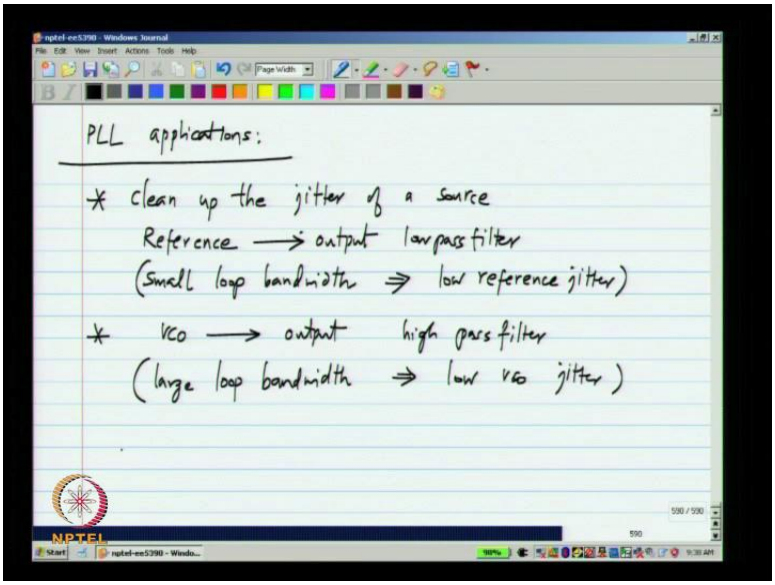
Now, as usual in any circuit let us say you make a filter the goal may be to reduce the noise from the input. Now, you also must make sure that the filter itself does not create too much noise. Now, in this case the noise in the control voltage and the noise of the V co are internal to the phase lock loop and they are something like the circuit noise the noise that is generated by the circuit. Now, these things you have to make sure that they are lower than a sufficient volume. And finally the V co noise goes to the output with a high pass transfer function and this is used to. In fact, clean up the low frequency noise of the V co.

Now, this is application that you have a variable frequency source like the V co. Now, its noise is too much you can clean it up within the PLL bandwidth that is beyond the PLL bandwidth beyond. The unit loop gain frequency of the PLL the V co noise comes straight to the output. But, within the bandwidth it gets significantly attenuated by the high loop gain that is present in the phase locked loop, so that is application. So, very frequently you have a noisy source like a voltage connected oscillator whose frequency is variable and you have a clean source like a crystal oscillator whose frequency is fixed.

So, what you can do is to realize the phase locked loop with the crystal oscillator as the input with a variable division module assigned. And V co in the phase locked loop what happens is within the loop bandwidth of this phase locked loop it will follow the crystal oscillator. That is the good reference which has very low jitter and outside the loop bandwidth it will follow the V co which has the poor jitter. So, within the V co

bandwidth you have cleaned up the jitter of the V co that is one of the ways in which the phase locked loop is most frequently used.

(Refer Slide Time: 20:00)




So, the reference output is low pass filter and a small loop bandwidth means that the contribution of the reference jitter to the output is small. But, V co to the output is a high pass filter and a large bandwidth implies a low V co phase noise that is low contribution of the V co phase noise to the output. So, in general what you would like is to have a low overall output noise and you would have to adjust the bandwidth accordingly. So, that the overall phase noise is low.

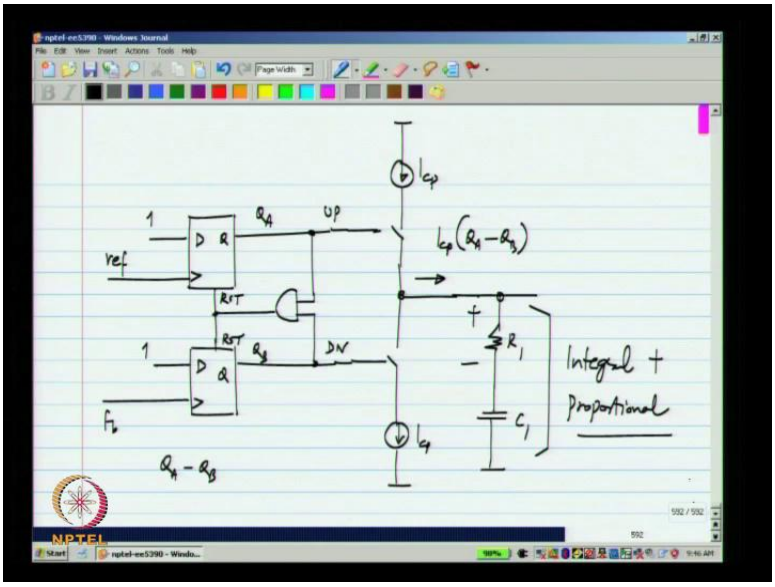
So, now we have looked at the type two PLL in some detail and we understand its workings that is we know the transfer functions between different parts the only confusing parts could be that. The transfer functions is between are between phases the output quantity is a phase. But, just like what we calculate it further for the reference feed through if you have some phase phi then what it really means is you have a periodic signal with that phase error. And for small values of phase error it is like having the ideal periodic signal plus a modulated sinusoid which is modulated by the phase error. So, whatever phase error is there will get translated to the frequency of the interest in this case n times f f.

So, essentially in addition to the impulse that represents the spectrum of an ideal periodic signal it will also have side bands which could consists of impulses if the error is

periodic it could consist of some continuous spectrum if the error is random. So, the bottom line is you will be able to calculate the output phase noise spectra from these transfer functions and understanding the noise sources spectral density.

Now, the thing we said earlier when we came to the type two phase locked loop was that there is no reference fore at all there is no reference feed through. Because the operating point phase difference between the reference and the feedback signals is 0 which means that the phase error is 0. Now, we have not yet looked at the complete implementation of the phase detector and the integral part of the phase detector. Look at the popular way in which the phase detector and the loop filter is implemented. And we will see that in some conditions there will be a reference feed through it will be much smaller than what we had in the type one loop what it is still there. And that has to be taken in to account while designing the PLL.

(Refer Slide Time: 23:48)



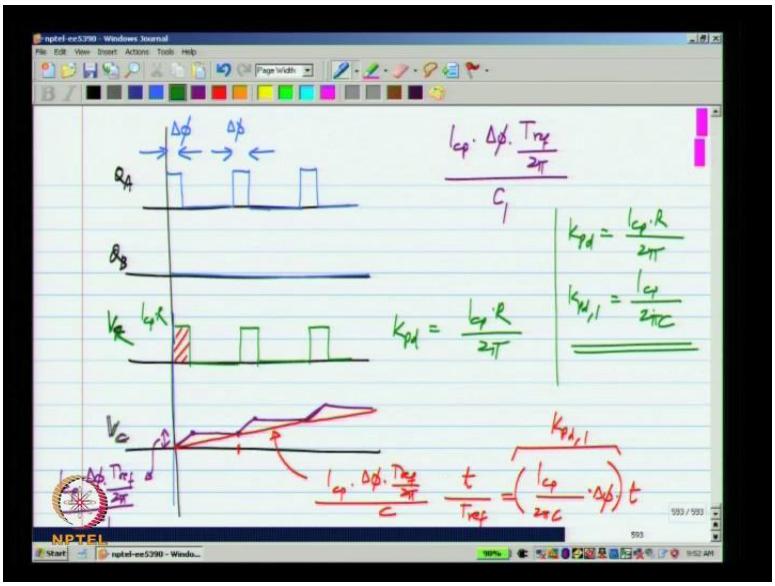

What we wanted was we have the reference and we have the feedback signal and we have these two parts this gives something proportional to the phase error. And this gives something that is related to the integral of the phase error over time and the sum of this is fed to the V co how do we implement this. We have already seen that the phase deduction itself can be implemented with these two flip flops the arrangement of two flip flops which respond to raising edges.

And both the flip flops are reset when these two signals go high. Now, what we need to do is if we look at the differences in the voltage between these two it will give you the proportional phase deduction. But, what we need is both the integral and the proportional together the sum of the two and the very need implementation of that which is very popularly used as well. So, what we do is this is the up and down or let say let me it call Q A and Q B and we saw that the average value of Q A minus Q B gives the phase error. But, because we want the integral and the proportional both we will not use the voltage signals directly what we do is.

Have current sources and switches like this by the way we had to take the difference between these two and also integrate the difference. This is the up switch and this is the down switch, now what happens is the current that is flowing here will be I cp times Q A minus Q B. That is if this is 1 and this is 0 the current I cp will flow that way if this is 0 and this is 1 minus I cp will flow this way or I cp will flow in the other direction. And if either both are 1 or both are 0 what happens is no current will flow that is exactly the kind of thing that you want. Now, we want something proportional to this and you get a voltage proportional to this one. The natural thing is to use a resistor and we also want something that is related to the integral to this. And to integrate a current we simply pass it through a capacitor, so this is a very compact and neat implementation of proportional plus integral phase detection.

Basically, we have these two current sources which are nominally identical and while operating these two switches we get a current here which is a current of the charge form I cp times current Q A minus Q B. And that is passed through a resistor to get the proportional output and a capacitor to get the integral output and simply by putting the two in series will get the integral plus proportional output. And this entire arrangement is called a charge pump because basically the current source will dump a certain amount of charge in a given period. And that is why it is called a charge pump this charge pump topology is very popularly used with phase locked loops. Now, we need to calculate the parameters of this phase locked loop what is the output voltage that we get here the voltage across the resistance will be.

(Refer Slide Time: 29:12)



So, first of all let us say Q A and Q B or signals like this is a case where references leading the feedback signal and Q A is high for a phase of delta phi and Q B is always 0. So, the voltage across the resistor would be would have the same form of Q A because Q A minus Q B is what we have and the amplitude of that will be I cp times R sorry this is the voltage across the resistor.

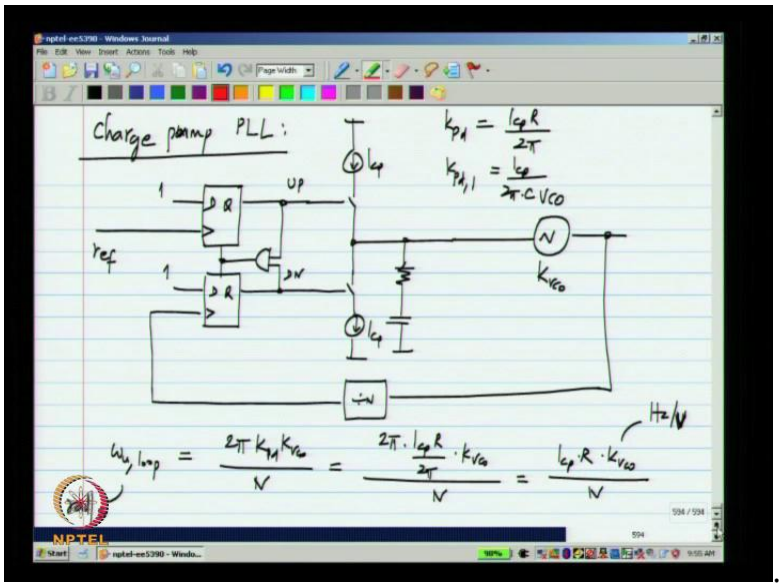
And voltage across the capacitor what will do what it will do is it will rise up by some amount. And how much is that that is related to the charge injected in to it which is I cp times delta phi T ref by 2 pi basically I cp times. This time duration and this time duration is delta phi by two pi times T ref. And that is the charge and that divided by C 1 is the incremental voltage. So, it will rise by some amount and that amount is I cp delta phi T ref by 2 pi by C 1.

And it will be constant over there because no current is being injected and then again it will rise by the same amount assuming delta phi is the same. I have assumed that the same phase difference is maintained and so on, so it will keep on doing that one. So, actually you see that for delta phi which is a constant we see the integral of a constant should be a ramp. But, this is not a ramp this is the ramp only in some average sense if you connect these starting and ending points at every period we will get something like this.

And slope of this will be nothing but the size of this step divided by the total time or the total phase which is 2 pi. Now, the voltage across the capacitor in some average sense will rise as a ramp. And the expressions for the ramp can be given by I cp delta phi T ref divided by 2 phi divided by C 1 that is the amount of rise in one cycle and one cycle is T ref and time is t.

So, if t equals to T ref it rises by one step like this two T ref it will by two steps and, so on. So, this can be written as I cp divided by two phi c times delta phi times t ok. So, this is the proportionality constant of integration and this will be K pd times I and K pd of course will be nothing but the average value of this which is I cp times R divided by 2 pi. So, this is what we will have and from this we can calculate the different parameters of the loop the bandwidth etc.

(Refer Slide Time: 33:49)

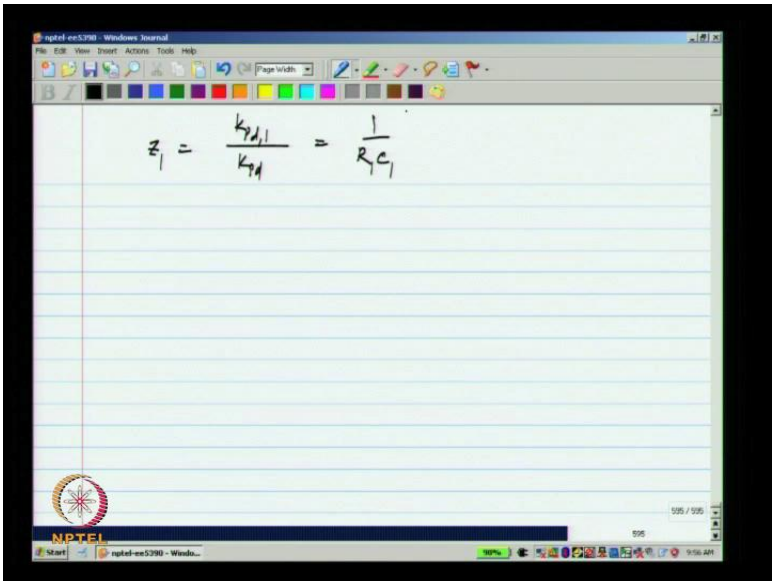



So, the charge pump PLL looks like this the reference signal can be reference signal aspired to one of the flip flops and this is the feedback signal and we have this current source and switch arrangement. And this resistance and capacitance implementing the proportional integral path the V co and the frequency divider. So, this is the charge pump PLL and the V co will have some gain k V co. And we already evaluated that with this arrangement the proportional path phase detector gain will be I cp times R divided by 2 pi and the integral path gain will be I cp divided by 2 pi times c.

So, we will have a phase locked loop whose unity loop gain frequency you know is 2 pi K pd K V co divided by n. And by substituting the value of K pd we get two phi I cp R divided by 2 pi times K V co divided by n this is I cp R K V co divided by n. And you can see that I cp r has dimensions of voltage K V co has dimensions of hertz per volts and omega loop is the frequency. So, it is dimensionally correct also one important thing do not get confused.

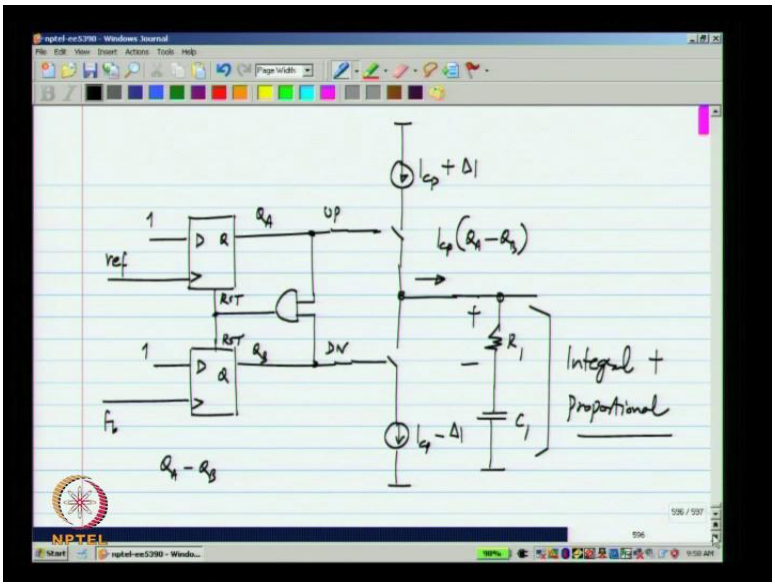
By this K V co here is in harts per volt whereas this is in radians per second and this is correct and it appears because the gain of the phase detector has 1 over 2 pi there and this 2 pi cancels with that two phi. So, if you want to calculate the unity loop gain frequency in harts this has to be further divided by 2 pi.

(Refer Slide Time: 36:44)




And the frequency of the 0 is K pd I divided by K pd which is nothing but 1 over R 1 C 1. So, if we call this R 1 and C 1 the 0 will be at 1 over R 1 C 1, now we already evaluated the constraints on the 0. And its location valid due to the unity loop gain frequency we can put those things in and then evaluate the constraints on I cp R and C 1 etcetera. Let us consider this three stage phase detector and charge pump once again.

(Refer Slide Time: 37:42)

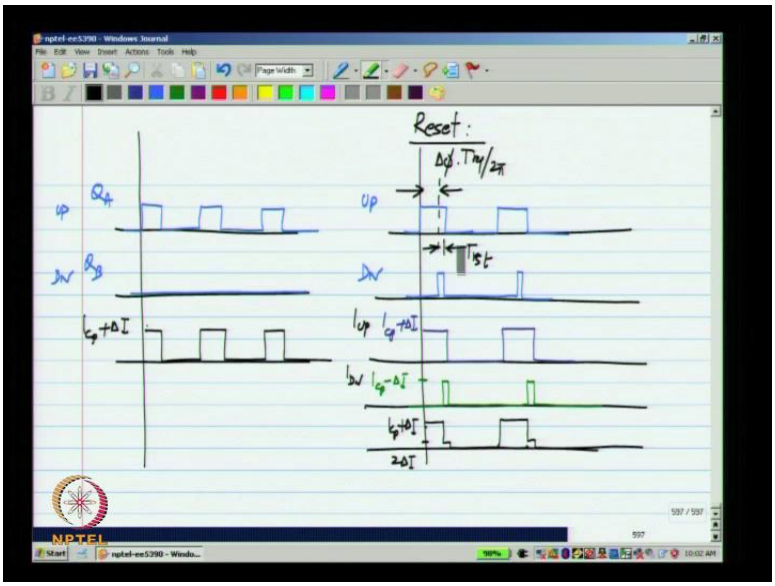



Ideally this current source will be exactly equal to that current source. Now, if we have that what happens is that if up and down are both one this will be exactly 0. In that case this will behave exactly as we predicted earlier. And the total charge that is coming out of this is proportional to the phase as I said earlier that is why this is called a charge pump.

Now, in reality what happens is these are two different current sources and they will be never exactly the same as each other we have already started mismatch in grid detail. There is systematic mismatch as well as random mismatch one of the problems is that I cp is a current source. That is something that is pushing out current and the lower I cp is a current sink which is something which is just pulling in current.

So, the upper source is realized by the p moss and lower source by n moss it is even harder to match this two very well. Now, given this there will be mismatch between the two current sources what happens because of mismatch let us take a look at it. So, in that case I will make this two slightly different from each other I will say I cp plus delta I and I cp minus delta I.

(Refer Slide Time: 39:04)




Again I will consider a case where the reference is leading the feedback signal. So, Q A will be like this and Q B will be continuously 0 or this will be the up signal and this will be the down signal. So, in this case again what we will get is that the output of the charge pump will be the upper current source modulated by this switch. So, it will be I cp plus delta I, so it looks like all that has happened is that the amount of charge from current is changed by a little bit. And that is not such a big deal that will change the loop parameter slightly the main point is if the phase difference between the reference and feedback is 0 the signal will also be 0.

Now, but there is another thing that comes in to picture in a real three state phase detector and that is the delay of the reset, now we have. So, far assumed that if Q A is high and the moment Q B goes high the reset will happen and both of the flip flops will reset instantaneously. But, in reality what happens is Q A goes high and Q B goes high only after certain delay will the reset be activated. So, in reality Q A and Q B or up and down signals do not look like this Q A goes high.

And after a while when the feedback signal arrives Q B goes high and they will be both high for a certain period and then come down and so on. Now, what happens in this particular case, so this part is delta phi times T ref by 2 pi and this part is the delay of the reset path. So, what ends up happening is that the upper current will be on for this duration and that will be I cp plus delta I and the lower current will be on for the other

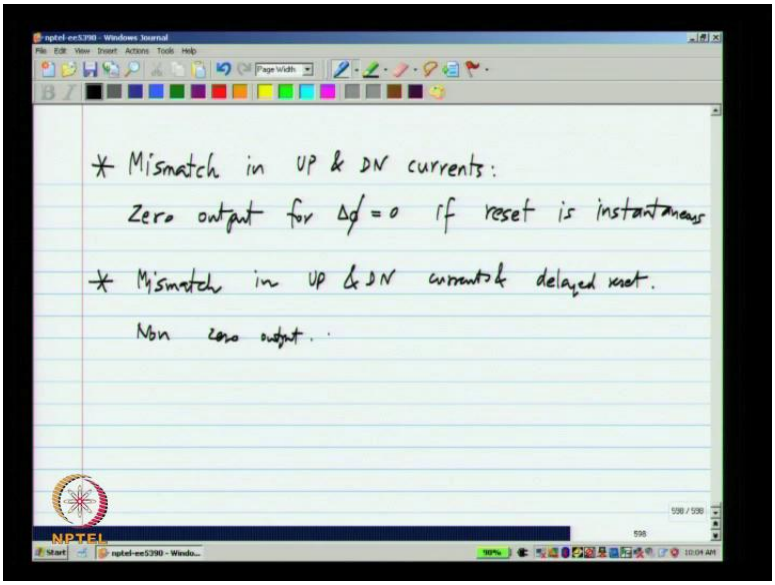
duration. And that will be I cp minus delta I the actual current that goes in to the R C filter is the difference between these two.

So, what really goes in there is I cp plus delta I for this duration and two delta I for that duration. So, this is what happens because of this it turns out that as the phase difference becomes 0 the output signal will not be 0 you can imagine that this part becomes 0. The reference and feedback signals are exactly aligned what will happen is then that up and down will both be high for a certain duration t reset up.

And down are both high the resulting current is not 0 because the two currents are unequal to each other. Now, if the two currents are matched then both up and down will be high for an equal duration and up minus down will be exactly 0. So, it is the combination of this reset delay and the mismatch between the currents that effectively gives rise to a phase offset what I mean by this is that if delta phi is 0. The output average will not be 0 that is very easy to see because if the reference and feedback signals are exactly aligned.

Both up and down will have the same shape and the output will be the difference between the up and down currents for that particular duration and in this example that will be entirely positive. So, what must happen is that down must lead up by a little bit. So, that you have a negative initial path and a positive path due to the mismatch and the net output is 0.

(Refer Slide Time: 44:23)



Basically entire type two phase locked loop synthesis was based on delta phi being 0 when the free running frequency equals the desired output frequency here. If there is mismatch between up and down currents and non0 reset delay. Then for delta phi equal to 0 output will not be 0. So, that means that in reality the operating point phase difference cannot be 0 and this results in certain reference feed through, which we will look at in the next lecture.

Thank you.