Analog Integrated Circuit Design
Prof. Nagendra Krishnapura
Department of Electrical Engineering
Indian institute of Technology, Madras

Lecture - 48
Type II PLL

Hello and welcome to lecture forty eight of analog integrated circuit design we were discussing the phase locked loop we have analyzed the type one phase locked loop, and saw that the periodic errors of the phase detector cause periodic modulation of the V c o output frequency and this leads to a lock range that is very small if the reference feed through has to be very small the lock range will be. So, small that you cannot use the phase locked loop, but we also noticed that the periodic error in the phase detector is proportional to the phase difference delta phi at the operating point.

So if the operating point phase difference is 0 that is if the output frequency happens to be the free running frequency of the V c o then there will be no reference feed through at all. So, we will exploit this fact you come with a better phase locked loop in which the reference feed through problem does not exist and it does not limit the lock range of the phase locked loop.

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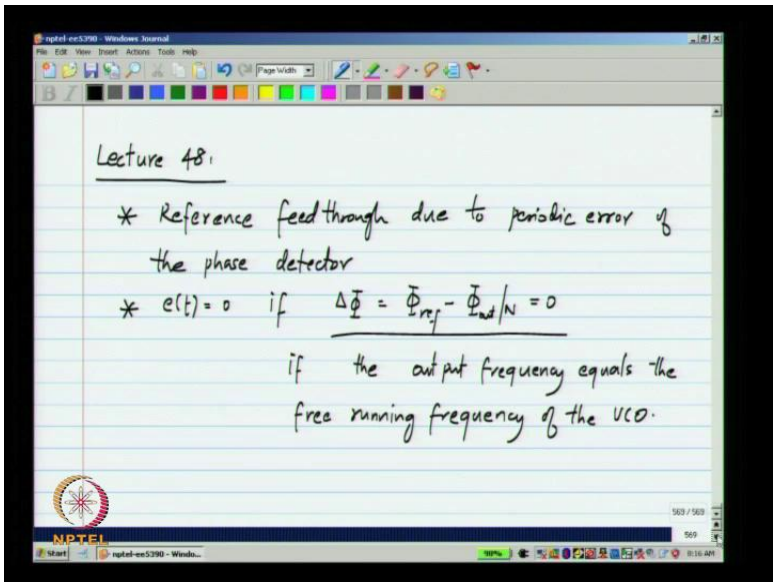

This is what we are going to exploit and this will happen if the output frequency equals the free running frequency of the V c o.

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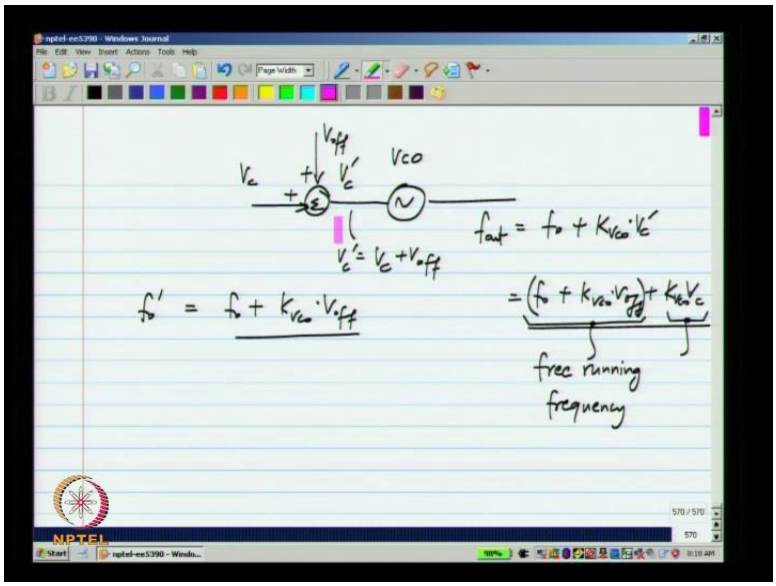

Now the question can we adjust the free running frequency of the V c o to be any value. Now we know that V c o to which control voltage V c prime is applied oscillates at a frequency f naught the free running frequency plus K v c o times V c prime. Now you can see that this f naught is like an offset to the desired output. This part is proportional to the control voltage V c prime and this is like a d c offset. So, an obvious way of changing the free running frequency of the V c o is to introduce a d c offset. So, let me call this V off and call this V c what happens is V c prime will of course, be equal to V c plus V offset. So, the output frequency will be equal to f naught plus K v c o V offset plus K v c o times V c. Now if you look at this the offset in this is this part and last part is proportional to V c. So, this is now the new free running frequency.

You can call it f not prime and that is equal to f not plus K v c o times V offset. So, by adding a d c offset to the control voltage of the V c o. We can change the free running frequency of the V c o as it appears from the control voltage V c. So, this is because the free running frequency itself is like a d c offset and we are adding another d c offset to that one.

Now what happens is if we adjust this V off appropriately the free running frequency can be exactly the output frequency that we want that is the new apparent free running frequency can be exactly the output frequency that we want in that case the operating point phase difference will be 0 and there will be no reference feed through.

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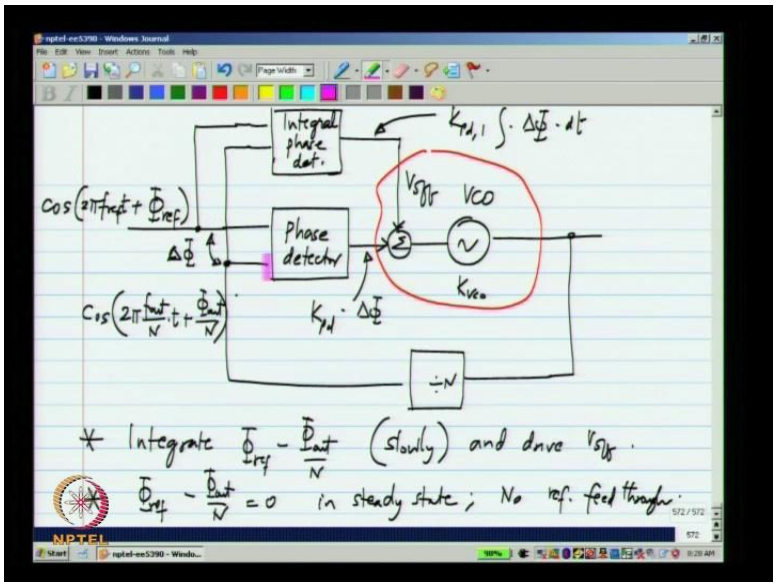

So, what should we do we have this phase locked loop I will show the model in terms of the signals and this goes to a phase detector and this is what we have had. So, far V c o has a gain of K v c o and this signal here will be cos 2phi f out by N times t plus phi out by N and the phase difference between these two would be delta phi which is equal to phi ref minus phi out by N.

So, now, what I will try to do is to introduce the d c offset here. So, what happens is if you think of this entire thing as the V c o the free running frequency of this will be the free running frequency of the V c o inside plus the V c o gain times the offset voltage. What I will then try to do is this is just a third experiment imagine that you have this arrangement and you go on adjusting V offset until the output frequency becomes equal to the free running frequency rather the free running frequency becomes equal to the desired output frequency .

Now how could I go about making this arrangement I have to go on adjusting V offset that is continuously until the new free running frequency f naught prime becomes equal to n f ref the desired output frequency. Now I need to do this electrically so, that means that I need to have an electrical variable in the circuit in the system which I can measure and based on that adjust V off continuously.

Now what is that variable that variable is nothing, but the phase difference phi ref minus phi out by N that is the phase difference between the input and the feedback signal. We

know that if the free running frequency happens to be exactly equal to the output frequency this phase difference will be 0.

So, what I have to do now is to adjust this offset voltage V offset until the phase difference becomes 0. Now this sounds very familiar to negative feedback adjustment of some quantity based on measuring some error this is what we have been doing all along this is how we synthesis the negative feedback amplifier and the phase locked loop etcetera we measure some error and adjust some variable continuously until the error is driven to 0.

So, what we have to do is based on the operating point phase difference phi ref minus phi out by n adjust this v off continuously that is integrate the error and adjust V offset. So, that finally, in steady state the phase difference becomes equal to zero. Now it is also clear here that this variation of v offset must be much slower than the main loop because again if you think of the third experiment what I will do is will first apply let us say zero offset I will let the phase locked loop steady state.

I will look at what the steady state phase difference phi out minus phi ref by n is based on that if it is positive I have to increase the increase the free running frequency. So, I will make V offset positive and then again let it reach steady state and measure the phase difference again and so on. So, essentially this will work in reality of course, the second loop also works in continuous time it does not work step by step like this, but you can imagine that for every setting of V offset the main phase locked loop has to reach steady state.

So, that you can make a new measurement the next time accurately and then adjust the value of v offset. So, what should I do here a measure of the free running frequency or the measure of difference between the free running frequency and the actual output frequency is this phase difference between the input and feedback quantities.

So, what I have to do is to integrate phi ref minus phi out by N and I have to do this slowly because what I am interested in is looking at the steady state phase difference between these two. So, I have to imagine that for every setting of V reference this loop reaches steady state you get the new phase difference and you measure it of course, in reality this happens continuously it is not a step by step process.

So, what I have do is to use an integral phase detector by that what I mean is the output of this here is some constant I will call K p d i for the integral path integral of the phase difference with respect to time whereas, this one is K p d times delta phi. Now what happens so, let us say you imagine that this V off here is zero initially and let us say to apply the signals then what happens is will also imagine that this constant K p d i is very small that is what is meant by integrating very slowly because if you have a constant here if K p d i is very small this voltage will ramp up very.

Very slowly then we can imagine that this reaches steady state within a short time and you have some phase difference this will have a nonzero input and it will start driving the offset voltage in some direction positive or negative it becomes positive the free running frequency of the composite V c o that is including V offset will increase that will give a new phase difference that is smaller and this phase difference will keep getting smaller and smaller and in steady state this phase difference has to be 0 because in steady state this output has to be a constant and output of an integrator will be a constant only if the input is 0.

So, what happens in steady state is that the phase difference here is 0 the this path the path that gives you an output proportional to the phase difference I will call it the proportional path it will have a 0 output and this voltage will be a constant which will make the free running frequency of this composite V c o equal to n times f ref and because this phase difference is 0 if you go back to the three state phase detector and see what it is doing the output will be 0 constantly it will not have the periodic component of the error and there will be no reference feed through at all.

So this is what happens so, this is a very clean way of breaking the tradeoff between reference feed through and the lock range. Now because in this case for any output frequency this delta phi will be 0 the range of the phase detector is not an issue the phase detector will be operating with a nonzero delta phi only during transients in steady state it will be zero. So, originally whereas, for type one phase locked loop the lock range was limited by the phase detector here the phase detector operates with zero phase difference in steady state. So, the lock range of the.

The range of the phase detector is not relevant. So, the lock range of the phase locked loop is not limited by the range of the phase detector it could be limited instead simply

by the range of the V c o every V c o will have some limits over which its frequency can be changed and it is very likely that the that range will limit the lock range of the phase locked loop

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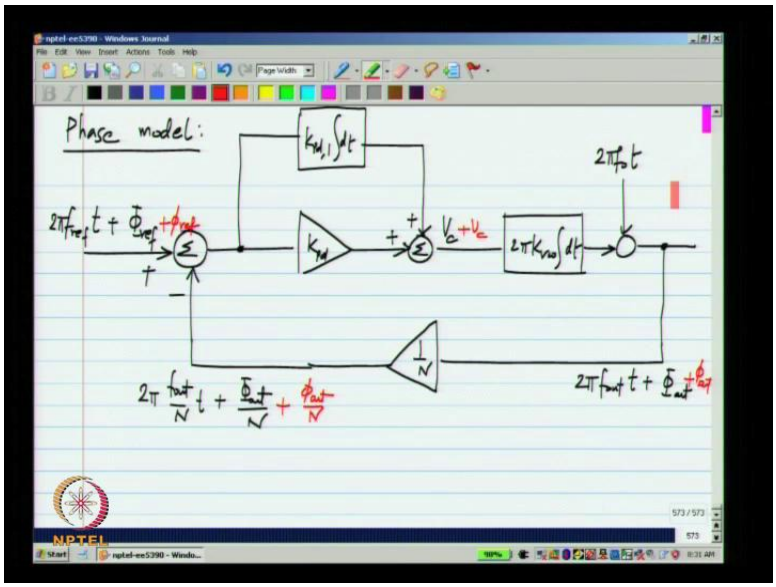

Now if we represent this with the phase model which is what is relevant for a phase locked loop here while only have the phase of the input signal which is two phi f ref t plus phase offset phi ref and here I will have something a proportional path that will give me a output proportional to the phase difference and an integral path that gives me a an output which is related to the integral of the phase difference and the sum of these two is given to the V c o which integrates the control voltage and adds a phase corresponding to the free running frequency and the divider of course, is just a attenuator of phase as I have explained before the output period of the divider is much longer than the input period.

So, any time shift at the input corresponds to a much smaller phase shift at the output when referred to the much longer output period. So, this is the model and the output signal will have a phase which is and the divider output signal will have now as usual the steady state can be determined without using the phase model, but what we are interested in is in the incremental model that is if you introduce disturbances anywhere in the circuit what happens?

So, I am showing it as the disturbance in phi ref, but it could be anywhere else also with increments this is what is going to be. So, originally we had some V c here will have n increment V c over there and the important thing is this part will remain fixed. So, the incremental phase model which is what we use for our calculations is given by this model where we have only the increments.

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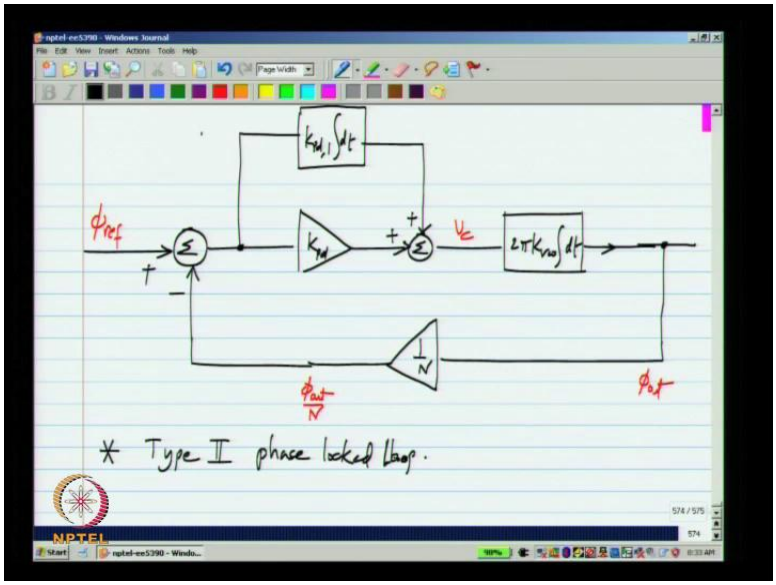

Now this is the incremental model and this is what is used for calculations of responses to different errors in the circuit and this is what we used earlier for the reference feed through now you see that first of all there are two integrators in the loop the integrator due to the integral phase detector and due to the V c o in the phase model and that is why this phase locked loop is known as a type two phase locked loop. So, this is control systems terminology type one has one integrator in the loop that will make sure that the steady state step error is 0, but the ramp error is not and type two phase locked loop where the steady state ramp error is also 0.

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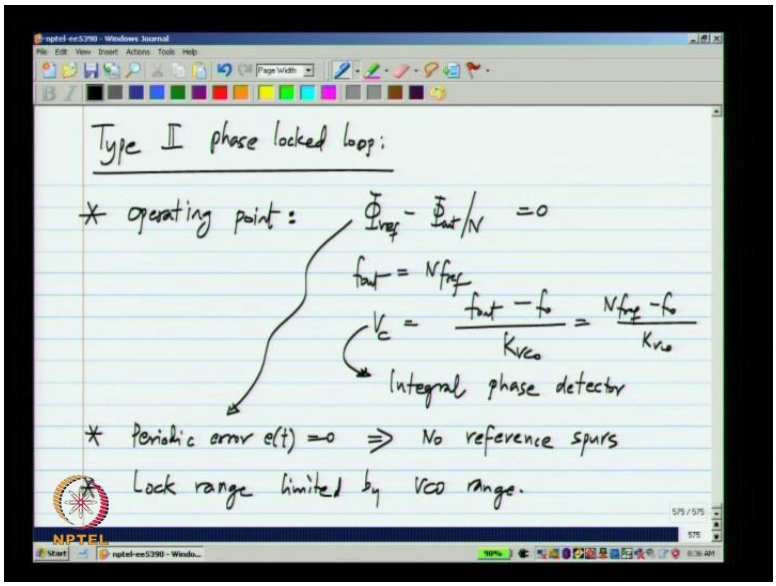

Now in the type two phase locked loop at the operating point we will have phi ref minus phi out by N to be equal to 0 and of course, the steady state output will be N times f f the control voltage will be of course, the difference between the output frequency and the free running frequency of the V c o divided by K v c o this has to be the case otherwise we will not get the output frequency, but the point is this will be the output of the integral path of the phase detector.

The proportional path will have a 0 output now because of this periodic error e of t will be 0 which means that there is no reference feed through or reference spurs now we will see later that due to non ideal features of the phase detector implementation there will be some periodic error, but it will be much much smaller than what we had earlier in the type one phase locked loop and the lock range is most likely limited by the V c o range or some swing limit in the circuit.

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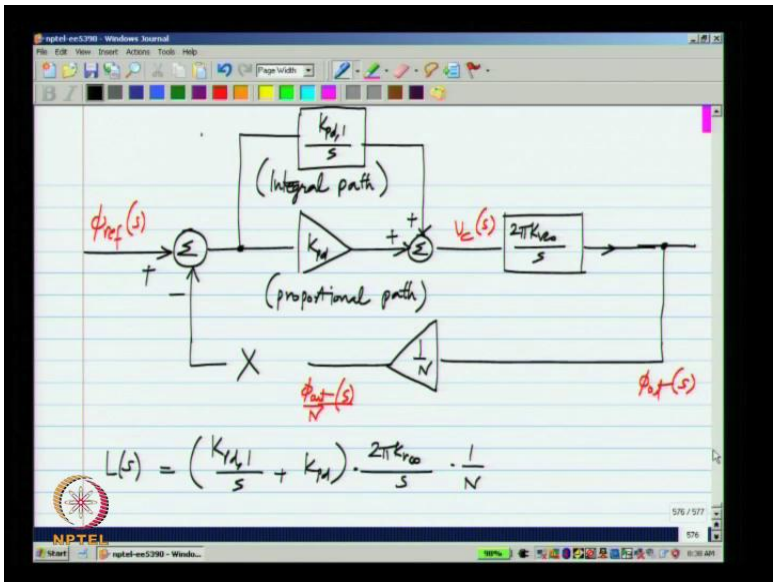

Now, that we have this increment model let us do a little more analysis of this and see what different parameters should be we have simply said that there should be a certain K p d and K p d i and so on, but we have not said what there should be and that we can get by doing the analysis of this system and for doing that analysis. We will use the frequency domain or the lap laws domain equivalent which means a simply replace this by K p d i by s and two phi K v c o by s and all these quantities will now be functions of s.

Now earlier we had a first order feedback loop which was always stable. Now we have a second order system and we also have to look at stability aspects of it that is whether it will have small damping factor or large damping factor what it should be and so on. So, first of all if we calculate the loop gain that is if we break the loop somewhere and go around the loop and compute the loop gain what do we get we will get the sum of these two that is and we will have the part due to the V c o and the part due to the divider. (

And if I plot the magnitude of this versus frequency what do we get at very low frequencies we will have K p d i by s times 2 phi K v c o by s times 1 by N because this number will be very large it be much more than K p d this system has two poles at the origin and one zero at K p d i divided by k p d. So, the loop gain starts off with a minus 40 d b per decade slope and at the frequency of the zero it changes to minus 20 d b per decade and if you look at the phase response what it will do is it will start with minus

180 degrees and it becomes minus one 35 at the frequency of the 0 and it will be at minus 90 degrees at high frequencies.

And if you look at this bode plot it is very similar to that of a two stage feed forward op amp two stage feed forward op amp also has two poles were at very low frequencies and then a zero before the unity gain frequency. And the unity loop gain frequency can be calculated quite easily for that it is instructive to write down the transfer function and in this region the transfer function is approximately K p d i by s 2 phi K v c o by s times 1 by N and in this region it is approximately K p d 2 phi K v c o by s 1 by N.

So, you see that this part of the transfer function is exactly the same as in the type one loop and that is not surprising basically for very low frequency this appears and for high frequencies the contribution due to this will be negligible compared to the contribution due to that one. So, we have only this part effectively and that will be the same as what we had in the type one loop.

So, the bandwidth is exactly the same as what we had in the type one loop that is the unity loop gain frequency which will be equal to the close loop bandwidth in radians per second is equal to the unity loop gain frequency also in radians per second and that will be two phi k V c o K p d divided by N times s. Now what should be the location of the zero we know that this zero must appear before the unity loop gain frequency we have discussed these things extensively while discussing stability of negative feedback systems and feed forward compensated op amps and so on.

So, this has to appear before the unity loop gain frequency and this is also consistent with our earlier saying that the integral path should change things very slowly compared to the proportional path the view we took earlier was that the main loop has to reach steady state and based on that the integral path will makes some corrections very slowly it will let the main loop re steady state and then make corrections and in the frequency domain that is equivalent to saying the zero has to be at a frequency that is lower than the unity loop gain frequency.

Now, how much lower should it be that depends on the damping factor that you would like to have and peaking magnitude and so on. So, then we can now calculate the transfer function from phi ref to phi out now we can also calculate the transfer function from any

other error injected to phi out, now what we will see later is that everyone of these components will have noise or some errors.

So, we will have errors injected to different parts we already have experience with this for the periodic error of the phase detector which gets injected here similarly the V c o will have some phase noise that will get injected there the phase detector combination and the loop filter will have some noise which will get injected there and similarly the divider can have some noise which will be injected there and so on. Now all those transfer functions will have the same denominator.

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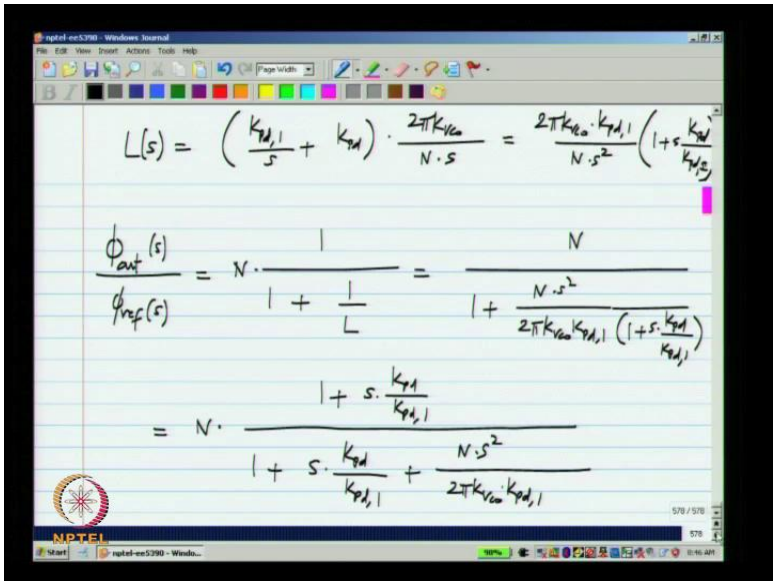

So, what we discuss based on the transfer function between phi ref and phi out will also hold for those other transfer functions phi out of s by phi ref of s this is what we want to calculate let me write down the loop gain again l of s will be and phi out of by phi ref I will write it directly it will be of the form N which is inverse of the feedback fraction times one by one plus one over l which is N divided by one plus n times s square two phi k v c o K p d i and will also have one plus s K p d by K p d i which will be N one plus s times K p d by K p d i and one plus s K p d k p d i plus n times s square two phi K v c o K p d i.

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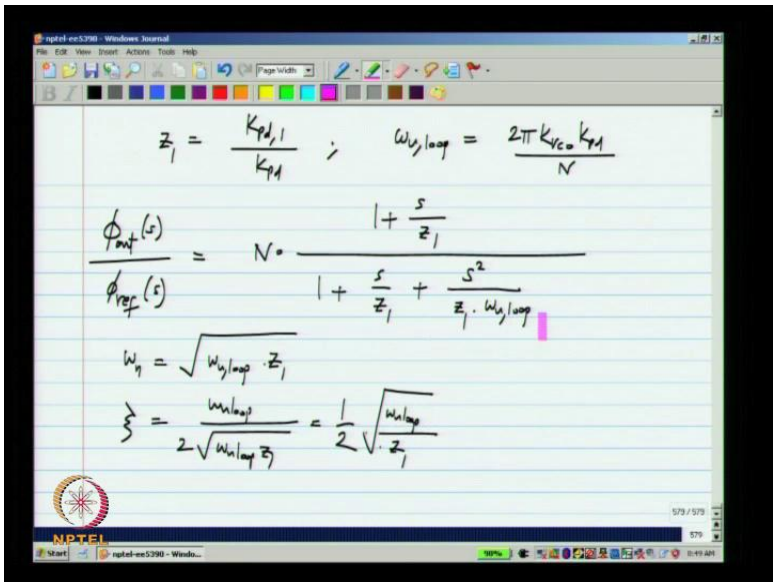

We know that the zero is at K p d i by K p d and the unity loop gain frequency that is assuming that the zero is at a sufficiently low frequency will be at two phi K v c o K p d divided by N. So, in this case phi out by phi ref can be written as N and this is exactly the kind of transfer function we encountered in a feed forward compensated op amp. So, you can go back to those lectures and look at the details and from the denominator we can see that the natural frequency will be square root of omega loop times zee one and the damping factor will be which should be half square root of omega n loop divided by zee one this again confirms our conclusion earlier that this zero zee one has to be smaller than omega n loop.

So, that you get a damping factor that is close to one or even one or more than one now this damping factor will affect the settling that is if the damping factor is very small there will be a lot of ringing which is usually undesirable and if would like to have a critically damped system then the damping factor has to be equal to 1. So that is one of the constraints, but there is also another constraint if you plot the frequency response of this transfer function.

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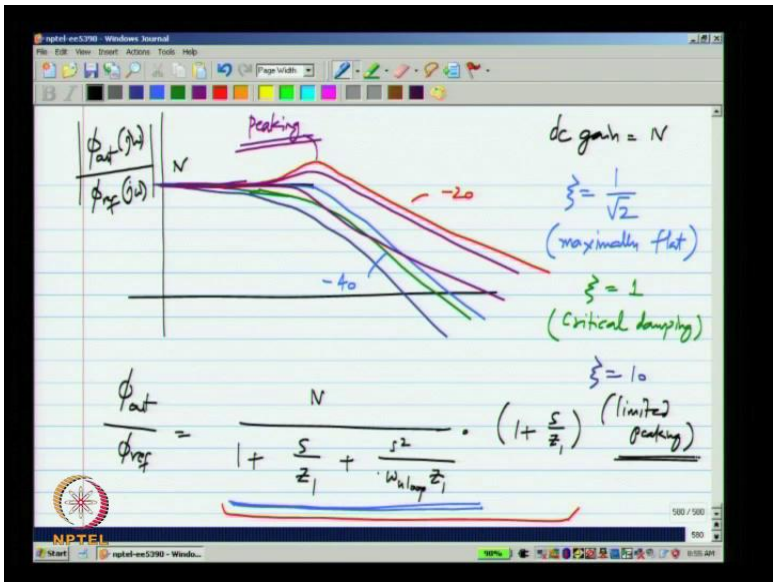

So, let us say we have plot the magnitude response of phi out by phi ref the low frequency gain will be N now this again we have the intuitive explanation for the output frequency is N times higher than the input frequency. So, any time deviation in the input any delay in the input will translate a corresponding delay in the output, but because the output period is shorter than the input period in terms of phase it will correspond to a much larger phase.

So, the d c gain will be N. In fact, we can write this as let me separate out the denominator and numerator of the transfer function part phi out by phi ref let me write it as N divided by the denominator and this times one plus s by zee 1. Now, let me first plot the transfer function of only this part of it. Now we know that this is a second order low pass filter transfer function that is only the part that I have marked in blue and if zeta is 1 over square root of two that is slightly less than one then this will have a maximally flat response that is only this part of it.

Now if I plot the overall transfer function that is including the 0 what happens is this 0 will introduce a rise in the transfer function and eventually it will do that the slope of this will b minus 40 d b per decade and the slope of that will be minus 20 d b per decade. Now, similarly even if you adjust it for let us say zeta is equal to 1 corresponds to critical damping and in that case the magnitude response will usually droop off a little more like that, but if you include the 0 you will still tend to get something of this sort that is mainly

they will be a peaking in the response and this is not due to low damping factor, but this is due to 0. So, what I am trying to emphasize here is that let us say you have a second order transfer function that is you do not have any zeros and you only have a second order denominator.

In that case adjusting the damping factor to be one over square root of 2 or quality factor to be 1 over square root of 2 will give you a nice maximally flat response and that is desirable in many circumstances. And now such a response will slightly be under damped so, that means, there will be a slight ringing, but that is very slight that is also usually tolerable now if no ringing is tolerable you can make the damping factor equal to 1 and then there will be no ringing at all of course, and magnitude response will be slightly more droopy compared to zeta equal to 1 over square root of 2.

Now in this case the bandwidth will be slightly lower, but that is also usually acceptable, but in this situation in a phase locked loop what we have is something different we also have a 0 in the transfer function. So, the transfer function will have a peak that is the magnitude of the transfer function will rise above the d c value for some frequencies because of the 0 and in a phase locked loop in many cases this is undesirable.

We will later see that this will amount to if the reference has some jitter it will get amplified first of all it is already getting magnified by a number N, but that is something fundamental that cannot be helped, because the input frequency is at n times lower than the output frequency the output jitter will be in terms of phase will be N times the input frequency, but many times you would not like to go beyond N. So, this boost the boost in gain because of the 0 is undesirable.

Now if you want to limit the amount of boost amount of boost in the magnitude response because of the zero you have to reduce the zero frequency to much smaller values much smaller than what is dictated by a damping factor of one let me take yet another case where, let us say zeta is equal to 10 or something what happens then is that the part due to only the denominator will do something like that its bandwidth will be even smaller and including the zero it may have a slight peak, but not too much.

So, if peaking is of a concern you would adjust the transfer function for a damping factor that is much more than1. Now this has a disadvantage if you make let us say the damping factor hundred that is you make the zero frequency much slower than the unity loop gain

frequency what happens is that you will get a very high damping factor, but from these expressions you also see that the natural frequency becomes very small.

So the phase locked loop response does becomes slower if you make the damping factor higher, but that is something that is the price you may have to pay if peaking in the magnitude response is a concern many times peaking in the magnitude response is a concern because the phase jitter or phase noise of the reference will get amplified too much if you have a lot of peaking. And many times you will be given the specification on peaking as well let us say one d b that is at d c the gain is n and maximum it can go above that is one d b and based on that you can adjust the damping factor and that damping factor usually comes out to be significantly more than one.

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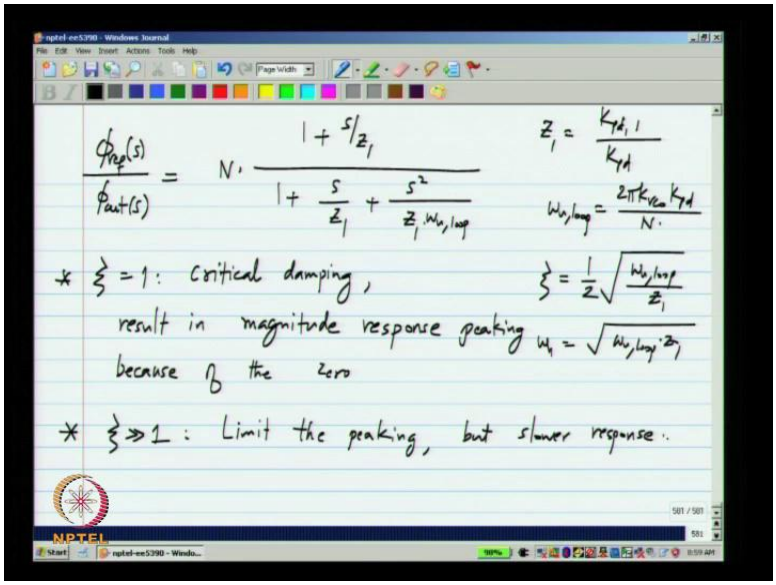

So, in summary the transfer function as a d c gain of n it has a zero and two poles and zero is at this ratio of the phase detector constants that is integral phase detector proportionality constant divided by the proportional phase detector proportionality constant and the unity loop gain frequency is 2 phi K v c o K p d divided by N times N and the damping factor will be half of that one and the natural frequency will be the geometric mean of the 2 zeta is equal to 1 for instance is critical damping and what this will result in magnitude response peaking because of the zero and zeta much more than 1 will limit the peaking, but the response will be slow.

So, you have to decide based on the specifications and requirements in the given application which is more important not to have magnitude response peaking all to have a sufficiently quick response and decide the damping factor accordingly. Now there is one more aspect that we have not discussed and we will not discuss further that is one of the facilities of this phase measurement is that.

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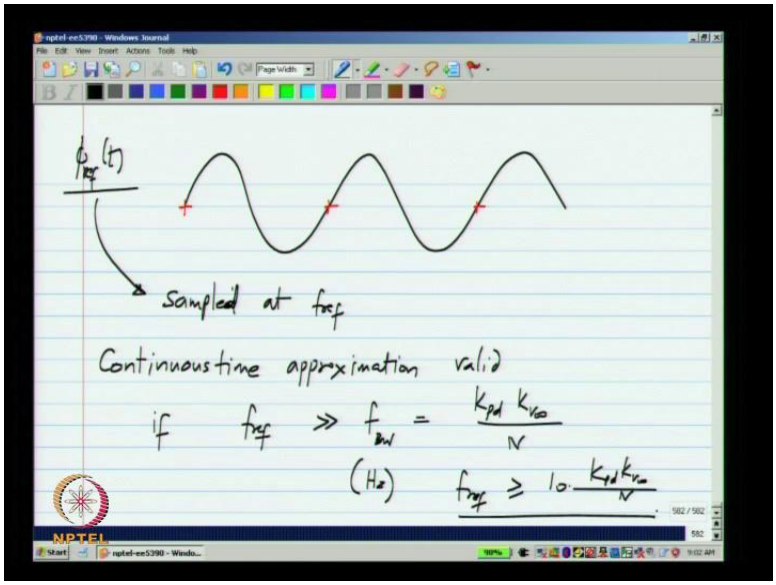

So, let us say we have a sinusoidal signal now or any signal sinusoidal or square wave we say will do phase detection, but the way we have been doing the phase detection and the way it is reasonably possible to do phase deduction is only at the zero crossings of the wave form although we represent let us say phi ref of t as a continuous wave form we are making the phase detection we are doing the phase detection or making phase measurements only at the zero crossings.

So, actually this phi ref of t is sampled at the reference frequency. So, this entire system is a hybrid system it has continuous time parts like the V c o and integrator and so on and it also has the discrete time parts that is the input phase is sampled at phi ref and the feedback phase is also sampled and so on, but it is too complicated to deal with that on a course like this now it turns out that if the response of the system is sufficiently slower than the sampling frequency or the reference frequency.

We can make this continuous time approximations and get away with it we can deal with everything in continuous time and that is a convenient thing to do and the answers will

be sufficiently accurate and a constraint for that is that this is valid if the reference frequency happens to be much more than the unity loop gain frequency or the bandwidth the bandwidth of the phase locked loop which is nothing, but K p d K v c o divided by N.

So, this is the bandwidth in harts. So, this is k p d times k v c o divided by n and typically if f ref is greater than let us say ten times the bandwidth this will hold. So, this is another constraint on the bandwidth this is really a constraint for the continuous time approximation to hold, but it turns out that this constraint is also satisfied by many many real phase locked loops. So, it is not an unrealistic constraint. So, the reference frequency will be ten times more than the bandwidth or the bandwidth that you set will be ten times less than the reference frequency and frequently it is a lot less it can even be hundred times smaller and so on. Now we have calculated the transfer function from here to there we see that it is a second order low pass transfer function with a 0.

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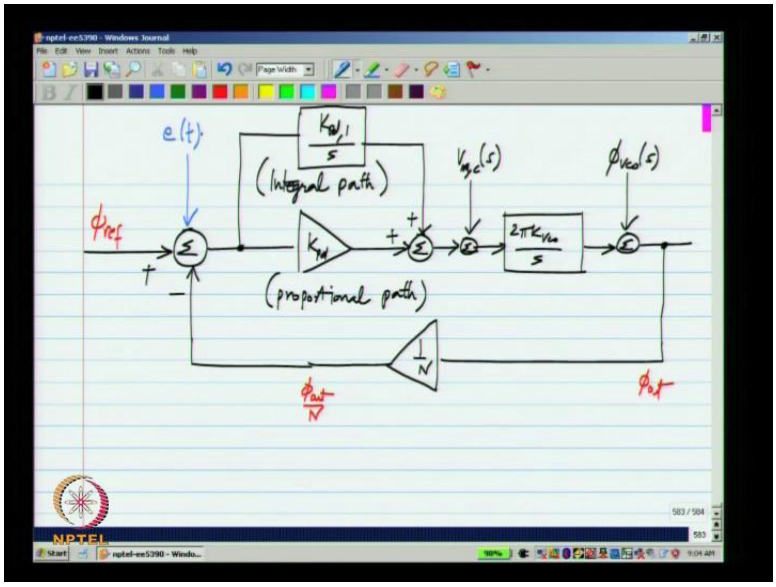

Now in addition to this let me copy over this. Now that represents the frequency response from the reference phase to the output it also represents if the phase detector has some errors like we had earlier. So, if we had e of t over here it also represents the transfer function from this to the output now errors can be injected in others places for instance at this point there could be a voltage noise or some kind of error that is injected at the control voltage let me call it V n c to denote that it is the noise in the control voltage and we could also have the V c o inject some phase error the V c o will have a

noise just like every component has noise with a V c o will noise in its phase it is called the phase noise of the V c o and it' s also interesting to find out the transfer function from that one. So, again exactly the same block diagram can be used. All these again will be functions of s. So, let me make that modification this will be K p d i by s and this is two phi K v o by s this is V n c of s and this is phi V c o of s.

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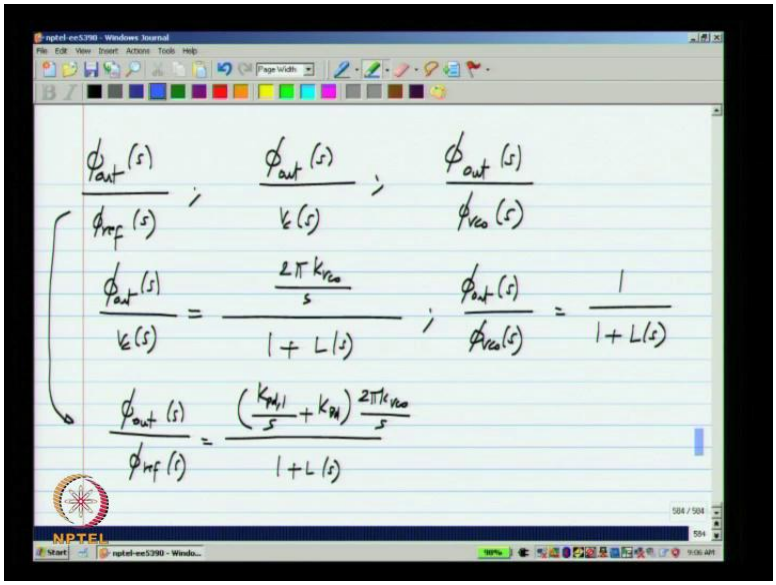

Now I have already calculated phi out of s by phi ref of s we can also calculate phi out of s by V c of s and phi out of s by phi V c o of s and so on. And this is just a matter of slightly modifying the result that we had earlier phi out of s by V c of s will be two phi k V c o by s divided by 1 plus l of s and phi out of s by phi V c o of s will be 1 by 1 plus l of s and just for completeness this is something we have already evaluated phi out of s by phi ref of s in every case it is the gain of the forward path from where we inject to where we take the output divided by 1 plus the loop gain.

So, what we will do in the next lecture is to evaluate these transfer functions and get an idea of how they behave over frequency, then we will look at what kind of errors can be injected at different parts and see how to specify them they form an important set of specifications for the phase locked loop over the V c o, and we will look at those things.

Thank you, I will see you in the next lecture.