Analog Integrated Circuit Design
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Lecture No - 46
Phase Domain Model

Hello and welcome to lecture 46 of analog integrated circuit design. In the previous lecture, we came up with the block diagram of the phase locked loop which is a circuit block used for multiplying frequencies. In this lecture, what we will do is to see how to modulate and evaluate the characteristics and also see how to build some of the blocks of the phase locked loop.

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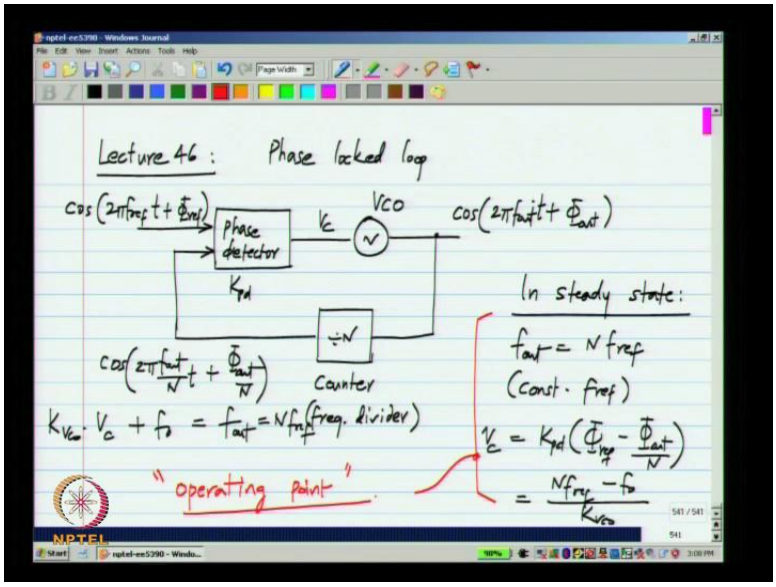

The system we came up with was like this, we have a voltage controlled oscillator which generates a controllable output frequency. So, the output signal will be cos 2 pi f out plus some praise offset phi out and we have a frequency divider or a counter. The input of course, is at the reference frequency. This is the control voltage. This control voltage, for this to be steady this ramp here has to be exactly equal to the ramp at this point and based on that the output will be at some constant frequency f out and that constant frequency f out will be n times f ref. In steady-state f out will be n times f ref. If this is not the case v c will be either ramping up or down as you expect in any negative feedback system and of course, we assume constant f ref and this constant value of Vc will be Kpd. That is the

gain of the phase detector times phi ref minus phi out by N. It is the difference between these 2 phases. The ramp parts are equal to each other and other parts we take the difference of multiplied by Kpd and we also know that Vc should be such that the output frequency is f out. This is again a property of the negative feedback system. The output of the integrator will adjust itself so that the final output will be whatever is desired by the negative feedback system.

So, that means, that KVco times Vc plus the free running frequency of the v c o must be equal to f out which of course, is n f ref. This is the same as saying Vc will be equal to N f ref minus f naught; the free running frequency divided by k v c o basically this Vc will cause the output frequency of the v c o to deviate from the free running frequency. So, Vc will be equal to the deviation from the free running frequency N f ref minus f naught divided by the v c o gain and this you can consider to be the operating point of this phase locked loop okay?

So, that will be the operating point. Now, like in any other system we will be analyzing the phase locked loop when there are disturbances introduced in it and for that we will do incremental analysis around this operating point. Now, before we do that, as I mentioned many times earlier, what we are interested in is the phase of the signals. That is, we are interested in looking at whether these signals are exactly periodic or not and not in the exact ah waveforms of each of the signals. So, the input signal, the output signal and output of the divider, we are only interested in the frequency of. The control voltage of course, is an important quantity and that will be retained as a voltage.

So, what we will do is reduce this to a model in the phase domain where we will be representing only the phases of the signals. That is phase of the input signal, phase of the feedback signal and phase of the output signal. Of course, control voltage will be part of this model and analyze the phase locked loop based on that model. That is model in the phase domain.

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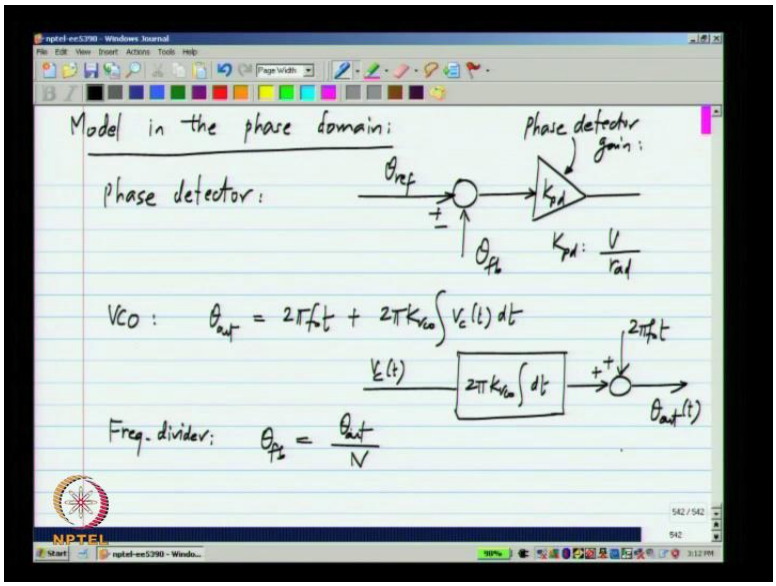

So, if you model each of these blocks in the phase domain, the phase detector of course, is very simple. All it does is to take the phase of the reference and phase of the feedback signal, multiply the difference by this number K p d which is the phase detector gain and the input quantity is phase in difference in radiance and output is in volts. So, this k p d has units of volts per radian or volts.

This is the output of the phase detector. Then the Vco itself we have already modeled this. I will show the picture of it. We know that the output phase of the Vco is the ramp corresponding to the free running frequency plus something related to the integral of the control voltage. The input of the Vco is the control voltage and output is some signal with this phase. Here we will be modeling only the phase. So, we take Vc of t, integrate it, add this ramp of 2 pi f naught t and so, the output will be the phase of the v c o and finally, the counter or the frequency divider. In this case the output phase theta f b will be simply the input phase which is the output phase of the phase locked loop divided by N.

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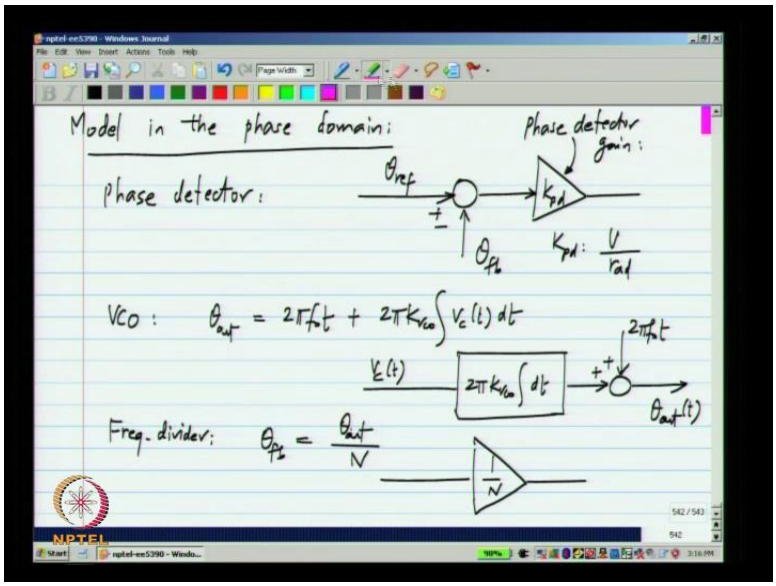

Here the frequency divider is operating with an input theta out. When I say theta out, it is the output of the phase locked loop and that is equal to 2 pi f out t plus some phase offset phi out and the feedback phase will be nothing but 2 pi f out by n times t plus phi out divided by n. So, this part must be pretty clear. It is a frequency divider after all. So, the output frequency will be 1 by n times the input frequency and this part again must be quite clear because imagine that the input is a sinusoid of this type. The output will be, let us say it is a divide by 2 counter.

So, it will have 1 cycle for every 2 cycles of the input. It will look like that and let us say the input sinusoid is shifted by some phase. What will happen to the output? It will also be shifted by the same amount in time. So, the phase difference between these 2 is this. The time difference is let us say is some delta t. Now, this delta t as a fraction of the output is half as much as delta t by the period of the output signal is 1 by 2 times delta t by the period of this input signal. This is because the output frequency is half of the input frequency.

So, it is shifted by the same time period that means that, the phase difference is half. In general, if you divided the frequency by N, the phase also gets divided by N. The reasoning is very simple. The output will be time shifted by the same amount that corresponds to 1 over N times smaller phase when you calculated for the longer period at the output of the frequency divider. So, the model for the frequency divider is extremely

simple. It is this attenuation by N. So, with all of these we can put the phase model of the phase locked loop together. Phase of loop is usually abbreviates PLL.

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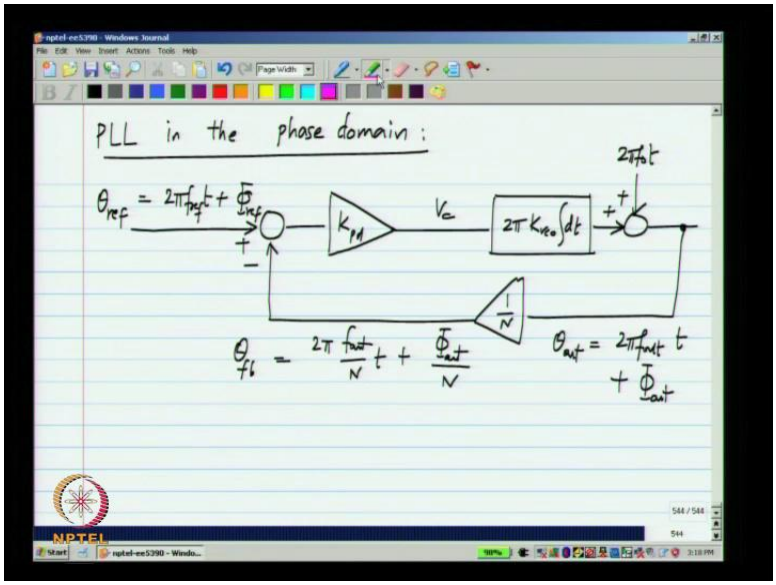

So, this is the phase model of the phase locked loop. In this model, we only considered the phase of the input feedback and output signals. Now, we have not yet looked at how to realize the phase detector and Vco design we will come to later. Now, we will take for granted that it can be realized. Now, the design of the phase detector presents certain inherent problems in the phase locked loop.

So, we will have to analyze those. In order to be able to analyze that, we have to come up with an incremental model of the phase locked loop in which let us say we introduce an incremental disturbance at some point. We will be able to calculate the effect of that on other signals, importantly the phase of the output signal. That is for instance to the input phase theta of t, I add a time varying component phi of t. It will clearly change the output in somewhere and I have to be able to calculate that.

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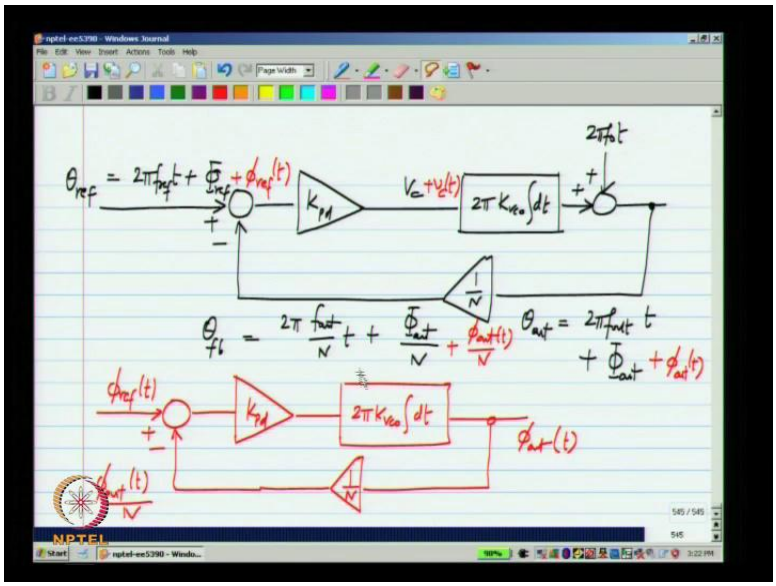

So, let me take this entire block diagram and place it here and what I do now is let us say I added some increment to the reference phi ref of t. What will that do? In general, there will be increment in every quantity in the circuit. We have these things and then of course, here we will have this phi out by N. Now, I am not so interested in the operating point quantities because once I calculate that, that part is fixed. So, for analyzing the relationship between the increments, I will come up with an incremental model in which only the increments are present.

So, how do I get that? I get that by subtracting the corresponding quantities in the model with increments and in a model without increments. This is what we have done earlier to derive incremental models of circuits. That is what we do for the phase locked loop and here. So, in all these quantities, only the increment will remain and this 2 pi f naught t which is fixed in both the model with the increment and without the increment will go away.

So, the result will be, I have the input phase increment phi ref and in the phase increment in the fed back quantities subtracted from that I have Kpd and this integrator which represents the Vco in the incremental sense. So, this part 2 pi f naught t which is fixed will go away and these things remain as they are. In fact, you see that in this model everything is linear. So, the blocks will remain as they are. The only part that goes away is this fixed ramp 2 pi f naught t.

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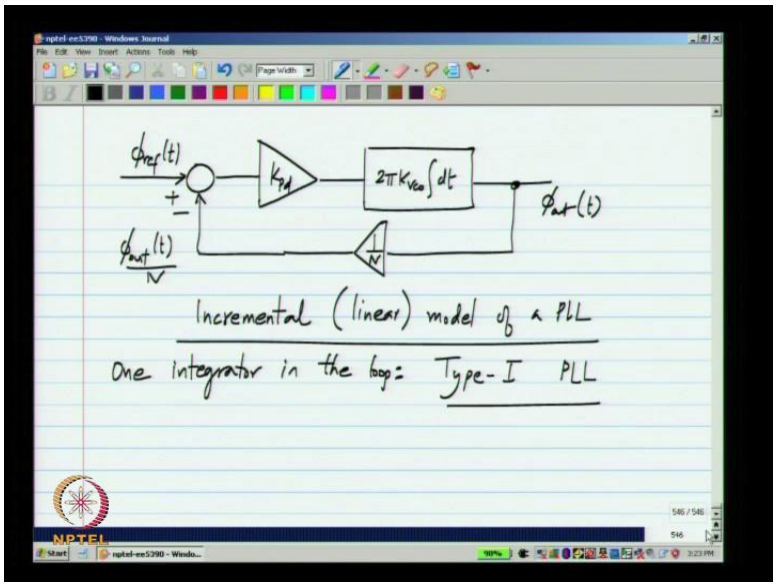

This is the incremental and of course, linear model of a PLL that is used very, very widely to calculate the effect of disturbances. Basically to calculate everything that is related to the phase locked loop. You see that inside the loop in the loop gain, there is 1 integral. That is this 2 pi Kvco integral d t. The integrator is contributed by the Vco and in control system parlance this is known as a type 1 system and this particular system is known as a type 1 PLL. That is the PLL that we designed earlier, this one, this is known as a type 1 PLL.

So, from this incremental model, we will calculate many characteristics of the phase locked loop and we will see that there is some inherent conflict between two different requirements and we will see how to solve. So, the first thing we will do is to get an idea of how to implement a phase detector. There are many, many topologies of the phase detector but, generally they are similar in principle and will anyway be focusing on some general characteristics of any phase detector.

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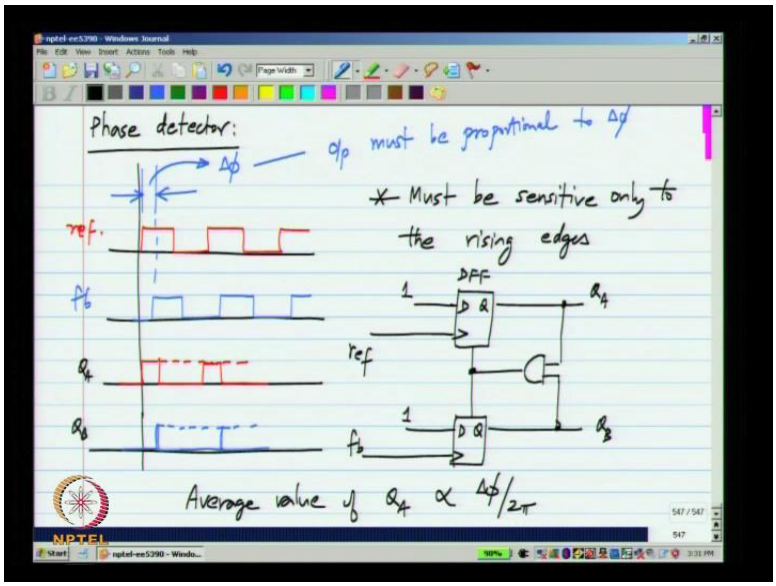

What is this phase detector suppose to do? It is supposed to take the phase difference between 2 waveforms. Let us say, they are like this. The reference waveform looks like that and the feedback waveform looks like that and for convenience I have shown them to be at the same frequency. What is the phase detector supposed to do? It is supposed to give an output signal which is proportional to the difference between the rising edge of the reference and rising edge of the feedback or you could alternatively take the falling edge of the reference and falling edge of the feedback. We will work with rising edges for now and this is delta phi and the output is supposed to be proportional to delta phi. So, that is one thing and secondly, we would have some characteristics that are desirable in a phase detector. It must not be sensitive to the duty cycle of the signals.

In other words, it must be sensitive only to the rising edges or it should be sensitive only to the falling edges but, it should not be sensitive to the details of the waveform in 1 period. Of course, the waveform in the second period will be the same as in the first period and so on but, within each period it should not be sensitive to the details of the waveform. Again we are only interested in generating periodic quantities. We will not concern ourselves with the problem of generating some particular waveforms. So, whatever we do here should not be sensitive to the exact waveform and another reason to be insensitive to the waveform is that if you take a digital counter and set the modulus to different values. So, let us say you have an even modulus, you could have a 50 percent duty cycle and if you had an odd modulus you could simply cannot

have a 50 percent duty cycle. You all had something skewed from 50 percent and some counters can have duty cycles of output which are very different from 50 percent. So, it should not be dependent on duty cycle and so on. It should be sensitive only to the edges. So, we must come up with the phase detector which does this. So, one possibility is, we know that the one circuit block that is sensitive to the edges is a flip flop.

So, let us say we take a deep flip flop and connect its input to one and connect the clock to reference. Now, what will this do? This is in some way sensitive to the edge. Now, let me assume that initially this output state is 0 and when the reference edge arrives, it becomes 1. Of course, if we do not do anything else, it will remain at 1 and we do not have any useful information but, this is something which gives an output sensitive to the edge of the reference. It gives an output at the edge of the reference. Similarly, I also have to be sensitive to the edge of the feedback signal. So, I use an identical block that is a deep flip flop with the input tied to 1 and the clock tied to the feedback signal. So, what happens? Let me call this Qa and Qb. What will Qa do? It will do that and Qb will do that.

Now, we would like the output to be proportional to the difference between these 2 and also more importantly we cannot leave the output like this. In the next period we should be able to again detect the phase. So, what we should do is to reset the flip flop so that Qa and Qb go to 0 before the next period so that, you can start off all over again and again. A convenient choice is to reset the d flip flops when both of them become high and this is the kind of an obvious choice. When Qa becomes high you have information about the rising edge of Qa and after Qb becomes high, there is no further measurement that can be done. So, we already have a measure of the difference between Qa and Qb and you can reset the flip flops. That is what is done here.

So, what really happens is, it would not continue off like that. You did not do anything you could do that. Here again if you did not do anything you could do that. What happens is as soon as Q b goes up, both of them will get reset and this does that. This one does that and in the next period it will rise up again and Qb will also tend to rise at the rising at the edge of f b and both of them will be reset. So, this is what the output will look like.

Now, where is the information about the phase? If you look at the duty cycle of the signal Qa, it is basically delta phi by 2 phi where delta phi is the phase difference between the 2 signals or in other words you look at the average value of Qa. It is related to the phase difference and the average value of Qb is 0 because it is not changing at all. As soon as it is rising it is also falling back to 0.

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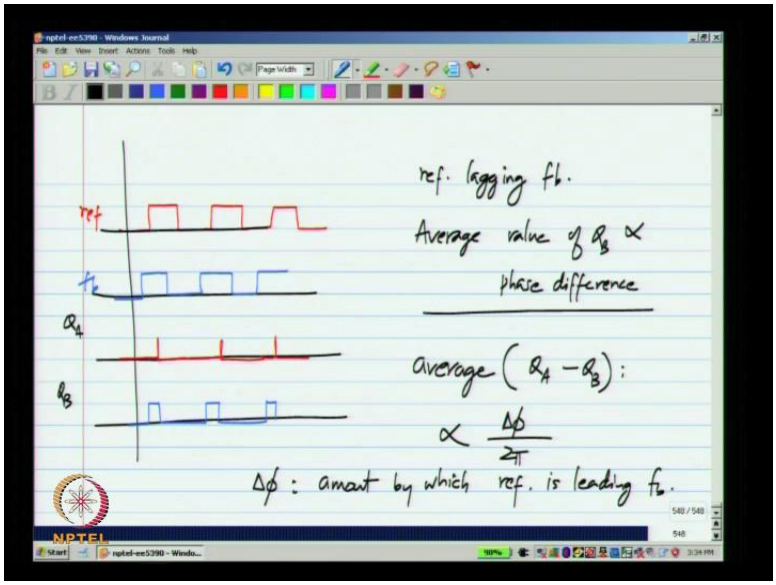

Now, you can take the alternative scenario where the reference signal is lagging the feedback signal and you can see that this system is exactly symmetrical between reference and feedback signals. So, the output will be reversed. What happens is you plot Qa and Qb. Qb will rise here and Qa will rise over there and immediately get reset. Qb will also get reset. In the next period exactly the same thing happens again. Something like that. In this case I have shown reference lagging feedback. In this case average value of Qb gives the phase difference.

Now, what we would like is when references leading f b for the output be positive and references lagging f b for the output be negative. So, it is very easy. If you take the average value of Qa minus Qb this will be nothing but some quantity proportional to delta phi by 2 pi where delta phi is the amount by which reference is leading the feedback signal.

So, if reference is actually lagging the feedback signal; that means, that this delta phi is negative and the average value will also be negative because if reference is leading the

feedback signal, Qa will have a positive average and Qb will have 0 average. If a reference is lagging the feedback signal, Qa will have a 0 average and Qb will have a positive average. So, this is a phase detector whose average output is related to the phase difference between the two signals. This by the way with 2 flip flops is known as the 3 state phase detector to be 2 flip flops it can actually have actually have 4 states, but Qa and Qb cannot be simultaneously high because that will reset the flip-flops.

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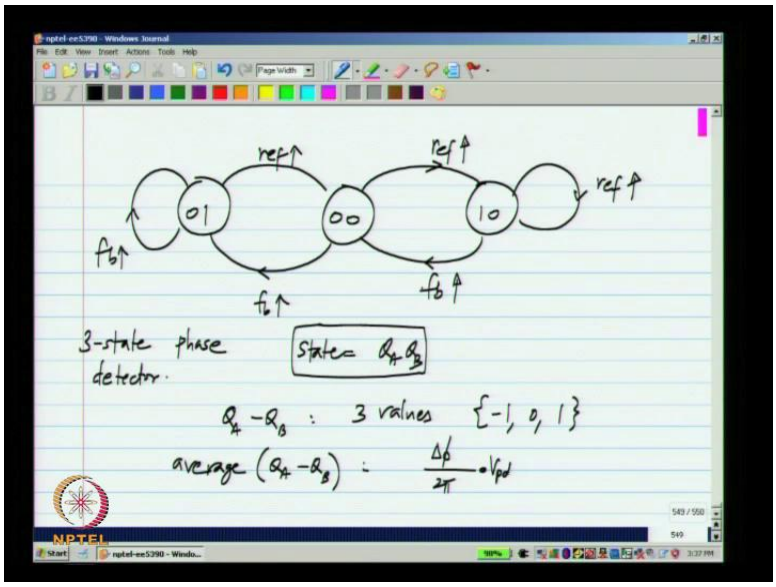

So, that state is forbidden and there were a total of three states and if we plot the state transition diagram by state, I mean Qa Qb, there are 3 possible states. 1, 1 is not allowed from this 0, 0 state, if we get a rising as the reference it will go to 1, 0 and if you keep getting rising as a reference the output will not change at all and from 1, 0 if you get the rising as the feedback, it will come back to 0, 0.

Again from 0, 0 if you again get a rising edges of the feedback will go to 0, 1 you get a rising edge of the reference you will go back to 0, 0 and if you get rising edge of a feedback it will stay at 0, 1. So, if reference is leading feedback it will go between these 2 states. If reference is lagging feedback, it will go between these 2 states. This is known as the 3 states phase detector. The output Qa minus Qb takes on 3 values as well which are minus 1, 0 and 1.

The average value of Qa minus Qb is what gives you major of the phase difference. It will be delta phi by Vpi times Vp d. By Vp d, I denote the voltages corresponding to

logic 1 either Qa or Qb. So, this will be repeating and you can see that this has the dimensions of volts per radium. So, that is a 3 states phase detector in average since that gives you the phase difference between the input and the feedback quantity.

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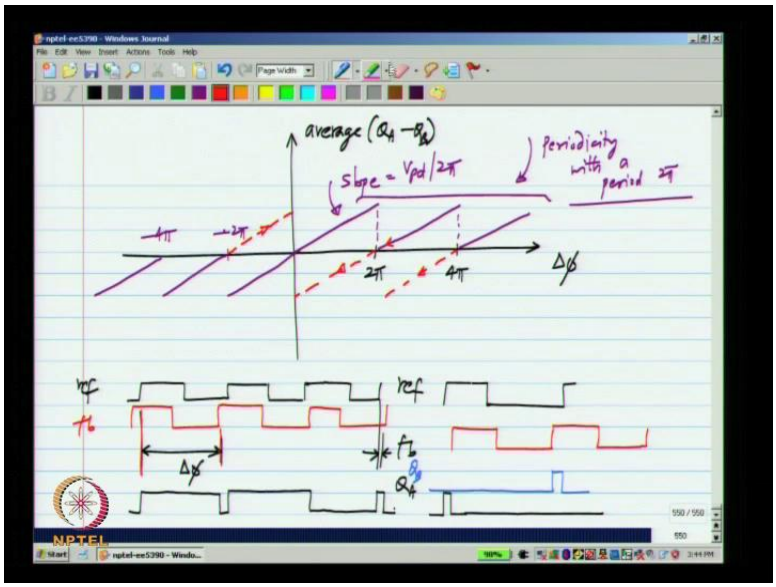

Now, if you plot the characteristics versus the phase difference, delta phi. What happens is that, you can imagine that you start with reference and feedback which are coincident. So, let us say initially they have coincident edges and under reference starts to lead the feedback slowly. That is successive edges appear earlier and earlier. Let us say this happens very, very slowly. So, what happens is, essentially I am increasing the value of delta phi and trying to measure the average output.

So, what will I get? Initially, I will get pulses which are narrow. Qa will be a narrow pulse and then it will become wider and wider and so on. So, the average value of Qa minus Qb will go on increasing. Now, what is the maximum phase difference that you can measure? So, let us say the feedback wave form is like this and the reference wave form is like that. So, the reference is leading feedback phi delta phi. In this particular cycle, this is the reference, this is the feedback.

Now, let us say in the next cycle it leads it by some more and the edge appears over there. What happens? During this part Qa will be 1 but, after this rising edge as the feedback, it will fall back to 0 and after that what happens is you start getting narrow

pulses of Qa. So, here you will get a Qa which is very wide and then here you will get a Qa that is very small. That is the difference between these 2.

What I am trying to say here is, here the delta pi is almost equal to 2 pi and once it crosses 2 pi it becomes module 2 pi and small. Now, this is some inherent property of the phase itself. So, if you have 2 signals and if you say that 1 of them is leading the other by 2 pi plus delta something, it is the same as saying that the waveform is leading only by the delta. So, if you lead by 361 degrees, you are really leading only by 1 degree.

So, up to delta five equals 2 phi, the output will go on increasing and then immediately jump to 0 and it will go on increasing if you further increase it and so on. 4 pi et cetera. So, inherent property of the phase, phase is modulo 2 pi makes the characteristic of the phase detector periodic with the period 2 pi. The slope here and everywhere will be Vpd by 2 pi.

It will have this periodicity with a period 2 pi. The exact periodicity of a phase detector depends on the implementation. It could be periodic with pi or many times of 2 pi depending on basically how much storage is there in the system. We will not deal with this further but, that is what happens. Now, another interesting thing with this phase detector is, let us say you start off with the reference leading the feedback like this. So, let me erase this and show a case where reference is leading feedback. Qa will be 1 and let us say reference starts lagging the feedback and this point what happens is the feedback edge appears before reference edge.

So, Qa will remain at 0 and Qb will become 1 and it will do that. So, if you start with a small positive delta phi but, then make it negative, what happens is that the output will become negative because Qb becomes high and Qa will remain at 0 and on the negative side also lets you go on increasing the lag of the reference with respect to feedback. It will be periodic with 2 pi, minus 2 pi minus 4 pi and so on and there will be hysteresis any time. Let us start with a positive value and go in the other direction and here also there will be feedback if you go back in that direction. So, the characteristic will consist of these line segments.

It will be periodic with 2 pi if you keep on increasing or decreasing the phase monotonically but, if you go in the other direction there will be hysteresis. But, everywhere the slope will be Vpd by 2 pi. So, the hysteresis of is of some interest but

mainly what we must pay attention to know is the periodicity of the phase detector characteristic. As I said, the specific periodicity depends on the implementation but, every phase detector will be periodic because inherently faced by itself is periodic right? A phase of 2 phi plus delta is the same as a phase of delta. So, given this, there are some constraints on the PLL that come over. That is what we look at.

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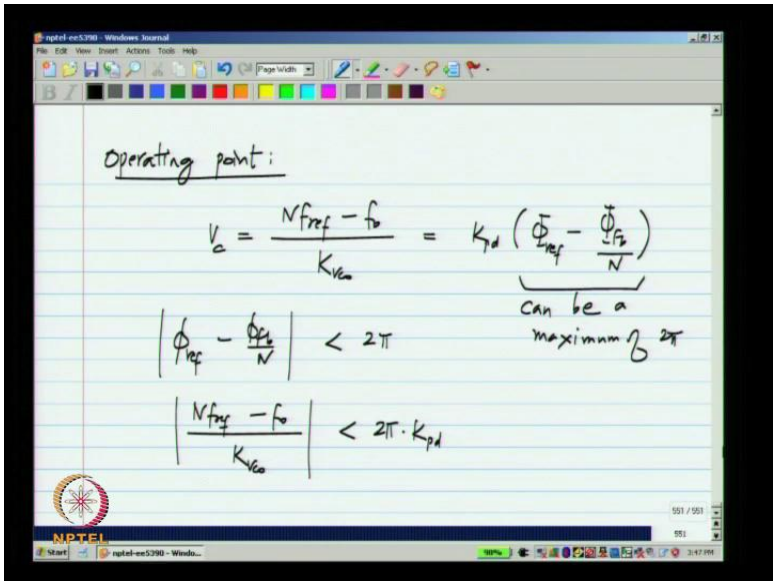

If you recall at the operating point, a control voltage had to be N f ref the output frequency minus the free running frequency divided by Kvco and it was also equal to Kpd times phi ref minus phi f b by N because it is detecting the phase difference between phi ref and phi f b by N. Now, this phase difference what is detected by the phase detector can be a maximum of 2 pi in our case. So, what does that mean? The maximum magnitude of this can be only 2 pi so; that means, that in f ref minus f naught divided by Kvco, the magnitude of that can only be less than 2 pi times Kpd.

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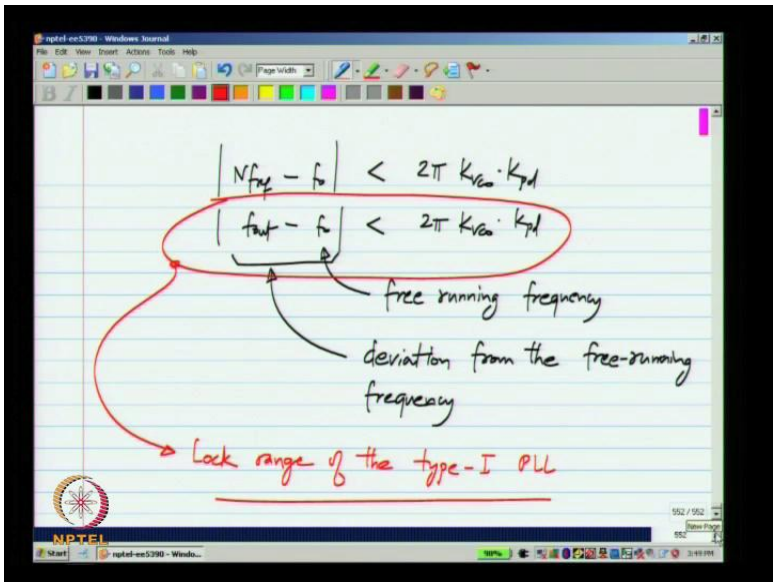

In other words, in N f ref that this is nothing other than f out, this has to be less than 2 pi times Kvco times Kpd. So, this is the free running frequency of the Vco and this is nothing but this absolute value of f out minus f naught is the deviation from the free running frequency. So, what this expression is saying is that the Vco will have a certain free running frequency and the phase locked loop will be able to adjust the output frequency to be n times the reference frequency, but only as long as the deviation from the free running frequency is 2 pi times Kvco times Kpd or less than that and this amount is known as the lock range of the phase lock loop and the lock range of the type 1 phase lock loop is given by this particular expression.

So, what this expression denotes is nothing but lock range of the type 1 PLL. Now, please keep this in mind and from this it appears that to increase the lock range which is the desirable thing to do you would like the output to be changed over a wide range. For instance if you have mobile phone or a radio, you would want to switch to many different channels.

And similarly you may want to vary the clock of a microprocessor over a wide range to save power or operate faster and so on. So, in order to have a wide range you need to maximize the value of 2 pi times Kvco times Kpd. That is increase the gain of the phase detector and the gain of the Vcd. Now, there is another aspect of the phase detector that brings in a completely different constraint that we will look at now.

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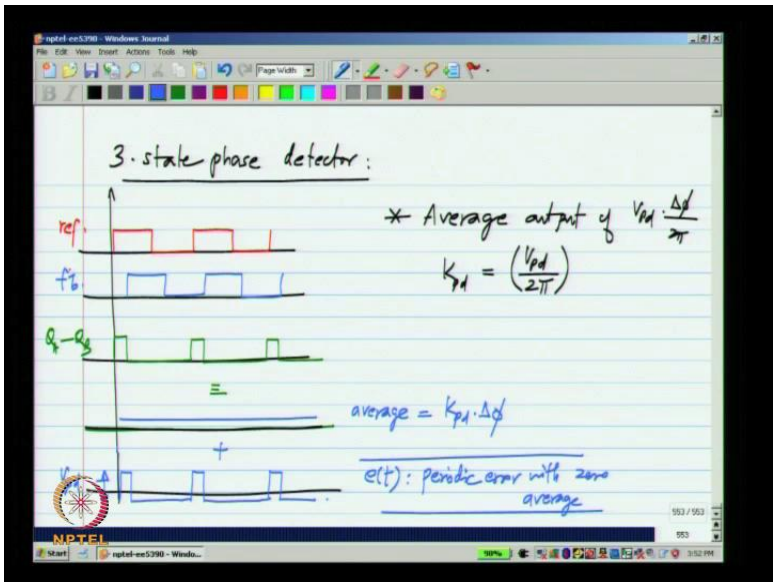

Our phrase detector, 3 state phase detector what it has is an average output of Vpd delta phi by 2 pi. This means that the phase detector gain Kpd is Vpd divided by 2 pi and that is only the average output as we know. Let's say again that reference is leading feedback. The output will not consist only of this average but, it will be this time wearing wave form. It looks like that. Here by the output I mean Qa minus Qb and this can be written as the sum of its average value which is equal to Kpd times delta phi or Vpd by 2 times delta phi plus a time varying part with the 0 average. It looks like that. I will call this error signal a periodic error with 0 average and peak to peak value of this will be Vpd. The average value will be 0.

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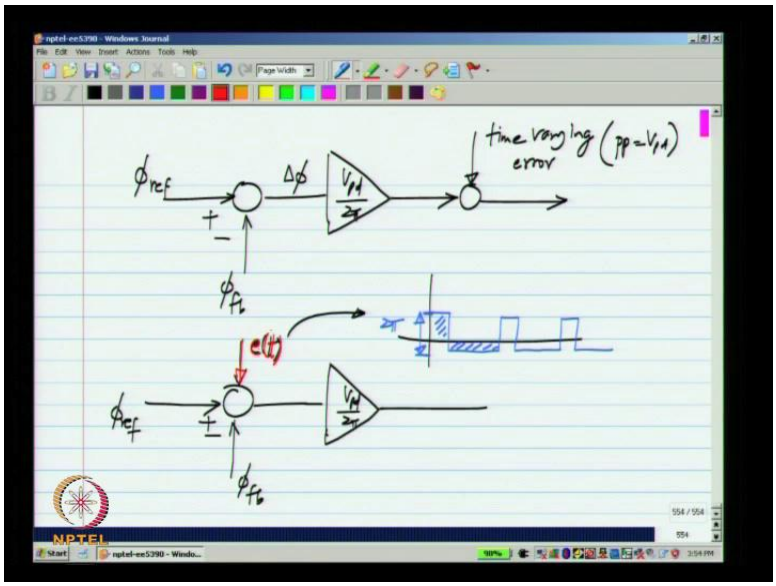

So, the actual representation of our 3 phase state detector is if you have let us say phi ref and phi f b it has a gain of Vpd by 2 pi. So, there is a phase difference is delta phi and the average output is Vpd by 2 phi. So, there will also be this time wearing error that is added to average output. This time varying error has peak to peak of Vpd and an average value of 0 and it has this rectangle wave shape.

Now, it is convenient to refer this time varying error to the input of this gain log because then the peak to peak here which is Vpd will be divided by the Vpd which is present in the gain and you will get something that is dimensionless. I can represent this equivalently as some e of t a. Difference between phi f and phi b will be delta phi. To that we have added Vf t and Vf t has a waveform like that which has these, are the peak to peak value of 2 phi. It has a zero average. That means that, the positive area equals the negative area.

So, the phase detector model consists of this error e of t in addition to the rest which is normally what we would like the phrase detector to be and this creates some problems for the phase locked loop because we see that even if the input is ideally periodic, there are some periodic disturbances created because of the inherent action of the phase detector. They quantitatively evaluate the effect of this disturbance in the next lecture and also evaluate the trade of between constraints imposed by this disturbance and also the constraints imposed by the lock range. What we will see is that we have to make

some refinements to the phase lock loop topology that we have and we also continue to do that.

Thank you. I will see you in the next lecture.