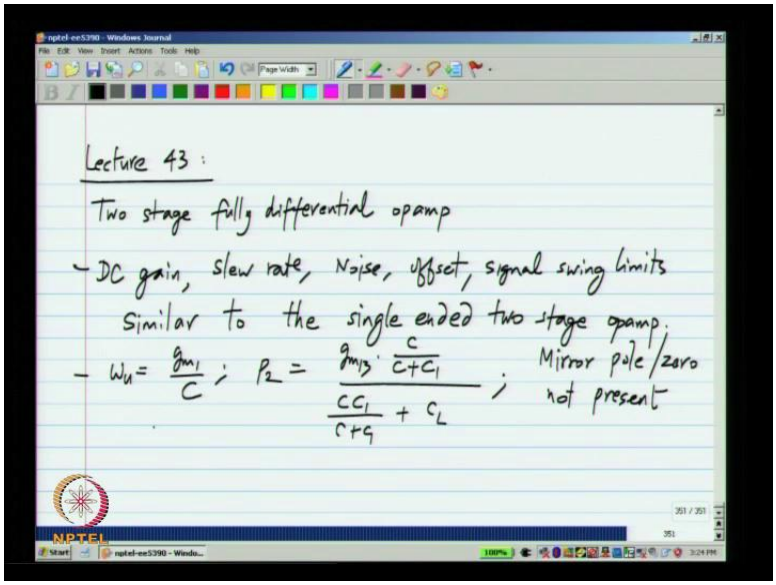
Analog Integrated Circuit Design
Prof. Nagendra Krishnapura
Department of Electrical Engineering
Indian Institute of Technology, Madras

Lecture - 43
Fully Differential Two Stage Opamp; Fully Differential Verses Pseudo-Differential Circuits

Hello and welcome to lecture forty three of analog integrated circuit designs. We were looking at fully differential two stage opamp. Now the differential half circuit of that consists of two common sources in cascade. So, it gives you the gain of two stages and the frequency response and other things are quite similar to like slew rate and so on or the same as what we would find in a two stage single handed opamp. The only difference is that the mirror pole and zero that appear in the single stage opamp do not appear in the two stage opamp, so the differential operation is by enlarging the same.

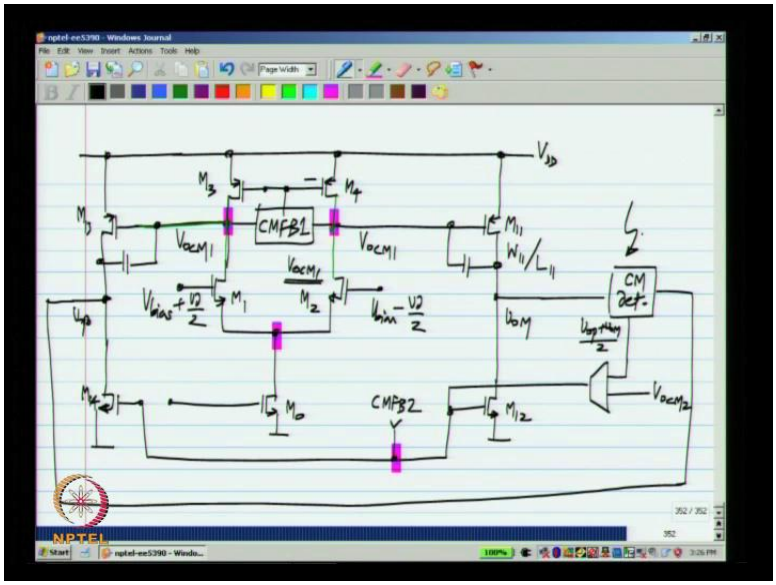
(Refer Slide Time: 00:55)



These all can be calculated for the fully differential case, but these will be similar to single handed two stage opamp. Now, the parasitic poles are also similar in that the unity gain frequency is g m 1 by C and the second pole is related to that. Except that, there will not be the mirror pole zero that is, the pole zero due to the current mirror is not present. Now, because of these reasons we would not discuss this further in perhaps a later

summary lecture, I will quickly summarise all these quantities. We will concentrate on the common mode feedback circuit for the fully differential two stage opamp.

(Refer Slide Time: 02:48)



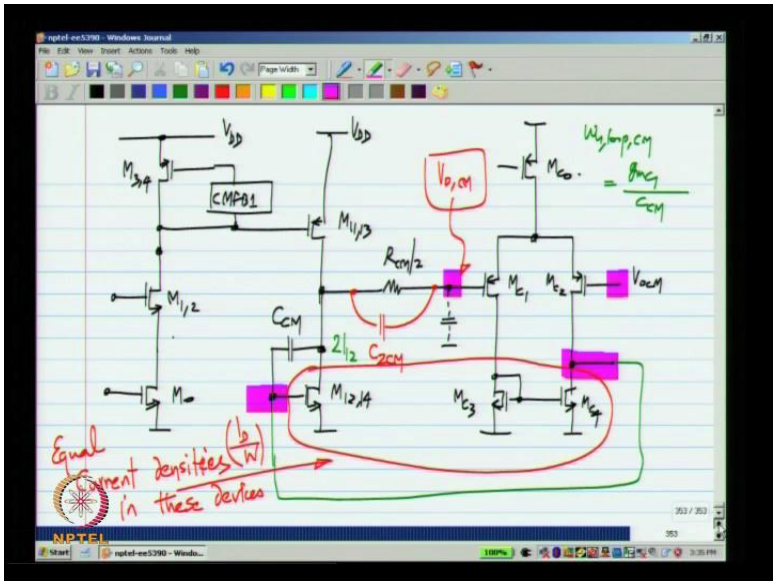
For now, I will assume that the first stages is independently stabilized using some circuit, which can be any one of the several circuits that we discussed while discussing the fully differential single stage opamp. Now, because the first stage is required to provide gain and if you have a resistible load here, it will compromise the gain of the opamp, severely. We will assume that the common mode feedback used for the first stage is one of those which do not have a resistive input. We will not use a resistive common mode detector, but we will use one of the other things either a buffered circuit or the circuit where we compare V o p and V o m separately with V o c m and so on.

Now, the active common mode detectors are usually non-linear, but if you consider a two stage opamp the output stage will have a large swing and the first stage output will have a relatively small swing. So, the non-linearity will not affect much and it is quite all right to use one of the active common mode detectors at the output of the first stage. For the second stage, basically we have to go on adjusting the gates of M 12 and M 14 and till V o p and V o m the common mode of that reaches the desired value. So, what do we do? What we need to do is to detect the common mode of the second stage that will give us V o p plus V o m by 2 and compare that with the desired common mode voltage V o c m 2 and apply it to CMFB2.

In this case what can we use for the common mode detector and if you observe while discussing the two stage opamp, I had said that the output can support a large swing. You have just one transistor at the top to the upper rail and one transistor at the bottom to the lower rail. Now, with these you get the maximum swing that is possible in a CMOS circuit that is, one we will site away from either of the rails. So, in this case we have to use a common mode detector that works with large single swings and really the only choice is the resistive common mode detector.

Now, this will add resistive load to the output of the two stage opamp, but a two stage opamp can handle resistive loads even if the gain of the second stage is compromised a little the first stage provides the bulk of the gain. So, it is to use a resistive two common mode detector with the two stage opamp. In fact, it is necessary to be able to support a high swing output. The trans-conductor that we use here is basically the single stage a single handed opamp.

(Refer Slide Time: 05:55)



What I will do now is to draw only the common mode equivalent circuit. This is the first stage M 1, 2 in parallel we have M 0 and we have M 3 and 4 in parallel. We have this first stage common mode feedback one. Here what I mean is the common mode have circuit corresponding to that one feeding it to M 3 and M 4 and the output of M 3 and M 4 is also connected to M 11 and M 13 and we have the loads M 12 and 14. So, we have the common mode detection and like I said we will use a resistive common mode

detector. So, we have R by two here I will call it R c m by 2 and that has to be compared with V o c m and fed back to the gates of M 12 and M 14.

Now, because we are feeding back to the gate of the NMOS the output of the single handed single stage opamp that is used for common mode feedback has to be able to support voltages closer to the lower rail. So, we cannot use an NMOS input here it is not suitable we will use a PMOS input stage with NMOS current mirror load and we have to complete the loop this. So, this forms the common mode feedback loop and for this for the loop gain to have an integrator like behave here the easiest thing to do, is to have an integrating capacitor over there. So, the equivalent picture looks like that of a two stage opamp except that we have a resistor in the middle.

Now because of parasitic capacitance is here, there can be a pole due to this resistor and that capacitor, which adds a lot of delay into the feedback loop. As usual we counter that by connecting a capacitor over there. So, as before the common mode feedback loop I mean this way I have seen in case of the fully differential single stage opamp the common mode feedback loop itself looks like a two stage single handed opamp in unity gain feedback. The first stage consists of the g m consisting of a form by M c 1 and M c 2 and the second stage consists of M 13 and M 14 which are basically the loads to the second stage in the differential picture.

Now again we know how to make this feedback loop nice and stable we know what it is unity feedback frequency is, so, I will not analyse that further the unity loop gain frequency of the common mode feedback circuit will be g M c 1, which essentially if you consider only this loop this is the first stage and that is the second stage divided by c, I mean to prevent confusion with the integrating capacitor in the differential picture. Let me call that C c m and I will rename these capacitors C z c m, just to imply that they introduce a zero into the loop gain and the dc loop gain of such a loop gain is quite high. So, we can expect that the common mode here will settle to something that is equal to V o c m.

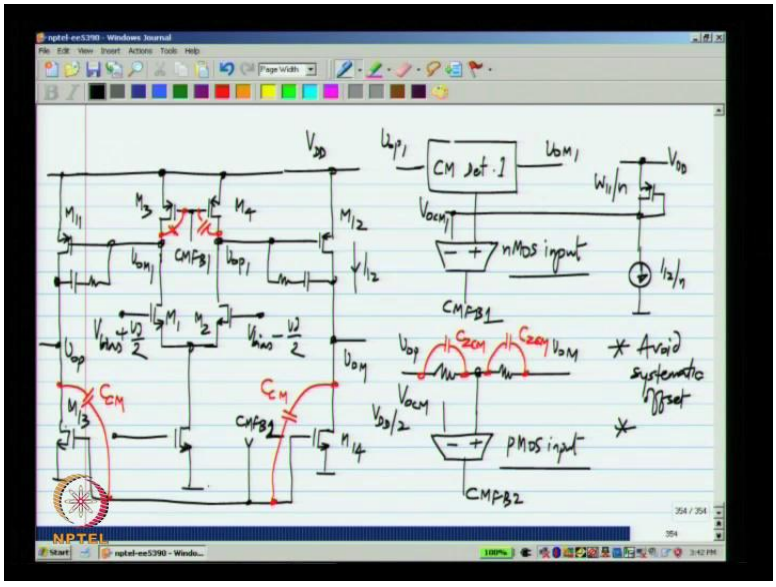
Now there is one other issue here that we discussed while discussing the single stage opamp. If the output of this when the loop is broken, let us say all the devices are identical if the output of this single stage opamp. Here is different from the voltage that is required at the gates of M 12 and M 14 to supply the desired current. Remember, the

current two times M 12 has to flow here in the common mode picture and that needs a certain voltage here. Now, if the voltage that comes out of this again we are assuming a fully symmetric here. So, the voltage will be same as V g s of M c 3.

That is different from the v g s required here when you connect it up this voltage has to shift and there will be a systematic off set between that node and that node. So, to avoid systematic offset, what we need to do is to have same current densities and equal current densities in these devices. When I say current density what I mean is the drain current divided by the width of the MOSFET. So, if that is the case then the voltage that we get out of this in the ideal condition equals the voltage that we need here.

So, when we connect it up the loop will stabilize with this voltage being exactly equal to that voltage. We extensively discuss the issue of systematic offset in the two stage single handed opamp and it is the same thing here. Now, did not mention that while discussing the fully differential single stage opamp, but even in that case you have to equalise the current densities in the trans-conductor used for common mode feedback and the load transistors used in the opamp, so this will stabilize to V o c m. So, as before for checking that the loop words properly you have to resort to simulation, you can simulate the loop gain you can also apply a common mode step and look at the step response. So, this is the way to stabilize a two stage fully differential opamp.

(Refer Slide Time: 13:21)



Let me try to draw the complete circuit here it is going to be very difficult, but just to show you the seeming complexity. The concepts are very simple, it is the same thing over and over; we have negative feedbacks everywhere the opamp itself is made. So, that it can be used in some negative feedback, but to make the opamp work properly you need two more negative feedbacks inside to stabilize the common mode voltages. This is the fully differential two stage opamp showing only the differential picture and these are the integrating capacitors and these are the outputs V o p and V o m.

I will call the outputs of the first stage V o p 1 and V o m 1, so we have to pass V o p 1 and V o m 1 to some common mode detector and compare its output to V o c m 1 and feed it back to CMFB 1. Now, as discussed earlier V o c m 1 must be derived from some replica bias that will establish the correct quiescent voltage at the output of the first stage and what is the meaning of the correct quiescent voltage; is the quiescent voltage that establishes the desired current in the second stage we need a certain quiescent current I twelve in the second stage. So, that can be done by having a scale replica of the output stage in the biasing branch.

This replica biasing is a very common thing that is used in analog circuits. For the second stage, we will invariably use the resistive divider though in some cases you could probably use something else if you are not concerned about swings. Again, you compared it with V o c m that is the common mode reference for the final output. Because, the final output goes very close to V D D and also comes fairly close to ground that is within one V D D in ground the output common mode voltage is frequently selected to be the half the supply voltage. Although this is not a sacred number and you could choose something else if that is required for now I will say this is V D D by 2.

Again this is also supplied to the second common mode feedback circuit and the way we have the structure M 3 and M 4 are PMOS devices. So, the trans-conductor that generates the first common mode feedback voltage must have an NMOS input that is when the levels will be compatible. Similarly, in the second stage we need to provide the feedback to the gates of and NMOS devices, so this should have a PMOS input. You need to mind the current density, so that you avoid systematic offset in both cases. And also you may have to use capacitors across the resistor to reduce delays in the common mode feedback loop.

Finally, you may have to use integrating capacitors for making the common mode feedback loop gain look like an integrator. This may be needed in both stages whether you need an explicit capacitor here or a capacitor elsewhere, it entirely depends on the bandwidth requirements and so on of the common mode feedback circuit. If you do add capacitors here they will load the differential picture, but you just have to live with it maybe you find some way of minimising the value of these capacitors and live with that. In this case each of the common mode feedback circuits for the first stage in the second stage will equivalently look like the feedback loop around a single and a two stage of opamp.

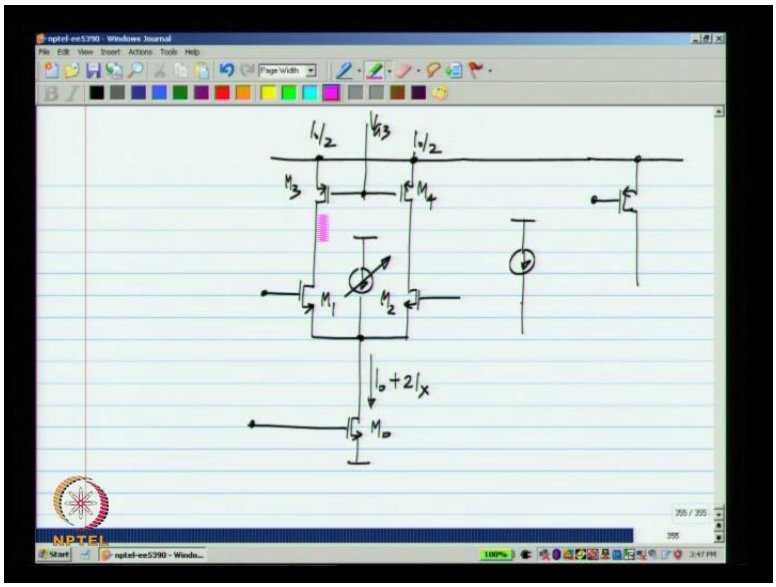
So, all the things that you can do with a single handed two stage opamp you can do here. For instance, you can add resistors in series with capacitors to cancel the right half plane zero in that feedback loop. In addition, you can also have resistors in series with integrating capacitors of the main opamp. Now, that is the rest of the fully differential two stage opamp we need to have a common mode feedbacks for both stages or find some way of stabilising the common mode voltages of two stages. Now, one thing I want to point out here is that you see that the circuit already has become. So, complicated that I cannot put all the transistors on his area that is available to me.

So, what does it mean it does not pay to memorise circuits to think of different circuits in an isolated fashion, here we have the main op amp which will be used in some feedback circuit, but to make the op amp work we have two more feedback circuits. Only way that you will clearly understand all of these things is if your first principles are solid. So, please pay attention to all of the loop gain and the basic feedback stuff with the single handed circuits and then you will be able to analyse something like this and also more importantly design something like this.

Now this is very important because in a given circuit you could have ten of these things. So, you just imagine the complexity we will never be able to put down the entire circuit on paper and the only way to even begin to make sense of it is by having a systematic approach. Now like before like with the single handed fully differential opamp, we have a choice of common mode feedback circuits available. Now as I mentioned there is just too much variety and I will not be able to go through all of them, but I will discuss one more interesting common mode feedback circuit that can be used for the first stage.

In this case it will become clear why it is suitable for the first stage for the second stage we will use the conventional one with a resistor common mode detector and feedback using another trans-conductor.

(Refer Slide Time: 21:25)

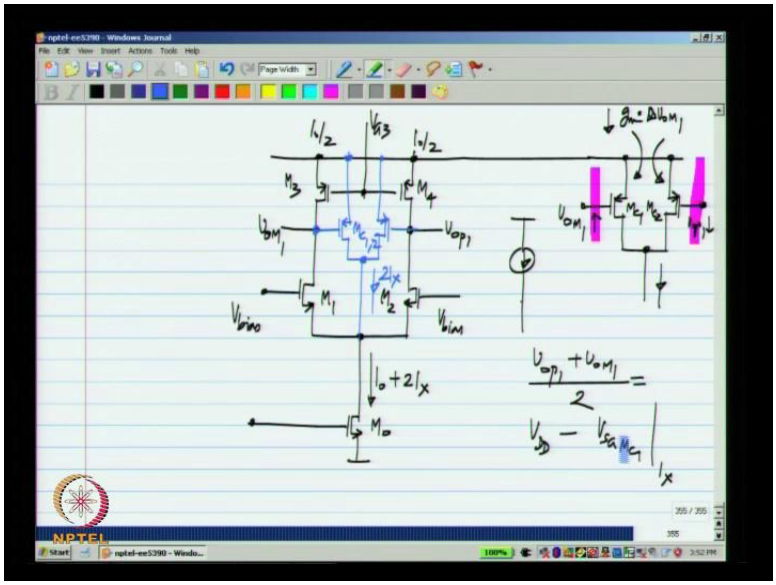


Let me draw only the first stage here now. So far whenever we stabilize the common mode of stage like this, the tail current was fixed and the currents on top were varying and it was varied by means of a feedback loop. So, that their sum exactly equals the current from the tail source. So, here we will do something different we will bias these with the fixed voltage V G 3 what I mean here is that it will be from some current mirror that is the current in this is not variable. It will always come from some circuit of this sort some replica and we will say that we have currents I naught by 2 in each of these branches, where I naught is the total tile current.

Now, what I can do is instead of the current from the top are fixed. So, I can vary the current at the bottom until the total current going into M 1 and M 2 equals the currents delivered from M 3 and M 4. Now, also the way I will choose to change the tail current is not by changing the gauge voltage of M 0 that is possible, but in this case I would not do that. What I will do is I will just make sure that the current in M 0 is more than I naught. So, let me call I naught plus two times sum I x. I will choose the transistor M 0 and the current in zero that way so that it is more than the desired current.

Then what I will do is I will take a portion of it and bleed of the tail that is I remove I ix from this current I will get exactly I naught. So, you can imagine that I can have a current source here, which is variable now I can go on varying this until the current that is flowing into M 1 and M 2 becomes equal to I naught. So, for that this current has to be equal to 2 I x. As before I do not know what the value of 2, I x is the only way I said this is by using negative feedback. Now, how can I make a current source that is that provides current that pumps out current, the easiest way to do that is by using a PMOS transistor.

(Refer Slide Time: 24:30)



Let me remove all of this I will level this V G 3. Now a current source like this which can source current can be implemented using a PMOS transistor with that gate bias to some voltage also when I have current like this and I want to make it variable, what is the quantity to which it should respond it is the common mode output of the first stage. So, always we look at the common mode output of a particular stage and based on that we vary the current until the current satisfies some particular condition; in this case it has to be equal to 2 I x more importantly M 1 and M 2 exactly equal to I naught. Now that is the total current should respond to V o p 1 plus V o m 1 by 2, in other words V o p 1 plus V o m 1.

Let me assume that this is V bias plus V D by 2 and that is V bias minus V D by 2. Now we also know that, the transistor here which I wanted to behave like a current source. In

the small signal sense it is a voltage control current source from the gate to drain and it has a linear relationship. Now, I will combine this with the fact that, I want the current source which should respond to V o p plus V o m by 2. So, what should I do then, remember the case where to detect the common mode we made some circuit for V o p and V o m separately and added up the currents I can do exactly the same here. So, let me call this V o m 1 and V o p 1 and I will add up the two currents.

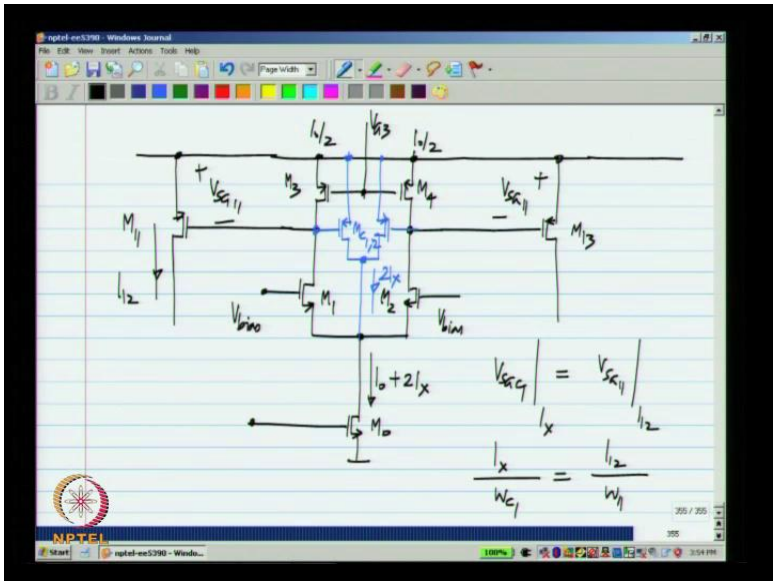
Now, what happens here is that let us say V o m 1 increases by a small amount and V o p one decreases by an equal amount. The current in this transistor will fall down by g m of this transistor times delta V o m 1 and the current and this will increase by exactly the same number. I am assuming these two transistors M c 1 and M c 2 are identical to each other and they have the same quiescent current. So, what happens is this current does not change at all if they vary in equal and opposite directions. So that means, that it does not respond to the differential of V o p and V o m, but it will respond to the common mode let us say both of them increase this current will reduce and if both of them reduce this current will increase.

Now what is that we want here if V o p 1 and V o m 1 are too high that means, that the currents from M 3 and M 4 are too much that is why their being pulled up what can we do from here the total current in M 1 and M 2 has to increase and for that this current source has to decrease. Now, if you look at what Ii described earlier if you increase both of these voltages the total current here will decrease. So, this just this structure is suitable for being used in this place. So, I will sum the two currents and connect it up there. Now, what I happens is that let us again imagine that there is no differential input by symmetry these two voltages will be equal.

Now, what will be the stabilised value of these two voltages the current in this has to be exactly equal 2 I x. So, the voltages here and there essentially the output common mode of the first stage V o c m 1 chance V o p 1 plus V o m 1 by 2 will be equal to V D D which is the upper rail voltage minus the gate source voltages of these two transistors. Let me call these mc one and two this is V D D minus V S G of M c 1 at a current of I x. These two currents are same and equal to I x. So, the total current is 2 I x. So, the output will get stabilised to V D D minus V S G of something. So, that is that is how the common mode stabilisation can be done for a single stage opamp; by the way this can be

used for the single stage opamp, but it is also very interesting for use in a two stage opamp.

(Refer Slide Time: 29: 45)

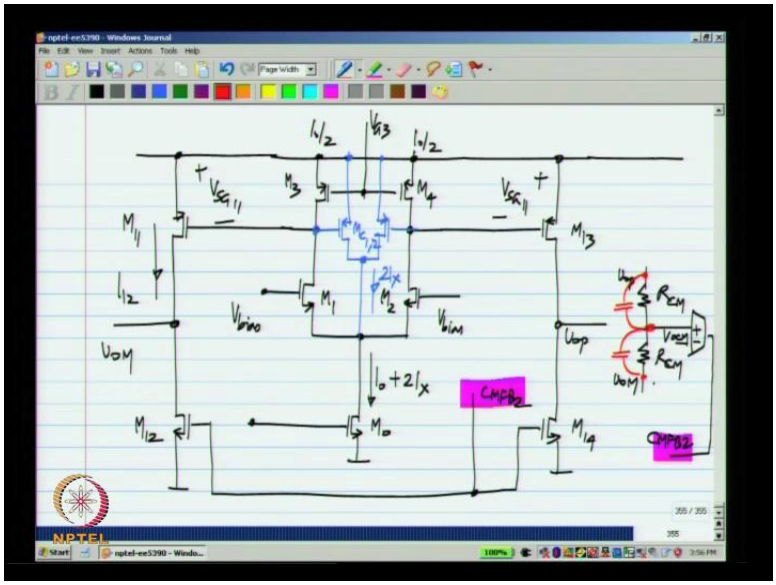


Now we do not need to do anything more than this. So, that is why this circuit is very simple and quite attractive. Now also in a two stage opamp, what happens is the outputs of the first stage, go to the second stage amplifier transistors M 11 and M 13 and the output common mode voltage should be such that M 11 and M 13 carry a certain current. Because M 11 and M 13 are biased by the common mode output voltage of the first stage so that means, that this has to carry some V S G, I will call V S G 11. Now, if you remember what I just said the output common mode voltage of a first stage will be V D D minus V S G M c 1 and M c 2. So, the voltage between V D D and this point is V S G c 1 at a current of I x; we want this to be equal to V S G 11 at a current of whatever is required that is I will call this I 12.

Now this is an extremely easy thing to do. So, for this to happen all we have to do is to make sure that M 11 M c 1 and 2 and M 13 have the same current densities that is in other words M c 1 and 2are replicas of M 11 and M 13. So what we need to do is I x divided by W c 1 should be the same as I twelve divided by W 11 and the same thing for of course, M c 2 and M 13. So, by using replica transistors of the transistors in the output stage, we can make a very simple common mode feedback circuit for the first stage. And

the output common mode voltage of the first stage will get set to the right value required to bias the second stage.

(Refer Slide time: 32:00)

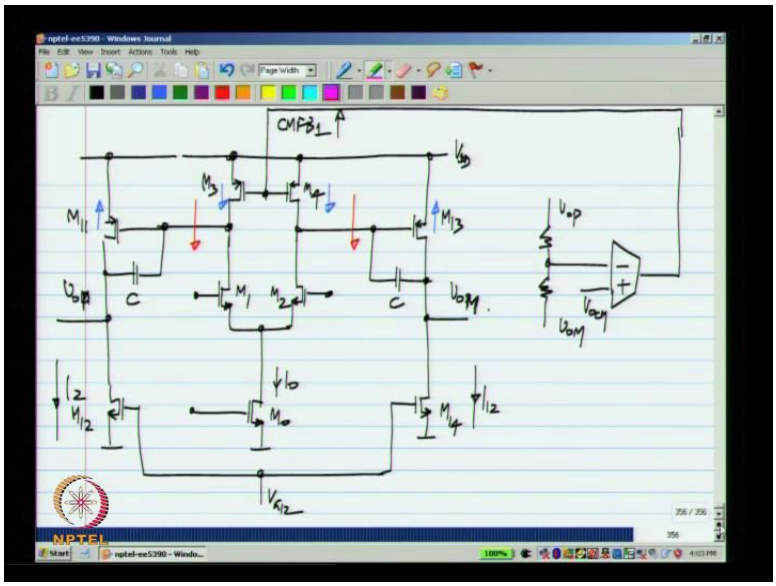


So, the main advantage of this kind of a biasing circuit is that we do not need any other circuit to generate a reference, simply by making these blue transistors replica of M 11 and M 13 we get the correct values of current in M 11 and M 13 now our job is not finished. We need to provide the common mode feedback to the second stage that is M 12 and M 14. So, that the output common mode voltage reaches the desired value. That we do in the usual way by using a resistor common mode detector comparing the output to some desired V o c m and feeding it back to CMFB2. So, this is same as that one now as usual we may have to use a capacitor here, so that the common mode detector works properly for high frequencies.

Now this is the exactly the same as what we were doing earlier. So, I would not go into the details of that again. So, far we have looked at a couple of ways of stabilizing the common mode voltages in a two stage opamp. All of them involve separately stabilising the first stage output common mode voltage and the second stage output common mode voltage. this is. In fact, the preferred way to do it there is a way to have a single loop that stabilises both common mode voltages we will look at that shortly, but it is a little more messy to stabilize and it is much simpler and generally does not cost much to stabilize the common mode of each stage separately. Now the first stage output common mode

voltage has to be of the right value to bias the second stage. So, that can be done by using replica transistors in one way or the other. The final output common mode voltage is usually close to V D D by 2, because in two stage opamp we are also generally interested in supporting a large output swing.

(Refer Slide Time: 34:07)



Let me consider the two stage fully differential opamp again. Let me go back to the topology where the current source here carries a current I naught, which is exactly the tail current required for the differential pair. Now, what we were earlier trying to do was or what we always try to do in common mode feedback is to make the currents from M 3 and M 4 equal to the current from M 0. Similarly, currents in M 11 and M 13 equal to the currents in M 12 and M 14. The way we went about it was we adjusted this current in M 3 and M 4. So, that it becomes equal to whatever is in M 0 and the current in M 11 and M 13 were set to some fixed values by adjusting the common mode output voltage of the first stage. Finally, using a second common mode feedback circuit we adjust at the current seen M 12 and M 14 to be equal to that of M 11 and M 13.

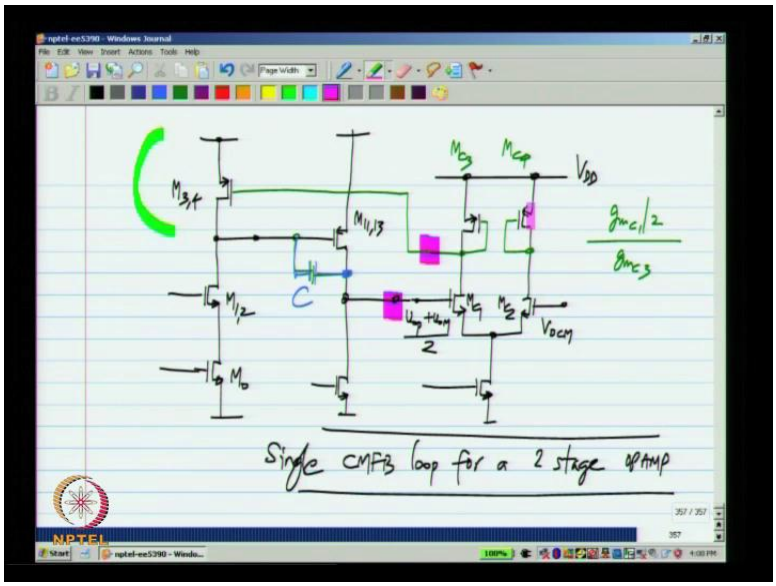
Now let us say we have fixed current sources at the bottom in the second stage. Let me call it V G 12. So, this means that a certain fixed current I 12 is going through both these transistors if they happen to be in the saturation region .Now what do we need to do the first stage remains the same I have to adjust this voltage until the current in M 3 and M 4 becomes equal to current in m zero. Now, the second stage the current in M 11 and M 13

must be made equal to that of M 12 and M 14. now how would we control the current in the current in transistors M 11 and M 13, if you observe let us say I change this voltage let me call that CMFB 1.

Now, what happens let say I increase this voltage the currents in M 3 and M 4 will reduce and the output voltage here will reduce because the currents in M 3 and M 4 will reduce these node voltages will be pulled down. Now because these voltages are pulled down the VSG of M 11 and M 13 are increasing. So, the currents in M 11 and M 13 will increase. So, you can see that this voltage CMFB 1 controls the current in M 3 and M 4 as well as the currents and M 11 and M 13. So, it looks like we do not need two nodes to control these two we can perhaps just control only this single voltage CMFB 1 and adjust the output common mode voltages stabilize the output common mode voltages of both the stages.

The way to do that is let us say this is V o p and V o m, we detect the common mode voltage as always using a resistive divider and compare this to a certain value V o c m and let the output continuously increase or decrease CMFB 1. Now what happens here is that let us say the output common mode voltage V o p and V o m the average of the two is too high, then what should happen is that the output voltage must be lowered so; that means, that the current in M 13 and M 11 must reduced; that means, these gate voltages must increase which in turn means that CMFB 1 must reduces. So, we need a trans-conductance of that polarity over there trans-conductance or an amplifier that is if V o p and V o m are too high this should be become small; V o p and V o m are too low this should become larger, by the way I should add the integrating capacitors.

(Refer Slide Time: 39:36)



Here, now in the common mode half circuit that let me redraw the common mode half circuit of this what I will have is, is that one we have R by 2 over there and V o c m. Now, you see that this feedback loop has a common source amplifier M 3, 4 another common source amplifiers M 11, 13 and this trans-conductor or an amplifier. Now, we have not yet said what amplifier it is, but if we use what we have been using all along that is a single handed single stage opamp will have three stages in feedback a single handed single stage opamp followed by a common source amplifier followed by another common source amplifier.

Now this looks like a three stage opamp and you know that a three stage opamp makes like a two integrated capacitors. So, it is a more complicated thing to stabilize a three stage opamp compared to a two stage opamp. So, we would not like to get into that complication. So, usually what is done is to use not an opamp in this place, but use a low gain amplifier. Normally, perhaps we would have used something like this. This gives the output and if we use this the main problem is that it is possible to use this something like that. So, then we need to have an integrating capacitor over there and then we need to have an integrating capacitor over there and the integrating capacitor of the main opamp will be over here.

Now all this becomes quite complicated to stabilize. So, what is normally done is not to use an opamp in this trans-conductor, but use some amplifier that has a positive

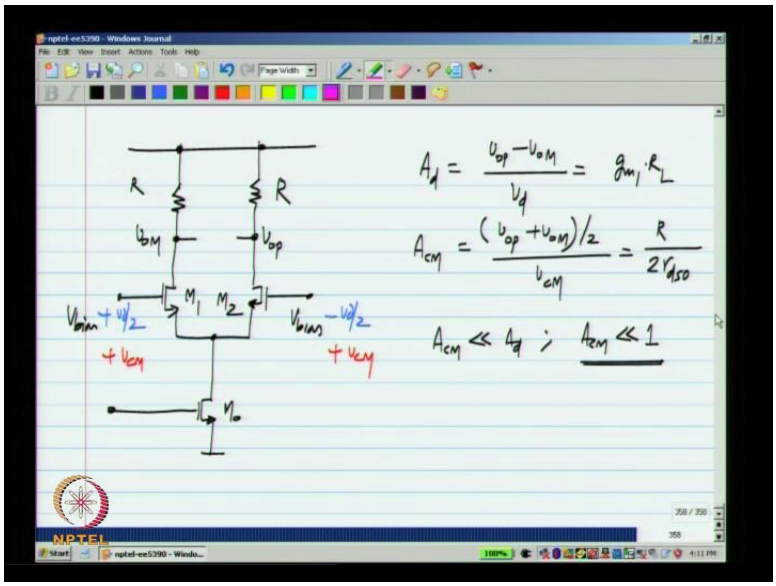
incremental gain and it is very easy to make a low gain amplifier all that is done is to do this. Now, you know that the diode connected transistors have an impedance of 1 by g m. Now, this is like a differential pair loaded by two resistors whose value is 1 over g m. If I call this M c 3 and M c 4 the gain from this point to that point will be simply g m c 1 divided by 2 divided by g m c 3. So, then the equivalent circuit will have a low gain amplifier with some parasitic pole and common source amplifier M 3, 4 and a common source amplifier M 11, 13.

Now this is lot easier to make stable and. In fact, many times the integrating capacitor used for the main opamp you see now that that also appears in this big feedback loop. So, let us imagine that the gain from here to there is almost 1, it is a ratio of g m it is close to 1 then we have this M 3, 4 and M 11, 13. So, the same integrating capacitor will also act as an integrating capacitor for the common mode feedback loop. So, it is possible to use a single common mode feedback loop for a two stage opamp; in that case you have to reduce the gain of the trans-conductor that you use. So, that you do not get into very complicated three stage stabilising networks, but also even if it is possible it is not very commonly done it is not advisable because now you have too many constraints you have some integrating capacitor for the main opamp for the differential picture.

You have to use the same thing for the stabilising the common mode feedback loop as well; that means, that the g m of M 3 four has to be constrained in some way. So, this just has too many constraints and it is usually much simpler to use separate common mode feedback circuits for the two stages of a two stage opamp. So, that kind of brings us to the end of common mode stabilisation circuits. Like I said there is a huge variety and in the exercises, there will be many problems that you can try and solve there are also lots of references on common mode feedback networks.

Now this can be extended further if you want three stage opamp with common mode stabilisation you can choose to stabilise the three stages separately; that is usually the easiest thing to do. Now what we will look at very quickly is the difference between truly fully differential circuit and simply putting two identical circuits next to each other. We have been talking about how differential circuits are good you transmit signals and two wires and measure the voltages between them and each wire acts as a reference for the other wire.

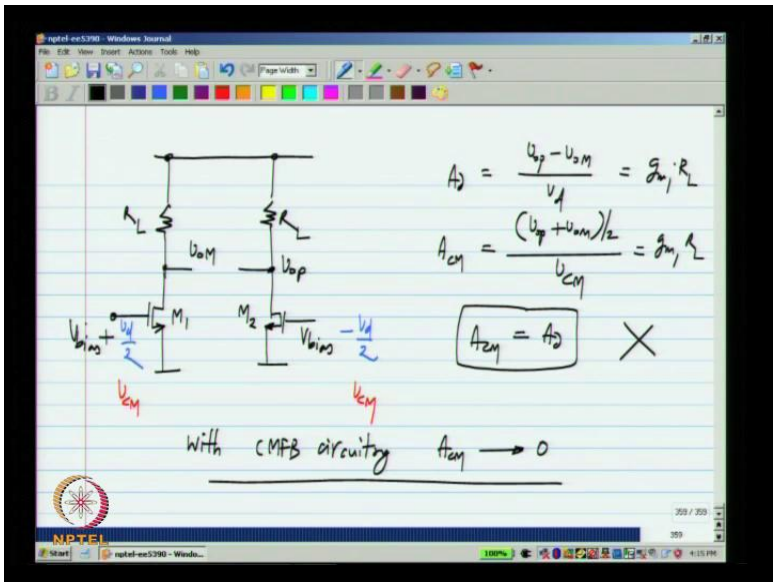
(Refer Slide Time: 45:51)



Now, the question that naturally occurs is, I said that this is a differential circuit I will show an ideal current source here, but even if with a real current source it works properly and to the bias I could have a differential input that is plus V d by 2 and minus V d by 2 or a common mode input plus V c m and plus v c m that may say the load resistors are the differential gain of this amplifier which is V o p minus V o m by V d. We know is g m 1 times r l a common mode gain of the amplifier which is V o p plus V o m by 2 divided by V c m.

This again we have worked out it is r by two times r d s 0. the important point here is the A c m is much much less than A d and also A c m is much much less than one it is required as well usually it is not enough to have it to be much smaller than A d, you also need it to be much smaller than 1. Now, this looks like we have already said that this differential pair is the differential version of a common source amplifier and that is reflected in the gain as well.

(Refer Slide Time: 47:47)



Now, let us say I just put two common source amplifiers next to each other and I apply some V wires. So, that it has the same g m as before and let us say I apply V d by 2 and minus V d by 2. We can also try applying a common mode voltage, what happens now? Let me call this V o p and this V o m the differential gain V o p minus V o m by V d equals g m 1 R L and if you look at the common mode gain which is V o p plus V o m by 2 divided by V c m that is also g m 1 R L because each circuit operates independently whether I have V c m here or V d and minus V d it does not matter, if I have equal voltages on two sides the output will still reduce.

So, in this case A d A c m equals A d. So, this basically is what makes the circuit useless for a fully differential operation, it is not enough to have two wires to carry the signal. So finally, you have to respond only to the difference between the voltages on the two wires that is the essence of two fully differential operations. So, if you have a chain of amplifier even if every stage does not have common mode rejection that is every stage does not have its differential gain much more than the common mode gain. There has to be something at least at the end which has sufficient common mode rejection. The differential pair is one such circuit now when you put two circuits together like this the common mode rejection is zero db; that is the differential gain and the common mode gain are the same and such circuits are known as pseudo-differential circuits.

Now, you can use pseudo-differential circuits, if you think about it the second stage of our fully differential opamp two stage opamp is a pseudo-differential circuit, we simply put two common source amplifiers together, but the reason the whole of opamp works is because we have two amplifiers in cascade and the first stage rejects the common mode signal. So, that is one thing also. Secondly, even the second stage has common mode feedback circuitry. So, now, if you let us say had current sources instead of these resistors and control those with common mode feedback circuitry A c m would become much smaller than A d.

Because, the whole idea of the common mode feedback circuitry is to hold the output common mode voltage constant so that means, that A c m should become zero with common mode feedback circuitry. In reality, it will be some small number we cannot simply put two circuits next to each other and use them as fully differential circuits. We will have to either have inherent common mode rejection like the differential pair does or we have to add the common mode feedback circuitry which will kill the output common mode signal or we have to do both.

Thank you. I will see you in the next lecture.