**Analog Integrated Circuit Design**
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**Lecture No - 42**
**Fully Differential Single Stage Opamp**

Hello and welcome to lecture 42 of analog integrated circuit design we are in the middle of discussion on common mode feedback circuits. The common mode feedback circuits can be very simple. In which case probably not much more is to be d1 the comp1nts in the opamp stabilize the common mode feedback loop as well sometimes, when the common mode feedback circuit is complicated. You help to take some special steps to stabilizes in a either case common mode equivalent circuits, the common mode half circuit its look like general feedback loop, which could look like either one or two stage opamp. We are seen examples of both. So, in this lecture what will do is look at some other case of common mode detectors and see how to use them in feedback.

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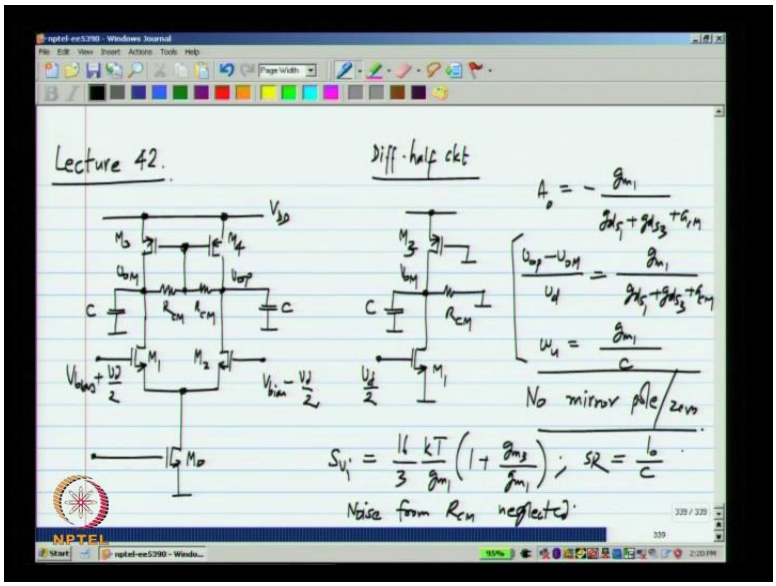


So, for as the big review of very simple, this fully differential single stage opamp, when this part is the trans-conductor and when loaded by capacitors it becomes an opamp. These are the two register are the common mode feedback detectors. Now the differential equivalent circuit is very simple. So, the differential equivalent circuit, the differential half circuit as a dc gain that is from V d by 2 Vom of minus g m1 by g d s1

plus g d s 3 plus g c m. Now when you of the full circuit at this circuit you will get minus of Vo m with the fully differential expectation, and the gain remains the same that is the gain V o p minus Vo m divided by V d will be equal to g m1 by g d s1 plus g d s3 plus g c m. And the unity gain frequency will be g m1 by c.

The c includes the load capacitance that you have plus any parasitic capacitance occurring this load. Now In fact, this transfer function is simpler than what we had for the single stage single ended opamp. If you recall in the single stage single ended opamp, we took a current of M1 merited the output was taken from this side. Now, because the current mirror as some pole in its frequency response, half of the current was going through some pole, and other half will coming directly. So, we add this mirror pole and zero in the fully differential. A single stage opamp we do not have in such thing. So, that action were advantage of the fully differential single stage opamp and the other thing remains the same. Now the noise we already calculated the input referred noise turns out to be exactly the same of what we had in the single stage single ended opamp.

I am not going to work it out here, but we already looked at how to calculate the noise of the fully differential circuit from the differential half circuit. We just have to calculate the input referred speckled density or the output voltage noise speckled density, and then double it to get the corresponding quantity in the fully differential is circuit. So, in this case we also have R c m which creates noise, but I am neglected the noise from R c m. The slew rate will be I0 by c because all of I0 flows into M1 or M2, and the rate of change of the output voltage will be related to I0 and the capacitors c. And finally, the offset again will be similar to

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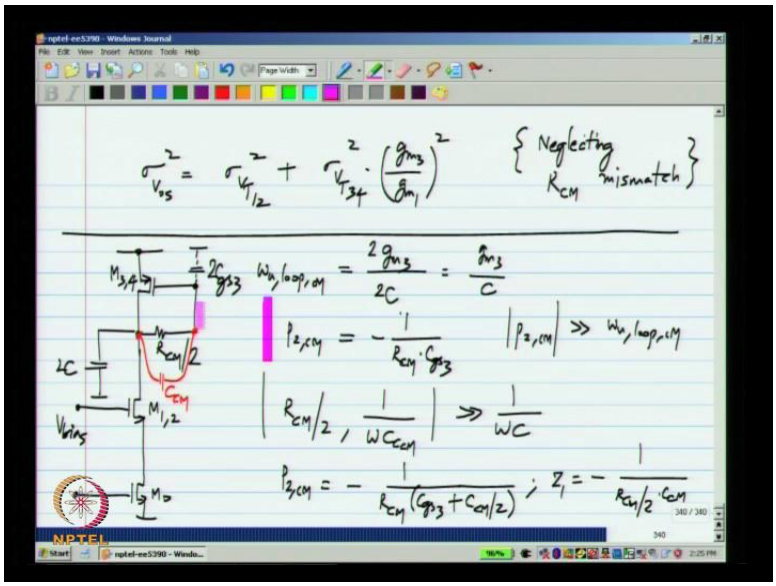


What we had in the single ended or single stage opamp, it will be equal to sigma VT 1square with this is the miss match between the transistor M1 and M2 plus the mismatch between the transistor that formed the load times g m3 by g m1 square. Again have negated the contributions from R the mismatch in R c m well contributed to the overall offset, but because the value of R c m. So, large that can be negated. And the common word off circuit of this which we also discussed earlier, there will be a parasitic. Here now in this loop the integrator is formed by the g M of M 3 and M4, and these capacitors 2c.

So, the unity gain frequency the common mode feedback loop is g m3 by c and there is parasitic pole. Due to this r and that c and this c is nothing, but 2 time's c g s3. So, this is and the left half plane of cause and minus for this is R c m by 2 R c m times c g s 3. And we would like this to be at a frequency much more than the unity loop gain frequency, otherwise what happens is when you have a common mode excitation the output will ring.

Now there is the way to fix this and that is to have the capacitors g c m across R c m that is, this the poll happens to be at a low in a frequency then, you will have ringing, you will have four phase margin in the common mode feedback loop, right to fix it. If you have this capacitors access zero has negative delay. So, in that case you can again calculate the poles and zeros. In the pole and zero calculation in this case is a little

complicated, but what I will assume is that, the impedance of R c m by 2 and the impedance of this C c m are much much more than the impedance of load capacitors. Because what happens when you have this coupled r c's, we have this r and then c, you will have some poles, which cannot be: related.

So, simply even this is an approximation when this part of the circuit as a very high impedance insignificant current is wrong from this and we can act as though this circuit is oscillated from that part. Now this is not the case then you have to go and calculated exactly. So, in this case you can calculated the pole and zero, and the zero is hat from all of this, you can calculate the phase margin in the loop gain function and make sure that it is sufficient. The many ways to calculate the stability of this, we have seen in circuit like, in other occasions like we can calculate the frequency response of a common source amplifier.

We have a similar circuit with a capacitance from the drain to ground, the capacitance from the gate to ground and a capacitance between gate and drain. We know where the poles are in such a situation, there will be poles splitting and so on. So, then we can calculate what the close loop poles will be, and whether the circuit is stable or not. And a simple feedback circuit like this is almost guarantee to be stable, we do not have to work too hard to make it stable or to eliminate ringing and thing.

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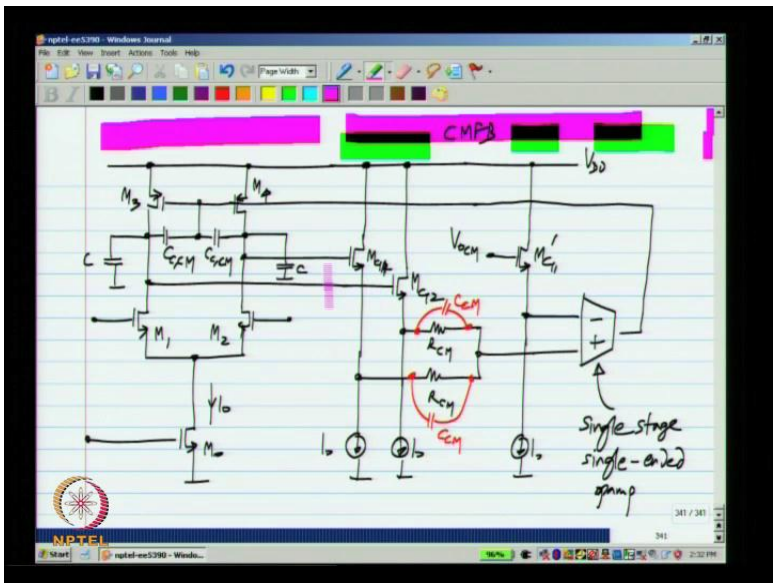

So, that now we have discussed other circuit quite extensively, that is when we have a fully differential circuit. Let me show it right here, we could make a common mode detectives with buffers. So, that the fully differential opamp is not loaded, and use trans conductor to complete the feedback. Previously had used the opamp symbol here, but it really a transconductor, you do not make a full place of opamp and this case. It is really a transconductor, but it as a high output resistance. Now, in this case when the common mode feedback loop works properly, the common mode of these two voltages will be said to V o c m. M c 11, M c 12 and this M c 11 prime are identical to each other.

They have this R c m and R c m. Here, we usually also have this capacitors C c m to make sure that there is an too much delay in the common mode feedback loop. We also have to a miller integrating capacitors in the common mode half circuit, it appears between the gate of M 34 and the drain.

So in the fully differential circuit, it will appear between the gate of M3 and M4, and each of the drains, something like this. And finally, the actual load of opamp will be here, c and c. So, now, the circuit looks very complicated, but it is not this part of it constitutes, if fully differential single stage opamp and M3 and M4 should act as common constant current source in differential mode. Now the rest of it for a common mode feedback, and this part is for detecting the common mode, this for the replica and this is for feeding the back to the gets an M3 and M4, and these are for stabilizing the common mode that is to make the loop gain of common mode feedback loop, look like an integrating function.

The many parasitic poles here, and also zeros and also in the implementation of this, which is the single stage single ended opamp. There will be parasitic poles and zeros and there have to be an adjusted. So, that we have sufficient phase margin in the common mode feedback loop gain. Now the moment you had this C c m in this portion, what happens is in the differential mode there will load the opamp, because in the differential mode this point is at ground and C c m will appearing parallel with c.

So, we have increase the load capacitance of the opamp, it will reduce the unity gain frequency, but we need the integrating capacitors or composition capacitors to make the common mode feedback loop stable. We need to have these capacitors and that will invertible add to the load capacitance we just have to lower than and if you minimize the

delays in other parts of the circuit, you do not need to large capacitors here, and they can be made as small as you wish, making you smaller will reduce the excess load on the opamp.

Now let us look a couple of different kinds of common mode detectors in general the scheme with every common mode detection and feedback is the same. You detect the common mode and you compared to some reference value, and then you feedback. Here, we needed a replica because the common mode detectors as this voltage drop V g s. Now, all of these can be merged to gather and comparison may not be; obviously, visible. That was the case with the simple circuit then not comparing, it with any reference that provides some outside, but the comparison is happening with the gate source voltage of the value of M3 and M4. So, the output common mode will set, itself to V DD minus the gate source voltages M3 and M4. Similarly this part, the single stage single ended opamp could be merged with the common mode detection. Let us see an example of that. Now for this illustration I will use the common mode detector without buffer.

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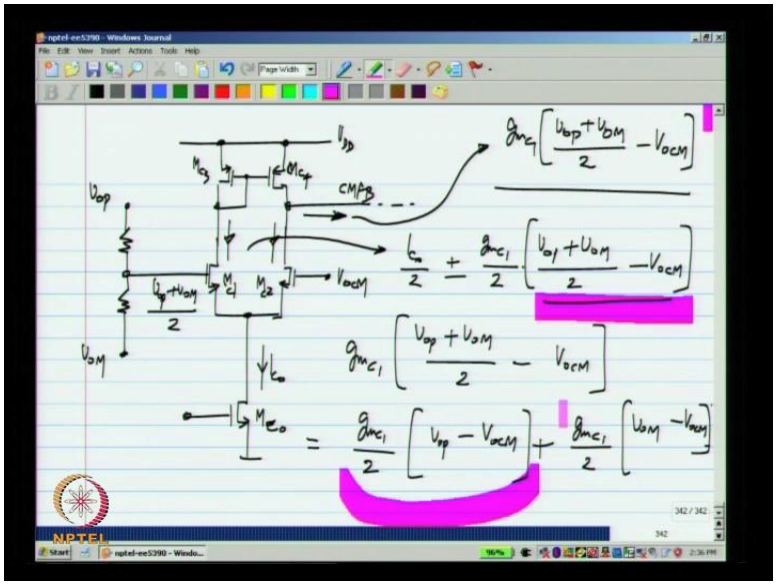

This is because it is just more complicated to draw, but you will get the point even without the buffer. The part that again I am going to drawn as is a common mode detector, itself plans the single stage single-handed opamp used for feedback. So, this is the common mode feedback that goes to M3 and M4.

These are Mc 0, Mc1, Mc2, Mc3, Mc4 for the current that gets pushed out of this can be calculated, the voltage at the gate of Mc 1 is V o p plus V o m by 2. And the current here and there will be let me call this Ic0. It will be Ic0 by 2 plus or minus g M c1 by 2 times V o p plus V o m by 2 minus V o c m. So this part of it input to the differential pair of Mc1 and MC2 that times g m c 1 by 2 is the current in each of these transistors and the total current output, and the bias component will be removed, and this will be a doubled. So, this will be nothing, but g M c1, V o p plus V o m by 2 minus V o c m.

The current that tends to flow here, if there is a load remember this is going to the gate of the transistors that start estate then there will be no current, there that is the current that tends to flow through the parasitic capacitance, that is at the particular load. Now any other circuit arrangements the gives us same current will work equally well between V o p and V o m and output current.

We need to have the same transfer function always can be do this. First of all we see that here, we have g M c1 times V o p plus V o m by 2 minus V o c m and this can be rewritten us g m c 1 by 2 V o p minus V o c m by 2 plus g m c 1 by 2 V o m minus V o c M. It has g m c 1 by 2 V o p minus V o c m plus g m c 1 by 2 V o m minus V o c m. So, now each of these is a certain different voltage this is between V o p and V o c m and between V o m and V o c m, we know that we can generate current which are of this form by passing this differential voltage to a differential pair.

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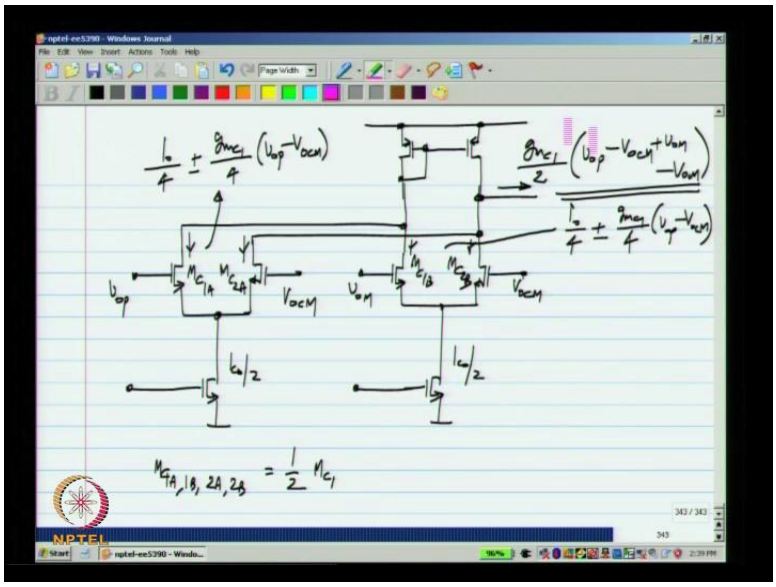

So, what I will do is, I will have 2 differential phase V o p and V o c M, V o m and V o c m. I add the currents, let us I have Ic0 by 2 flowing here, Ic0 by 2 flowing there and then these transistors. Let us see each of these transistors is half the size of the M c 1 used in the previous circuit.

So, we have half the current of before and half the otherwise as before when I say half of M c 1 half the width. The g M of these transistors is g m c 1 by 2. So, what happens is in each of these will be a differential current. Now these 2 currents will be I0 by 4 plus minus g m c 1 by 4 ,V o p minus V o c m and then these 2 transistors, it will be I 0 by 4 plus minus g m c 1 by 4 V o p minus V o c M. And we may or this current as usual then remove the bias component, and if you calculate the total current that tends to flow out of this. If there is a load capacitance are a voltage source will be the bias current sources will cancel out and we will have g m c 1 by 2, V o p minus V o c m plus V o m minus V o c m.

This is exactly the current that we had earlier we add this plus that one which gives you the same expression as this is the circuit, in which the common mode data exchange and the trans-conductor are merged together. What we have D1 is we have taken the single stage single ended opamp and splitter or the transistors pair into two parts, and also made the tile current half basically the differential pair is split into two half's, so each half as after g m s before.

The one of the differential pairs to apply V o p and V o c m to the other one we apply Vo m and V o c m. And finally, when you add up all the currents together, what you will get, you will be g m c 1 by 2 V o p plus V o m minus g M c times V o c m. This is exactly the quantity that we wanted. So, this circuit can also be used for common mode feedback circuitry and how do we used, let me V o p this over.

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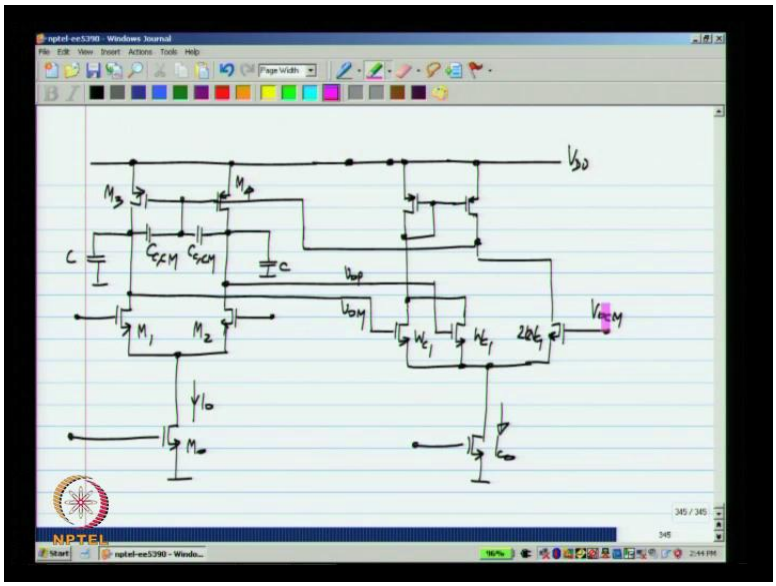

So, I will remove all of this step, this is one of the differential pairs and this is the other differential pair add up the two currents together and whether in to the other side. I also add up these two currents. And this is the output of a single ended opamp, which is used for common mode feedback. So we complete the feedback loop in this way the rest of the circuit remains this same. The Cc, cm is the integrating capacitors, if you want to think of it that way, alternatively you can think of it as providing feedback around M 3 and M4 high frequencies. For low frequencies the feedback goes through the complicated circuitry, which as high dc gain for high frequencies, the feedback around M3 and M4 is close through Cc, cm. This is V o p and that is V o m.

So, this also works equally well and again, because we have connected gates of MOSFET to the differential pair there is no resistive loading of the differential pair and the dc gain is not compromised. So, we can think of a lot of circuit like this, I will quickly discussed one minor variant, which is actually more frequently used. Now if you look at it imagine the quiescent condition, we are both V o p and V o m are equal to be Vo c m then this voltage and that voltage will be the same.

So, you can simply connect those together, that case you see that, this transistor and that transistor are in parallel the gate is be a Vo c m. The source is the same and the drives are also connected together. So, I will redraw this differently, I will show this to transistor like this and there are added together and this transistor, in which is twice the width. So,

this is w c1. And w c 1 this will be 2 w c 1 and the total current is Ic0. So, this circuit is the same when the opamp's is an quiescent condition.

When the V o p and V o m are equal to V o c m, when it turns out that this circuit has some advantages, when V o p and V o m are different from V o c m. How the circuit behaves and so on. It is somewhat are advantages to have this circuit with the two sources tried together than the previous one. So, this circuit is also use quite of and it has the same benefits of not loading the differential opamp. It does not load the opamp in the differential pictures.

So, this also some circuit, which as a merge in which the common mode detection and the trans-conductor tends or merged together. Now, there is the use variety of the common mode feedback circuit and you can think of your own circuit as well. So, I will not going to the details all of that, we have looked at a couple of them and we will use it for a two-stage opamp as well. There is one more common mode feedback circuit that will discussed, but in general the principle of in the following that you have two current sources 1 on top 1 on the bottom. And you have to adjust one of them. So, we need a variable current source and one easy way of doing that is to have a most transistor and various get voltage that is what we went doing so far.

So, there are many other variants as well you can have a degenerated current sources and vary the degeneration resistance that gives you yet another type of common mode feedback circuit. And similarly, the common mode detection and wave you amplify the difference between the detected common mode and the reference voltage can be very different.

So, by combining all of these you can easily come off with many many common mode feedback circuits. Now, exactly which one you use depends on details like the signal range over, which the circuits operates how stable they are, and how fast they are. So, on we have discussed the single stage fully differential opamp, a quite extensively. Now the differential picture is extremely simple. In fact, it is a simpler then the single ended single stage opamp, because the mirror pole and zero go away and this behaves like a truly single pole system with the pole very close to the origin. That is its behaves more or less like an integrator and all the other differential characteristics also we have calculated.

Now, what we will do is go on to the two-stage opamp, which we said was improvement over the single stage of opamp I am not going to discuss the cascaded opamp's in a details, the cascaded opamp are nothing, but single stage opamp with each transistor replaced by cascaded transistor. So, the common mode feedback was exactly in the same way were cascaded amplifiers as it does for the simple and deferential pair opamp. And all the arguments that we made so for apply also to the cascade amplifier.

Further, you can make either the telescopic cascade or the folded cascade fully differential very easily. All you have to do it is to add a common feedback circuit in the manner that we just described and as with a single size opamp. If you have resistive loading, because of the common mode detection circuitry that will compromise the dc gain your constraint to use common mode detectors, which present a high impedance that is basically gate of a MOS transistor. So, besides that there is nothing special about common mode feedback circuit for telescopic and folded cascade amplifiers. I am assuming that you will be able to work it out yourself.

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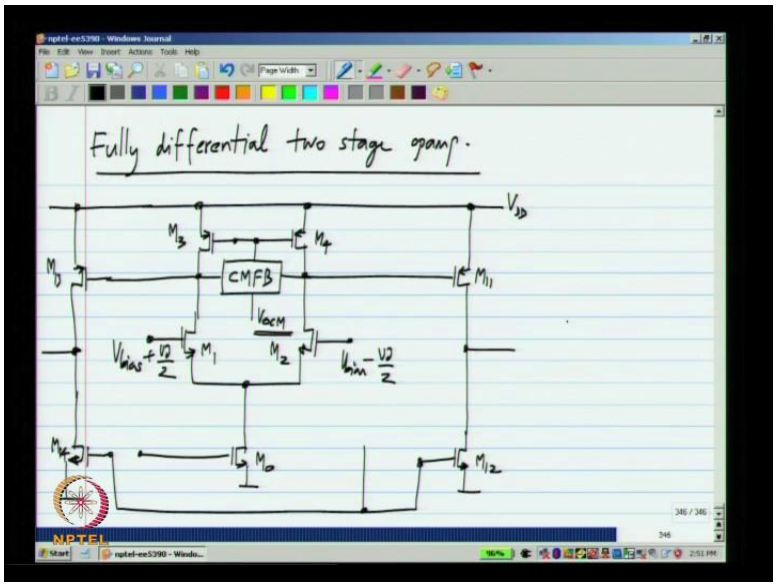


Now, we will go on to fully differential two-stage opamp. Let me first draw the single ended two stage opamp. This is the first stage with a differential input and the second stage is common source amplifiers and we can connect some load to this point. Now when we make it fully differential the output also must be differential. So, first of all the first stage will not be a differential to single ended converting stage like this. It will also

be fully differential that is the inputs and outputs are fully differential. And we make the second stage differential, we need to add a counter part to M11 let me call it M13 and this is M14. And the bios for this as to be properly adjusted that the currents from these to equal the current in this, similarly bios for M12and M14 as to be properly adjusted.

So, that the currents from M12 and M14 exactly equal the currents in M11 and M 13 and than using common mode feedback. So, what I have, here is a fully differential two-stage opamp, but showing only the differential signal path components.

I will not added common mode feedback circuitry. Now, we need common mode feedback to the first stage and the second stage. In both stages the current from the top and the currents from the bottom has to be exactly equal to each other. So, we will see, how to do that common mode feedback for this particular opamp. There are now many more options, one possibility is we starts with, a remember the first stage. This single stage fully differential opamp write this part of it. So, we can start with making the single stage fully differential opamp with common mode feedback that is, I will show this as a box, this box includes common mode detection and feedback. As you know finally, comes to the gates of M3 and M4. Now we look at the details of this, but the common mode feedback circuits.

We are discussed so for will work perfectly well. So, now the output common mode of the first stages stabilize. Now only thing to figure out is what the output common mode is stabilized to, that is the value of V o c m. Now, before let us say, we had this particular circuit in this case is the output common mode voltage will be equal to V o c m. What should be the value of V o c m, between discussed that. But it can a straight forward there will be certain output string limit for the fully differential opamp. Now V o c m should be in the middle for that range. So, that you can string the maximum possible, I did not discussed the string limits of the fully differential single stage opamp, but again it is quite simple.

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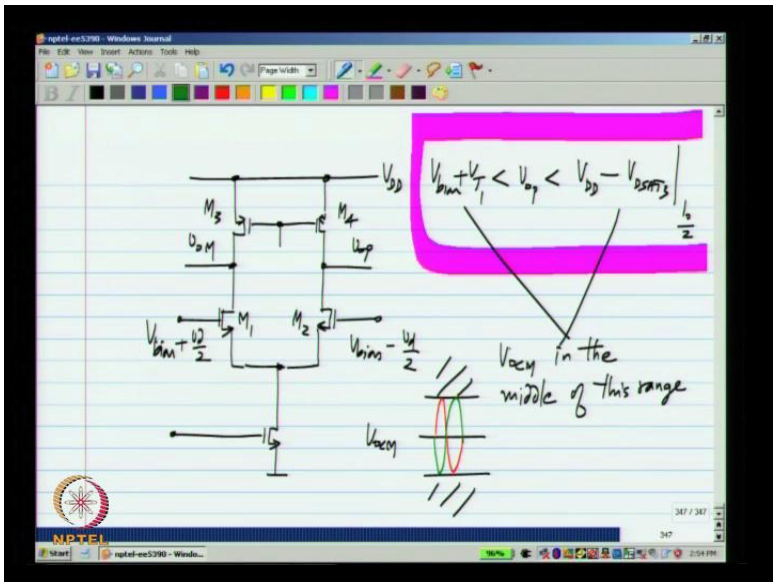


Not showing any of other details, this are yet will be operating. And outputs are here, we know that a V o p becomes very large, M4 goes into saturation and M 3 if V o m becomes very large. Similarly V o p becomes very small either M 1 and M 2 going to dried region that is a V o p becomes small try out region. And the limits are straight forward the limit on V o p is V DD minus V D sat 3 for a current of I0 by 2 on the upper side and on the lower side it is V bios plus VTof M 1 and M 2. I am assuming that the signals will V D is so small. So, it does not affect the limit. So, this is the case now, in quiescent condition V o p and V o m will be equal to V o c m. We should said V o c m to be in the middle of this range. So, that is V o c m and we have the maximum possible room for V o p and V o m that is the idea.

So, that is have select V o c m. Now we have the fully differential two-stage opamp and we assume that first stage as common mode feedback circuit that is the first stages the fully differential single stage opamp with its own common mode feedback circuit. Now what should be the quiescent and output voltage of the first stage.

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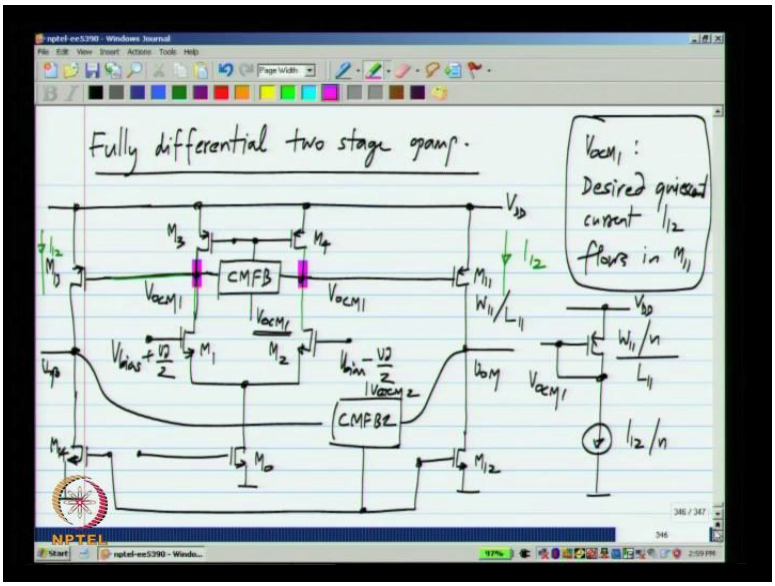


We need a certain bias current that it will in the second stage. The common mode voltage at the output of the first stage equal to the V o c m. And V o c m produce the certain current in M11 and M13 in the quiescent condition and that should be equal to the desired bias current in the second stage. I hope that this part is clear, in the single ended two stage opamp what happens is, we have differential pair with a current mirror and that drives a transistor M11 and M12 is a fixed current source. When you put the opamp in feedback, the current will M11 becomes equal to the fixed current source supply from the bottom, when you have the fully differential two-stage opamp, the situation will different.

Now, in this case the first stages is fully differential the single stage opamp and its output produce the certain current in M11and M13 and we should using another common mode feedback circuit make sure that M12 and M14 carry the same current. There are not current sources at the bottom in this particular arrangement of the two-stage opamp.

So, V o c m for the first aid let me call it V o c m 1. V o c m 1 must be such that the desired quiescent current I 12 flows in M 11 and outdo be produced that V o c m 1. So, let us say we make a replica of the M 11. Let us say M11 as a certain width by certain length, here we make let us say some multiple of that width divided by M 11 and V bios it with the current at 12 divided by n.

That is the desired current in M 11 is it well here, we put height well by n just to save of current, and then we also have a transistor is width is one over n times width of M11, and then we die out connected. This will provide V o c m because we know that if this V o c m, the voltage here were directly applied to the gate of M 11. The current in this would be the exactly equal to I12, the desired value of I12. Now this not directly applied to M 11 what is happening is this V o c m goes to the common mode feedback circuit, and the value here and there in quiescent condition when VD is zero will be equal to V o c m and that will give us the desired current.

So, basically this V o c m is not something that we independently said to be some absolute voltage, but we derive weight using a transistor level circuit. So, this is another example of replica. We have to adjust V o c m. So, that the output stage carry the certain current and we contributed to the voltage source and adjusted to hope to give the right current, because changes in transistor threshold voltage, and current factor will give you different currents, will you bias the gated it of its fixed volts. So, you have bias due to the current mirror basically. So, that is all that there. Now that V o c m 1 is derived like this, let me correct these things its V o c m 1, the output as to be again common mode stabilize. The output says, the gate voltage of the M 12 and M 14 must be adjusted using and other common mode feedback loop.

And, what is this now, it calculate the common mode voltage of the output. Let us say, this is V o p and V o m and it will add some common mode voltage, which will set the output common mode voltage to the desired value and what is the desired value again, we look at the signal string limit of the output stage, and we said the common mode voltage V o c m 2 to be in the middle of that stage. Now, we will see out to realize this common mode feedback circuit. Now before we go into the details of the common mode feedback circuit of the two-stage opamp.

Let us quickly go through the differential half circuit of the two-stage opamp. To avoid clutter, I will remove the common mode feedback circuits from this, we know that the common mode feedback circuits do not play a role in the differential picture them and add low to the differential picture, but that is about it. this is the point to which we apply the common mode feedback of the first stage and here is the common mode feedback of the second stage.

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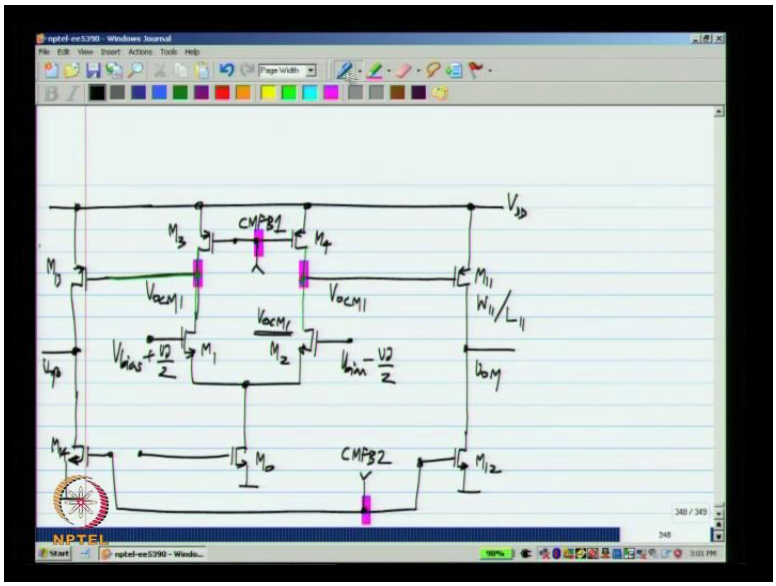


Now in the differential of circular what do, we have this point to be ground and that point to be ground and also this point to be ground.

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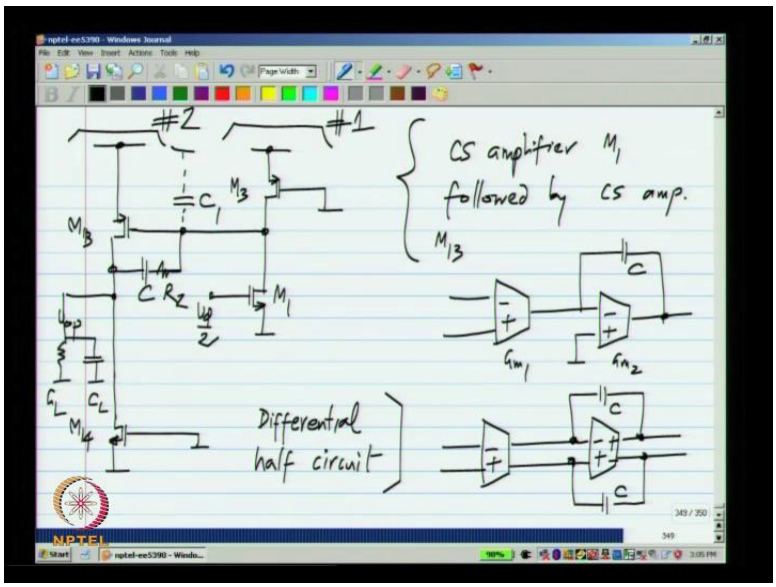


So, we will have M 1 with its sources grounded M3 with its gate grounded and this is M13 and M14. So, this is the output. So, this is the posting input V d by 2 and this is the output V o p, this is the differential half circuit of the fully differential two-stage opamp, this is the first stage and here, we have the second stage. As before the differential half circuit is extremely simple, we have a common source amplifiers M 1 followed by

common source amplifier M13. Now to make this two-stage opamp, you need to have the integrating capacitor here that i been sure earlier, so that in the complete circuit it will appear here and then. In terms of transcended the single ended two-stage opamp, its like that, this is g m 1 and that is g m 2.

The fully differential one looks. So, it is just a fully differential version of the same circuit. So, this circuit is again extremely easy to analyze. Now, because of the symmetry we do not have the mirror pole and zero in the first stage in a single ended two stage opamp. You have that, because first half of the current is mirror, in this case you do not have that. So, the transfer function of this is lot cleaner than single ended two-stage opamp. Now I want workout these things, but you already know, we have analyze the extensively. The frequency response of a common source amplifier M 13 the capacitor c between its drain and gate.

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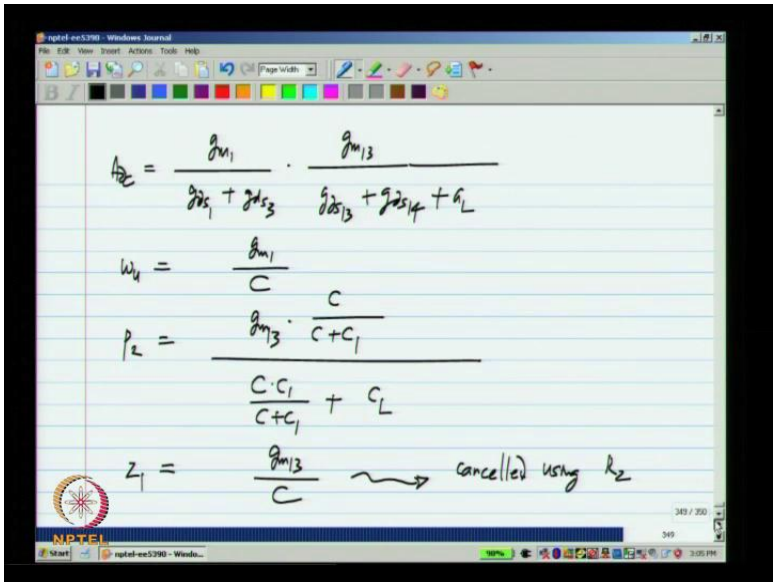


So, the dc gain of this will be, the gain of the first stage g M 1 by g d s 1 plus g d s 3 times that very easy to see in the half circuit. We have g M 1 loaded by g d s 1 and g d s3 times g M 13 divided by g d s13 and g d s14. I am assuming that, there could be some load here, which could g l and the unity gain frequency, of course will be g M 1 by c the non-dominant pole will at g M 13. C by C plus C 1, were C 1 is the parasitic capacitance, here that is the conductance due to M 13 being in feedback. I will neglect the other terms

associated with that, and then we have C c 1 is series plus any load capacitance that is connected.

So, we have a load conductance g l and the load capacitance c l. So, this is what we assumed in addition to this, we have an r h p right half plane zero which is at g m 13 by c, and this can be cancelled using r g that is using a resistance with series, with a integrating capacitance. So, the two-stage fully differential opamp is just a fully differential version that is, all we do the first stages is already almost differential it used the differential pair, but we do not use the current mirror load, be used the current source load. And the second stage you have replicated to the other side and we get the fully differential opamp. be gain and frequency response or are very similar to that of the single ended case. So, in the next lecture we look at how to do the common mode feedback stabilization for the fully differential two-stage opamp.

Thank you.