**Analog Integrated Circuit Design**
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**Lecture No - 41**
**Common Mode Feedback**

Hello welcome to lecture forty one of analog integrated circuit design. we have been discussing fully differential op-amp, fully differential circuit have a lot of advantages like immunity to noise and also that they cause less noise, and interference to other circuits. So, that is why most of the circuits today are fully differential. Now, when you make a circuit fully differential you need to have a common mode feedback loop to stabilize the output common mode voltage. This is true of any circuit that you think of and every circuit that we have discussed.

So, far can be turned into a fully differential version like the trans-conductor or the single stage op-amp, two stage op-amp, three stage anything that you take, but each of this stages needs a common mode feedback circuit and sometimes like let us say two stage op-amp we need to common mode feedback circuits one for each stage of the op-amp. So, we need to understand common mode feedback circuit very well, we will first do that with the single stage op-amp, because the single stage op-amp circuits is simple we can discuss a number of ways of a compilation common mode feedback in that circuit, and then we can translate that to any other circuit that we want to build.

Now there is a great variety of common mode feedback circuits just like any other circuit just like op-amp topology there is a huge variety will not be discussing all of them, but will discuss a few interesting cases and you can consent the literature, and textbooks for a other possible common mode feedback circuit variants, but the basic principle behind all of them is the same you will always have two current sources sort of fighting each other one current source at the bottom and another at the top, and this is necessary in order to have a very high impedance, which is what gives you very high gain, but if you just leave it like that, because of small mismatches in the current and the high impedance the voltage will either go to somewhere near VDD or somewhere near ground and the transistors will no longer work in saturation region. We have to establish the common

mode or the bias voltage at some desired value somewhere in the between the supplier else.

So, that the transistors are in saturation and that is why we have the common mode feedback circuit. So, the job of the common mode feedback circuit is to adjust one of the current sources using negative feedback. So, that exactly matches the value of the other current sources now when I say one of the current sources we do not mean the individual current sources, but the some of the current sources in the two differential arms of the circuit. Now another way to think of common mode feedback circuit is that it provides a low impedance in the common mode.

What is mean by common mode and differential mode? If you apply two signal either voltages or current of equal magnitude and opposite sign that is differential mode, if you apply to voltages or current of equal magnitude and the same sign that is common mode. Now, when you apply a common mode signal it should appear like a low impedance circuit and when you apply a differential mode signal it should appear like a high impedance circuit, because four differential signal we need very high gain.

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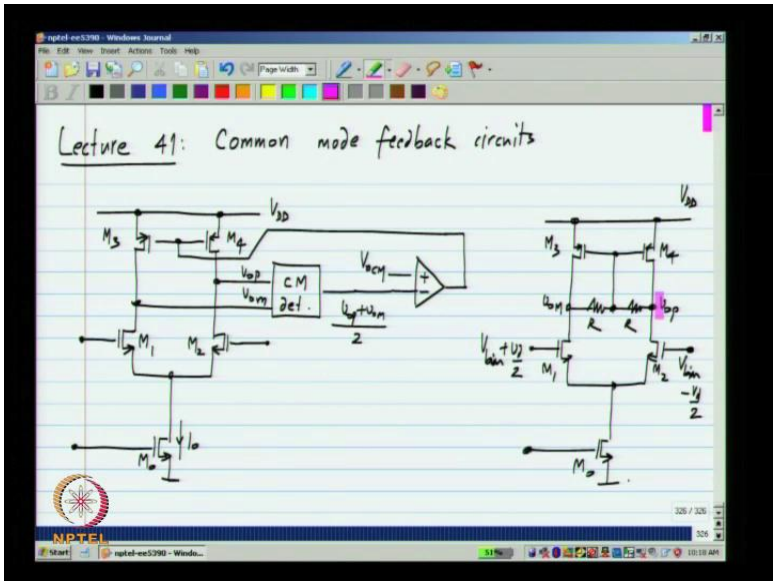


This is our single stage op-amp and the voltage here that the gate of M3 and M4 controls the values of the current sources from the top and at the tail i have assumed a fixed current source I naught, now the common mode feedback can be used either said this voltage or this voltage. So, that the tail current adjusted in this particular case i have

assumed that the tail current is fixed and we are adjusting the value of the current from the top.

Now a general representation of a common mode feedback circuit is like this, we have a common mode detector that is we have something that measures the common mode voltage compares it to a desired common mode voltage Vocm and continuously increases or decreases the gate of M3 and M4 in a direction such that the detected common mode voltage converges to the desired voltage Vocm, it is a classic negative feedback circuit. Now in this particular circuit, because increasing the gate voltage reduces the output common mode voltage V o p plus V o m by 2, the signs have to be of this for this particular op-amp. we also saw a very simple realization of the circuit were we did not have an explicit op-amp for comparison all we had was we made a common mode detector using a resistive divider of equal resistors.

Midpoint will be added Vop plus Vom by 2 they simply connected to the gates of the M4 and M4 now in this particular case the output common mode voltage will be stabilize to the gate voltage of M3 and M4 at a drain current off I naught by 2. When you apply a differential voltage what happens is that Vop will swing up let us say and Vom will swing down by an equal amount the average value does not change. So, the common mode feedback circuit does not react to differential signals that is a prerequisites of the common mode feedback circuit it should not react to differential signals the same thing happens here a Vop goes up Vom goes down by an equal amount this voltage does not change. So, the currents delivered by M3 and M4 do not change at all. Now only problem with something like this resistive common mode detector is that it always load the op-amp or whatever stage we are deducting the common mode…

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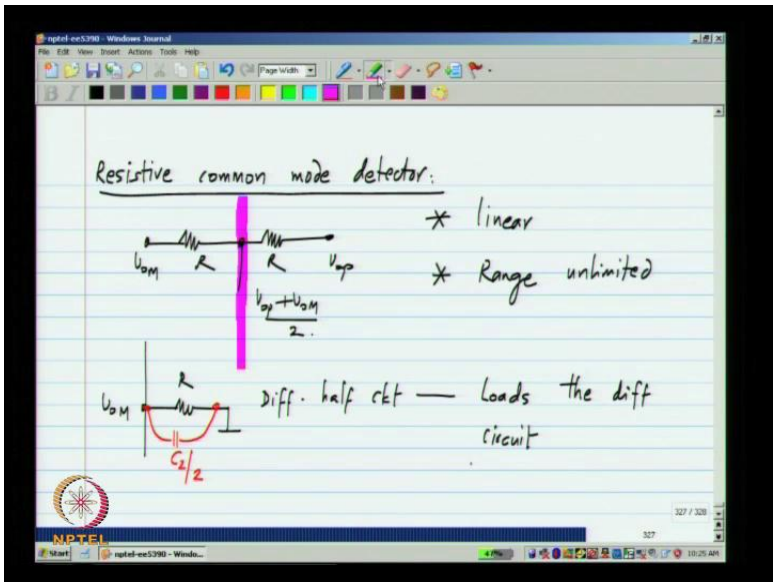


Now, the advantage of the resistive common mode detector like this is that more or less ideal we have Vop and Vom here, we get Vop plus Vom by 2 and first of all, because use resistors it is linear even for large swings of Vop and Vom and also its range is not limited, by itself Vop can swing to any value and Vom can swing to any value, and the midpoint of this will be Vop plus Vom by 2, but the disadvantage is that in the differential picture keep in mind this midpoint will be ground. So, we will have this in the differential half circuit. So, from the output to small signal ground they will be resistance R which will load the differential circuit.

So, while the resistive common mode detector is more or less ideal, it loads the differential circuit that is one disadvantage of it for instance you use it in a single stage op-amp, it will reduce the again. So, in order for it to not reduce the gain significantly the value of R must be as high as possible now there may be practical problems in achieving this, because if you want a high resistance you need to have a very long skinny resistance and that may take up a lot of area. So, that could be one practical problem and in any case even if you make large resistance you may not be able to make it much large then the Rds of the transistors, if you have a resistance R that is smaller than the Rds of the transistors, the dc gain will be dependent on R and not on the Rds of the transistors any j will not be able to achieve the maximum gain that is possible in a single stage op-amp. So, a resistive common mode detective is usually not used with the single stage op-amp.

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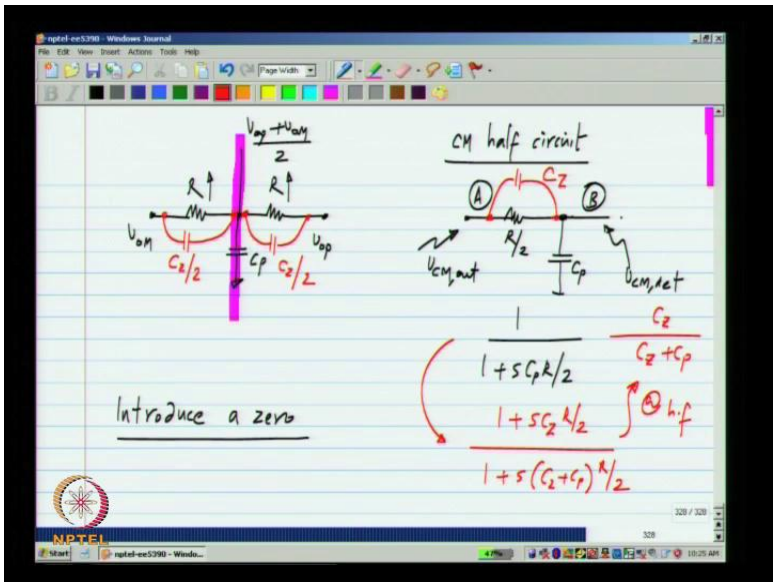


So, that is one think now there is another issue let say you go and making the resistance very large, what happens is there will be a parasitic capacitance from the midpoint this is Vom Vop here i get Vop plus Vom by 2 at dc . if you consider higher frequencies let see you go on increasing R just because you do not want to load the circuit what happens is that in the common mode half circuit let me draw the common mode half circuit of this ( refer time: 11:00) for that I simply take this is the line of symmetry, I simply take this side and fold it back on that side. So, I have a resistance R by two and C p and this is the detected common mode. So, here I have the common mode output and here I have the detected common mode, I has clear that for higher frequencies the detected common mode is not the same as this, because this is a low pass filter.

Now this can also be a problem now when we have this feedback loop, if you have a pole in the common mode detective that adds to parasitic delay as we know any parasitic pole adds to delay in the feedback loop and that can make this circuit on stable that can make this feedback loop on stable you not looked at the details of this feedback loop gain what will do the soon, but then any case you know that a negative feedback system cannot have to many extra delays. So, here the transfer function from this point to that point would be a first order loop as transfer function. So, if R is very large; obviously, the delay is very large or the low or the bandwidth of low pass filter very small how do we fix this we earlier seen that by introducing a zero, we can essentially present an advance that is a negative delay, and then counter the effect of the delay.

Now, how do we implement zero in this first-order low pass filter that is very easy, all we have to do is to connect some capacitance like this, let me just call that C z in this particular case the transfer function changes to from A to B it will be… So, at high frequencies it will simply be that of the capacitive divider is easiest to think of this as the capacitor C z is a short-circuit across R by 2 at very high frequencies. So, all you have is this capacitive divider you do not have the phase shift due to this RC circuit you simply have an at attenuation and the transfer function changes to C z by C z plus C p, if C z is comparable to C p this is some number some fraction of one and that is quite acceptable as long as it does not give a phase shift. So, that as many way to about think of this you can think of the zero providing a phase lead or a negative delay, but in any case this can be used to stabilize the circuit.

So; that means, that in the actual circuit remember this is only the common mode half circuit. So, in the actual circuit you need to have half of the capacitor across each of the resistor in the common mode detector. Now this is fine this can be done, but you see that this will also load the circuit. So, now, in the differential half circuit will have this load as well. So, in addition to the integrating capacitor and the load capacitors of the single stage op-amp we also have the capacitance used in the common mode detector. So that, the passive common mode detector is very useful, because it is linear, but it is some problem first of all it loads the circuit that is the main problem, but the advantages that it is very linear. So, we will see that there are some situation, where we will use this and in some cases were will try not to use this one now what is the alternative the one common thing whenever you are presented with a heavy load is to buffer it. So, that is one of the obvious solution.

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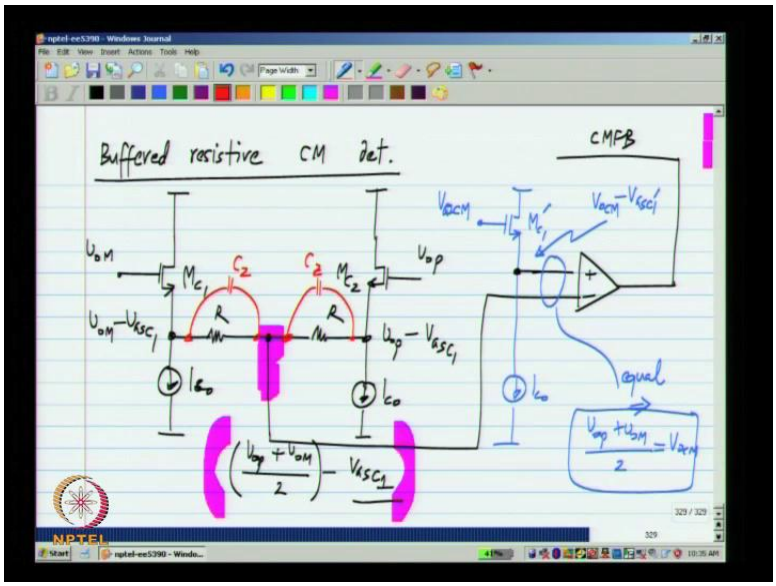


What is the buffer? We can use a source follower as a buffer, I will show it with an n-mos source follower we could also use p- mos, if the voltage ranges are compatible. So, let us say this is Vop and Vom and we have two source followers Mc1 and Mc2 this will be some Vop minus sum fixed voltage Vgsc1 and this will be Vom minus Vgsc1, I will assume that for now there is nobody effect in this transistors. So, the detector voltage here at the output will be Vop plus Vom by 2 minus Vgsc1. So, it is related to the common mode voltage, but it also has a level shift, which is same level shift of the source follower buffer. Now our circuit looks something like this we have to compare the detector common mode voltage to the desired common mode voltage and feed it back to a current source transistors.

I will simply label this CMFB a CMFB is nothing but this node i am only concentrating on this part of the circuit here now what happens is, if common mode feedback loop is stabilized, the detected a voltage here and this Vocm will be equal to each other after all this op-amp here is measuring the error between the two, and changing the common mode feedback voltage until this two become equal now this is a problem, because Vop plus Vom by 2 does not equal Vocm it will equal Vocm plus Vgsc1. Now, this Vgsc1 is an unknown quantity in that you can calculate it, if you know the parameter of the transistor and the current exactly, but you do not know that. So, you would in general like to avoid something like this, where you have the output common mode voltage dependent of n some Vgs that depends in turn on crosses variation.

Now, this kind of situation occurs very commonly in IC design as well you will have to deal with some quantities, which in principle can be calculated, but because the parameters of the most transistors varies across the process and temperature in these numbers also very quiet a lot now a very common technique in IC design to counter this is to exploit matching. It is very clear that instead of comparing the detected common mode voltage with Vocm, if i compared it with Vocm minus Vgsc1, i will get exactly what i wanted Vop plus Vom by 2 it will be equal to Vocm.

What i mean is? I should not do the comparison with Vocm, but Vocm minus Vgsc1. Now, how do I open in this Vgsc1 in this expression that is again very easy I use a replica of this particular circuit I will write that here again a different color is to make that clear. So, let me call this Mc1 prime and you use the same current we have call this I c naught these are also Ic naught and I connect it of there in the gate of this is connected to Vocm here what will get is Vocm minus Vgsc1 prime.

Now, this stage is a replica of these two stages source follower stages. So, Vgsc1 prime will be equal to Vgsc1. So, finally, when this two voltages become equal it implies that Vop plus Vom by 2 equals Vocm. Now, this business of exploiting matching on a integrated circuits is very very common. We have used it for simple circuit like current mirrors there are so many cases, where you have a two things to match very well you have to match all the parameters.

In that case you simply use a replica circuit, now that sounds weight have shown you one instant of it. So, whenever you have let us say voltage drops or some other parameters dependent on the most transistor characteristics you may be able to use a replica circuit. So, that the dependence on most parameters, which is also process dependent will be cancelled out, so this buffered resistive common mode detector clearly does not load Vop and Vom, because looking into the gates of Mc1 and Mc2, we have high impedances, but the problem now is that initially when we have only resistors the range was infinite I mean practically you could have Vop and Vom of any values.

Now, if Vop and Vom become very small there will derive this current source transistors into saturation we can find out for yourself what the limits are Ic naught this current sources are also implemented using most transistors and similarly, if it becomes very large Mc1 and Mc2 will go out of saturation into tryout region now that is not very

likely, because for a enhancement transistor with a positive threshold voltage Vop has to be about the supply voltage VDD for Mc2 to go into tryout region. So, that is not likely, but at least there is a lower limit. So, that is one problem.

So, will end up with some swing limit. Now secondly, this transistors will body effect, if you use p- mos you going you can avoid it, but as I have mentioned earlier even with the p- mos tying the substrate to the sources is not a very good idea, because it increases the parasitic capacitance and other sources greatly. So, if you do a body effect what happens is that this draught beer is not a constant as i have represented it is not just Vgsc1 on both sides, if Vop is larger and Vom is small the Vgs of Mc1 will be small and Mc2 will be larger. So, the level shift will depend on the absolute value of Vop and Vom.

So, you will get some nonlinearity in the detected common mode now this is a very common effect with any active circuit and with the active common mode deduction circuit the same problem will apply, but if you expect the swings here to be small this kind of circuit can be used. Now, what is the problem with a nonlinearity in a common mode detector the problem is that once the circuit becomes non-linear it will not react only to the common mode Vop plus Vom by 2, in general it'll be some non-linear function of Vop and Vom.

So, you will have some response to the differential component of the circuit as well and that is not good a it turns out that, if you have some nonlinearity in a common mode feedback circuit that will be an even order nonlinearity, because of the symmetry of the circuit and even order nonlinearity combine with some mismatch in the circuit can give you a even order harmonic in the output of the circuit.

Now, this is a very general description for details you have to look at a specific circuits, but what you can expect from nonlinearity in common mode feedback circuit and combined with mismatch in the differential part of the circuit is that you will have even order distortion. A fully differential circuits it should have no even order distortion, but you can have it because of this reason now has before, if R is very large then there is a pole between the actual common mode Vop plus Vom by 2 and this point this point, where you do the comparison and you can reduce the effect of that pole by adding a zeros using this capacitance.

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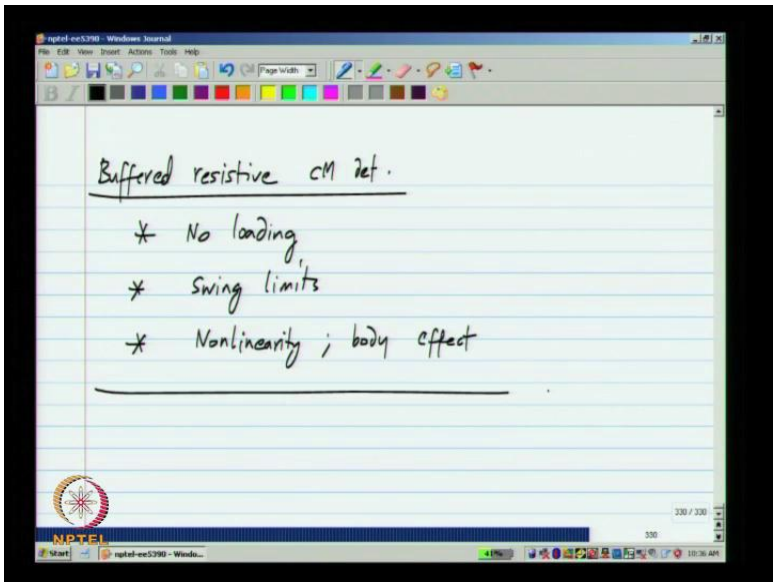


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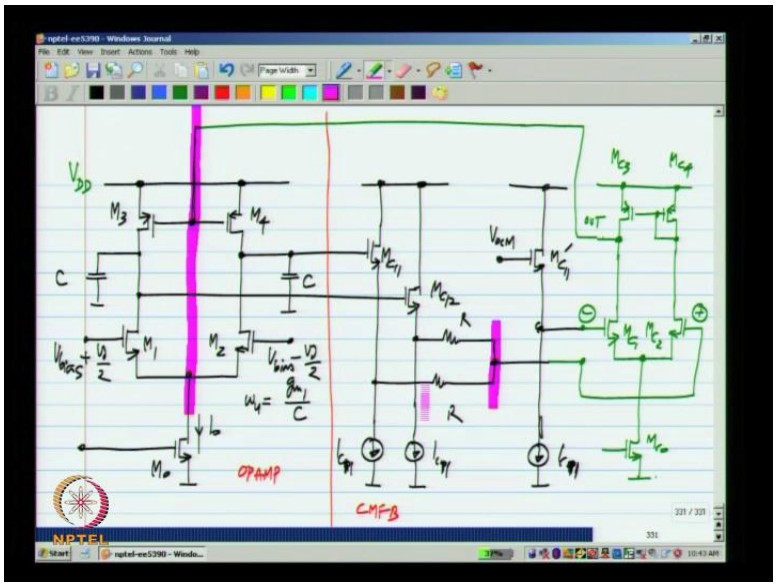


This is a summary of the buffered resistive common mode detector. Let me just show you the full circuit of the single stage op-amp throughout slightly differently from before I will show these as current sources, but it is understood that you make them using most transistors. So, we compare this to and feedback there will see how to make this particular op-amp shortly. So, right now this is what the circuit is and we can also see that in the differential picture this point will be a ground and this two will in the ideal case offered no loading in reality, because of Cgs of Mc1 and Mc2, there is some small loading on the single stage op-amp.

I have not shown the integrating capacitors of the single stage op-amp whatever load capacitors you have here will be the integrating capacitances and it is this part of it that is the op-amp and this is the common mode feedback, and this implements a fully differential single stage op-amp with a unity gain omega u equal to gm1 by c and a dc gain, which is the gm of this transistors divided by some of gds of these two transistors now we need to go in and implement that op-amp.

Now, we do not need a really fancy op-amp that. So, we will start with the simplest open that we know that is the single stage up now notice that this op-amp differential input in single ended output. So, the single stage op-amp that we analyzed earlier with the single ended output is what we are going to use. Let me change the notation a little here, I will call this transistors Mc11 and Mc12 this is Mc11 prime this are all equal to Mc11. So, the single ended single stage op-amp looks like this, this is the plus terminal and this is the minus terminal that is the output and a common mode feedback is completed like that, all this upper lines are VDD.

Now, first of all one remark about this circuit this is just a single stage fully differential op-amp with common mode feedback already you see that the circuit looks very complicated with many transistors and it is probably at the limit of what I can draw in this area of the screen. So, it is extremely, extremely important to understand what is beyond the circuits you cannot really mug of this circuits, you cannot learn them bait and then figure out how the work, you have to be able to understand each part of the circuit, and then understand the function of the circuit also there is a huge variety of circuits I can change from n-mos to p-mos in most of the circuits I can change the kind of the common mode detective and so on. So, the most important thing is to understand the principles beyond this common mode feedback circuit or in fact, any other circuit.

Now, we have this common mode feedback loop and like any other negative feedback loop, we have to make sure that it has a small enough delay and it is stable now as well as the common mode feedback loop is concerned. We need to be concerned only with the common mode operation. So, I leaves the common mode half circuit that is normally you would apply a differential input to this op-amp, but I will now assume that we have applied only a common mode input and analyze a common mode part of it, and we want to analyze the differential part we can do it using the differential half circuit now keep in mind that this is the line of symmetry and this is the line of the symmetry as well.

So, these points will be at ground in the differential half circuit and in the common model half circuit I have to fold all of this circuits, and top of each other in parallel for instance this R comes on top of that R, these two transistors will be in parallel these two current sources will be in parallel and so on.

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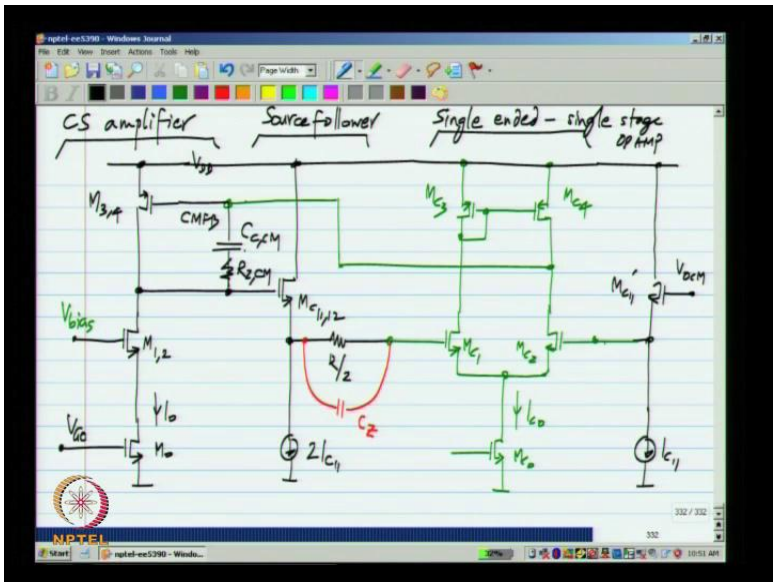


Let me draw the common mode equivalent circuit and I write M1,2 it means that M1 and M2 are in parallel and M0 appears as it is with a current I zero this is the common mode feedback node M3 and 4 are in parallel there and here I will have Mc11 and 12 and parallel with a bias current of two Ic 0, because I have a two current sources in parallel. I have the resistance R by 2, and this part of the circuit this is the same color as before here, I have the replica could generate the correct half set of the source follower. This is 2Ic11 and the current in this I will denoted by I c 0 and the common mode feedback circuit is completed from here. So, this part of it, which is really the differential op-amp simply looks like a current source in the common mode equivalent circuit. So, this is at some V bias and this the bias from M0 is derived from some current mirror, I will just call it VG0 these two together for my cascade current source.

So, now, if you look at this circuit we have a differential pair that is a single and that single stage op-amp, and the output of that goes to M3, 4 and this output is from the drain. So, basically M3, 4 acts like a common source amplifier this is a common source amplifier and the output of the common source amplifier goes to a source follower M

c11 and 12, it has a series resistance R by 2 but let is now acts as though it is not their are assume that the frequencies are so low that no current flows through R by two, because it is connected to the gate. So, we have a source follower. So, we have a single ended single stage op-amp cascaded with a common source amplifier and a source follower in the feedback loop, the feedback loop goes like this right. So, here we have it, and then the output of the single ended single stage op-amp is like that, and then feedback loop gets completed that way.

So, that is the feedback loop now, what do we know about the stability of this, if you observe this circuit what we have is equivalent to a two-stage op-amp with an additional source follower buffer, a source follower buffer came, because we use the buffer common mode feedback stage, if we did not use that even that could not be there, because what we have in a two-stage op-amp is a single ended single stage op-amp followed by a common source amplifier. So, the part that I have drawn in green plus the transistors M3, 4 will act like a two stage op-amp and it happens to have an additional source follower buffer MC11 and 12 in the common mode equivalent circuit.

So, whatever we discussed earlier for the stability of the two-stage op-amp will apply here as well, now we know that in order to have stability in the two-stage op-amp we needed to have miller or integrating capacitor from the gate of the common source amplifier to its drain. So, this is what was called Cz, and because it is here for the common mode feedback loop, I will call it Cccm this is what makes this g m and this C behave like an integrator remember what we what we need here is an integrator now, what we have implemented is not an integrator by itself, but trance conductor and its trans conductor in combination with this Cccm behaves like an integrator now, another way to think about it is that there are too many stages in feedback loop. So, there is a lot of parasitic delay.

So, one of them has to dominate right one of the delays has to dominate that is what we call by dominant pole compensation. So, the feedback as to be close around a single stage and that can be done by using this capacitor. So, anyway you think about it essentially you will have single stage an feedback and also as, I mentioned earlier if this R by 2 is very large then these R by 2 in combination with the Cgsmc1 will cause a lot of delay in the loop. So, you may also have to connect a capacitor. So, there it creates a zero in the loop. So, this is what we need in order to have a stable common mode feedback

loop now, you see that the circuit looks exactly like the two-stage amplifier, where the Cccm is the integrating or the miller compensation capacitor, and just like with the two-stage op-amp you can also add a zero cancelling resistor in series with this. Now, please do not get this confused with the op-amp that we are trying to realize we are trying to make a fully differential single stage op-amp now, the common mode feedback loop for that op-amp looks like the single ended two stage op-amp.

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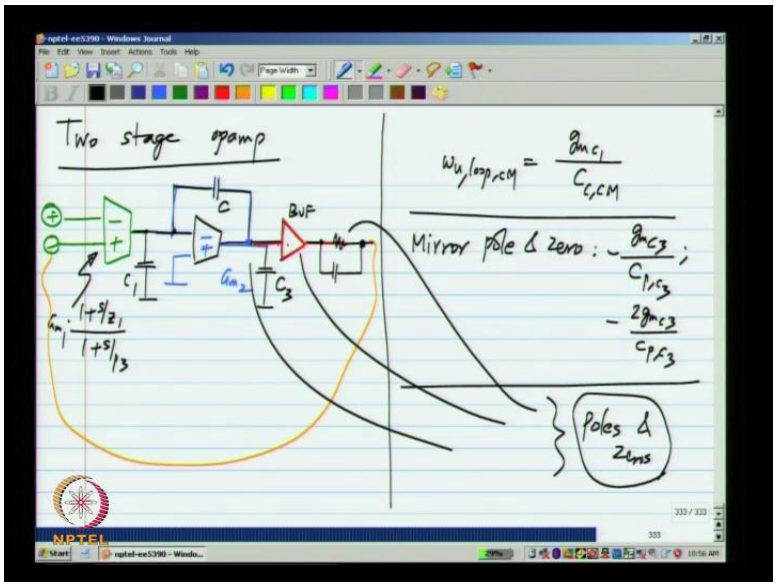


Now, because we have already analyze the single ended two-stage op-amp to a great detail we do not have to reanalyze that here we just have to associated the terms here with what we used over there, that is recall let the two-stage op-amp add a topology like this even addition to that we have the buffer, we also have parasitic capacitances here and there.

Let me just call it as C3 and this is C, and this Gm1 we know is not memory less g m, but it as a pole under zero. We these are the results that we have already derived for the two-stage op-amp you can go back to those lectures and revise that if you wish to. Now, this part corresponds to whatever, I drawn in green in the previous picture. So, that is the single ended single stage op-amp and this Gm2 in the second stage corresponds to the same three four and this integrating capacitor possibly with something that cancels their right half plane zero and finally, this buffer is made using that in addition to all of this we also have this in the loop.

So, you see that the loop is completed around this entire thing this loop is an unity feedback. So, what we need to know is which components are associated with, which part of this and if you wish to you can put down the values of Gms and calculate the, where the poles and zeros are and as certain, if the circuit is stable now the unity gain frequency of this feedback loop, which is also the unity loop gain frequency, because we have unity feedback around is will be Gm1 corresponding to this divided by C. Now, translating the terms it will be the Gm of these transistors Gmc1 divided by this capacitor here the integrating capacitor Cccm, the unity loop gain frequency of the common mode feedback loop is Gmc1 divided by Cccm.

Now, there is a number of poles and zeros is will have mirror pole and zero due to the first stage it will be at gmc3 divided by some parasitic capacitance associated with that that is, where the pole is and the zero will be at twice that value all this results you can recall from earlier analysis of the single stage op-amp. In addition to that we have the second pole due to this G m2 and load capacitance very rudely it is G m2 by C3 plus C 1, but we know it is not the case g m two will be divided by some factor and so on. So, you can work out the calculation and there also basically poles at associated with this node, and poles in the buffer and also due to this resistive element here. So, there will be a number of poles and zeros we have to make sure that the phase lag due to all of this poles and zeros at the unity loop gain frequency is let us see less than some value. So, 30 degrees also. So, you could have a healthy phase margin.

When practice what you do is not to sit and calculate all of this analytically you need to know, which of the company and contributes to poles and zero. So, that you can manipulate the values if you need to if you if necessary you can change the poles that is move the poles to higher frequencies and so on, but generally once the circuit becomes so complicated this hand calculations will not be efficient. So, we will go to the simulator in one of the later lectures, I will show in detail how to design an op-amp using the stimulator and how to measure the loop gain and so on.

So, that you can have a sufficient phase margin you can design the feedback loop to have a sufficient phase margin and limited ringing in the step response. So, for this were will do is put the circuit in a simulator and there are ways to measure the small signal loop gain, and are also ways to measure the step response you will do that and make sure that the stability is guaranteed. When you carry out its an exercise and find out that the phase

margin is not sufficient or there is a lot of ringing you will need to know, which components to change now the analyses that we have done earlier is useful for that. So, you should know which components are contributing to the poles and zeros. So, that you can change that part of the circuit and improve the phase margin.

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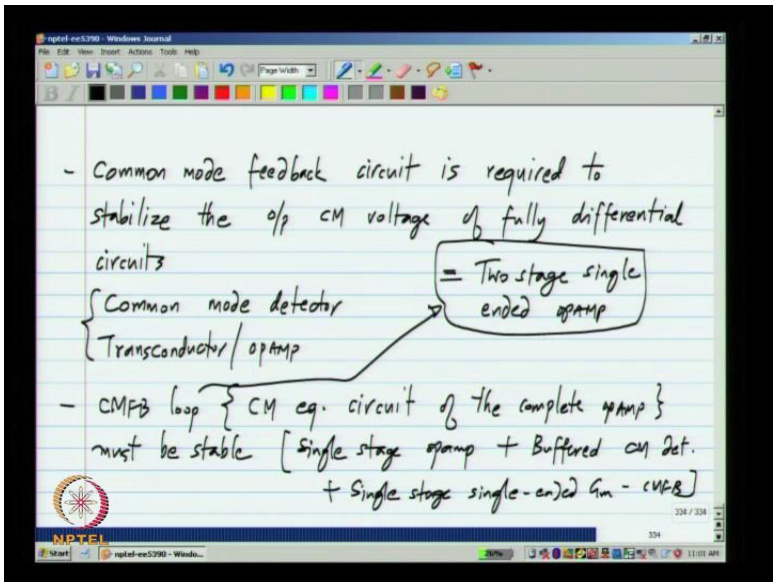


Then summary, a common mode feedback circuit is required stabilize the output common mode voltage of fully differential circuits. Common mode feedback circuit consists of a common mode detector plus some trans- conductor or op-amp to complete the feedback sometimes this trans-conductor to compare the detected common mode to the desired common mode is not explicit, but it is implicit within some part of the circuit. Now, the common mode feedback loop, which basically is the common mode equivalent circuit of the complete op-amp must be stable of course, like any other feedback loop and hereby stability we mean not only not oscillating that is not nearly having poles in the left half plane, but also limited amount of ringing and overshoot .

So, the common mode equivalent circuit can be anything now further particular case that we considered and this is fairly typical case single stage op-amp plus a buffered CM detector plus the single stage trans-conductor, single stage single ended trans conductor for CMFB. Now, in this case the common mode feedback loop itself looks like a two-stage single ended op-amp and you have to analyze this usually with the simulator and ensure that it is stable. Now, if we go back to the very simple common mode feedback

we had earlier although had was this R connected there, there will be invariable some parasitic capacitance at this node due to this transistors as well as may be due to the resistors. The common mode equal lent circuit of this is...

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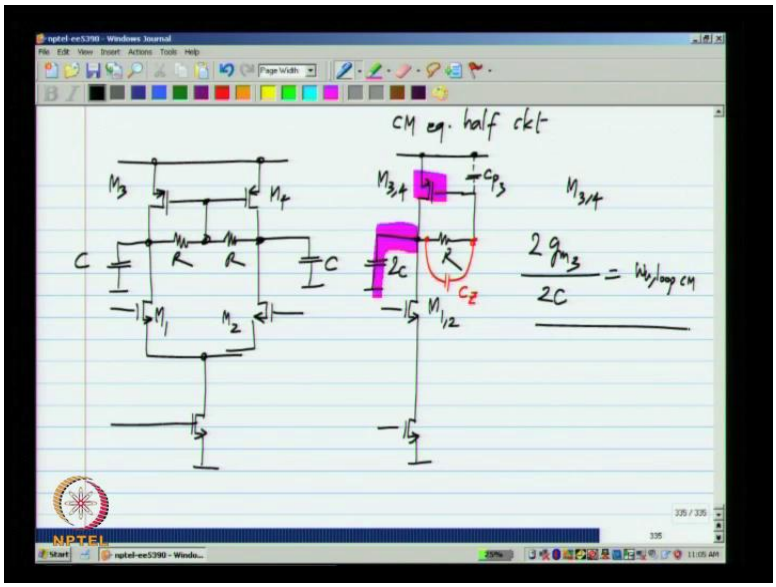


So, there may be some parasitic capacitance here I will call at C p3, and then the to make this into an op-amp will have the integrating capacitors C will have that now, in this feedback loop, which is basically that one. The combination of M3,4 and this capacitors this should be 2C in the common mode half circuit common mode equivalent circuit. So, this transistor and these capacitors behave like an integrator, and this resistance in combination with Cp3 will be a parasitic delay, which can be reduced by adding a capacitor Cz now, because we have one integrator and a single parasitic pole quite easy to stabilize this one compare to the other case, where we add a two-stage op-amp.Now, the common mode feedback loop in this particular case is equivalent to a single stage op-amp and the common mode feedback loop when we have a more elaborate common mode detector is like a two-stage op-amp.

Now, this is fairly typical case and you need to be able to work with this, but because we have analyses the two-stage op-amp in great detail you should be able to work it out I am not going to write the expressions for poles and zeros here I am assuming that you can associate this components with the components in the two-stage op-amp. Similarly, here the integrator is the g m of M3,4 that is two times g m3 divided by 2C that will be the

unity gain frequency of the integrator in the common mode feedback loop in any feedback loop you will have some integrator like behavior, and you will also have parasitic poles and zeros in the circuit you just need to make sure that the effect of all those things is such that the phase margin is sufficient that is there is not a significant is that phase lag at the unity loop gain frequency. This is the unity loop gain frequency of the common mode feedback soon see you in the next.

Thank you.