Analog Integrated Circuit Design
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Lecture No - 39
Fully Differential Circuits

Hello everyone and welcome to lecture thirty nine of analog integrated circuit design in the previous lecture, we looked that a common mode rejection and what can happen if you have insufficient common mode rejection in this lecture. What will do is to see the other effects of common voltage drops in the circuits. Now, it turns out that a in every circuit there is common node that is known as the reference node.

Now, we have been measuring voltages with respect to that like for instants the opamp that we have as a single node as the output voltage about what it really means, is it is between that and common reference node of the circuit. So, whenever we specify voltages at some node, what we mean is between that node and the common reference point. Now, this common reference point may not be all that common to the different parts of the circuit will see exactly what we mean in a moment and, because of that voltage that we want to be applied to some particular stage of the circuit may not be applied in that way there could be some extra voltage added to it. Because of all the things we may need to change the way, we transmit voltages and that is what we look at in this lecture.

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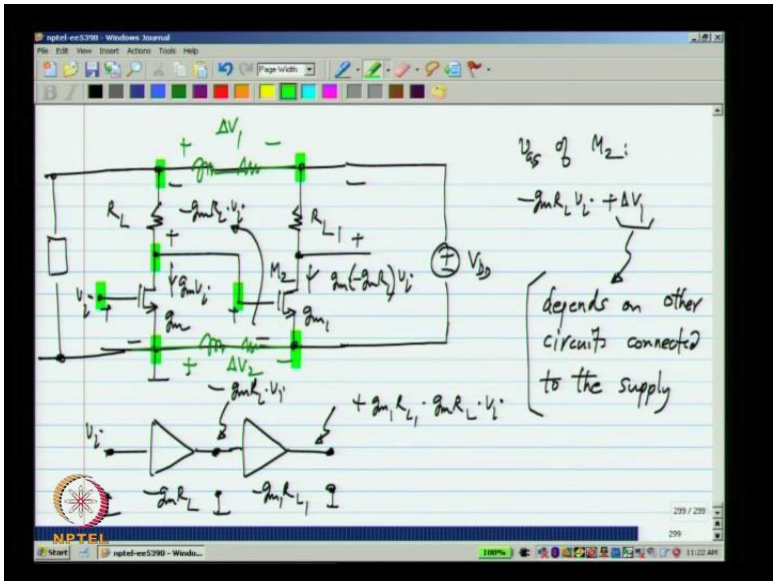

In case of an opamp in many cases, we specify the voltage at some node at v node, what it really means, is that it is the voltage between that node and the common reference point. Now, let us take common source amplifier for instance, I will not show the biasing details. Let us assumed that it is biased in saturation region. Now, if a voltage v I is applied here, output voltage is said to be minus g m r l times v i. Now, what is this really mean the input voltage v I is not at this point, but it should be applied between gate and source that is what the meaning of the common source amplifier is and only, then will be get g m times v I as the incremental current through the transistor and that flows into register, and we get this as a output voltage, and this output voltage appears really between these two nodes that is across resistor, but we assume that v dd is powered by a dc voltage source v d d such as this.

So, there is no difference in incremental voltage between the upper node and the lower node. So, if you measure the increment between these two points that is between output of the common source amplifier and the ground. We also get the same voltage that is the assumption. Now, let us consider a cascade of amplifiers. Let, us say we have number of common source amplifiers in cascade this as a gain of minus g m r l, and let us say the next one has a gain of minus g m one r l one and. So, on if I have v I here, the voltage here is minus g m r l v I and here it is minus g m one r l one times minus g m r l, which makes it plus g m r l v i.

Now, as before what I want to emphasize here is that all these voltages are measured with respect to some common ground, and that ground must be common to both the amplifiers. Now, let us say we have a cascade of two n most common source amplifiers and again let us not worry about biasing. Let, us just assume that there bias correctly and in saturation reason and. So, on the second stage as a load resistance r l 1, and this as a trans-conductor g m 1.

Now, if the circuit is really as shown here everything will be fine, if I apply v I between this point, and that point and incremental current g m v I flows through the transistors, which flows into the resistor and that creates a voltage drop of minus g m r l v I between these two points and, because v d d is a fixed dc voltage the increment that is applied to the gate of the second transistors is also exactly equal to that one. So, that in turn produces an incremental current, which is g m g m r l v I and that produces another

voltage and. So, on and you can measure it either to respect with v d d or with respect to ground. Now, what happens in reality these wires here are not perfect conductors.

So, what happens is that they have resistors and inductances and similarly, on every rail there will be resistance and inductors. So, now, let me just consider this two, and then let me assume that there is some delta v 1 across this and delta v 2 across that now, it is still true that if you apply v I between these two terminals the voltage across r l will be minus g m r l times v i, but what is a voltage that appears across the gate source of the second transistors the incremental v g s of m2. Let, me call this m 2 will be minus g m r l v I plus delta v1, because we have this extra drop and this and that point are at the same points small signal wise that is the assumption the voltage here, and there are the same thing. So, you have a minus g m r l v I across this and plus delta v1. Now, what is this plus delta v1 it could be anything, because it depends on the currents flowing in this parasitic elements. First of all we do not know the value of this parasitic elements also there could be other circuits connected to it.

So, what happens in that case is that the current through this depends on what is happening in the circuit, what is happening in that circuits and every other circuit that is connected together. So, this delta v1 depends on other circuits connected to the supply and, what is the consequence of that the input to this amplifier stage formed by m2 is not just the output of the previous stage plus some garbage delta v1, which is basically unrelated to the input that you wanted to apply now, the consequences of this can be very severe. So, first of all you could get some additional signal, which you could calls interference, because of other circuits and also sometimes because.

Now, some tools circuits, which are internet to be separate are talking to each other are communicating with each other. There could be unintentional feedback and feedback loops and. So, on between different parts of the circuit and, because of that there could be instability as well. So, in general the voltage that is applied to one stage depends on the voltage of the previous stage plus some parasitic drops, which could be related to every circuit, which shares the common supply line.

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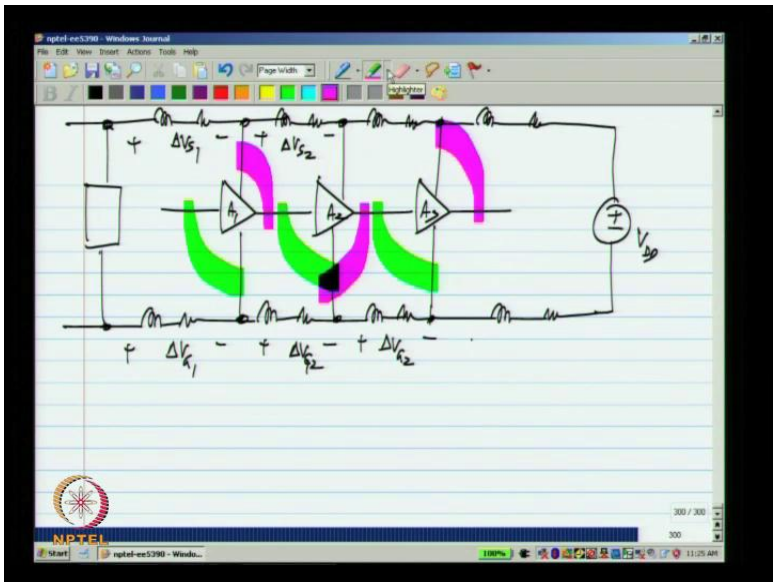

Also, we have three amplifier stages A1, A2, A3, and some other circuits connected together. There will be parasitic impedances in every wire and the share of common supply. Now, clearly there will be all kinds of voltage drops here. So, let I call this delta vg1 and delta vg2 and.

So, on just to show that their voltage drop across the ground lines and similarly, here we could have delta vs2 delta vs1 and things. The actual input of the first amplifier is between these two terminals, this is between those two. Let, us assume that is the case and the output voltage of the first amplifier could be this and ground. Let us say it could be like that and the second one let us say between those two it depends on, what is inside the amplifier, but here we are not worried about the details, but just to say that what they seen by the input of the second amplifier is not just the output first amplifier, but it has a extra parasitic voltages due to a inductance in a supply and ground lines. Similarly, a the third one does not see the output of the second one and so on.

Now, this is a consequence of sharing common supplies and that is simply not avoidable. We cannot have separate supply for every circuit. So, that we do not share the common vdd ground lines. It will always be there and they will always be some currents flowing through that. So, we have to find ways of combating this right this is one of the serious problems and this is also the reason, why any circuit that you wire should be wired compactly. It should not have long wires going all over the place that will simply

increase the parasitic inductance and the resistance and make your life harder. So, whether you are doing layout of integrated circuit or building circuits on the bread board. You should keep the circuits need and compact that is the key to this fully working circuits.

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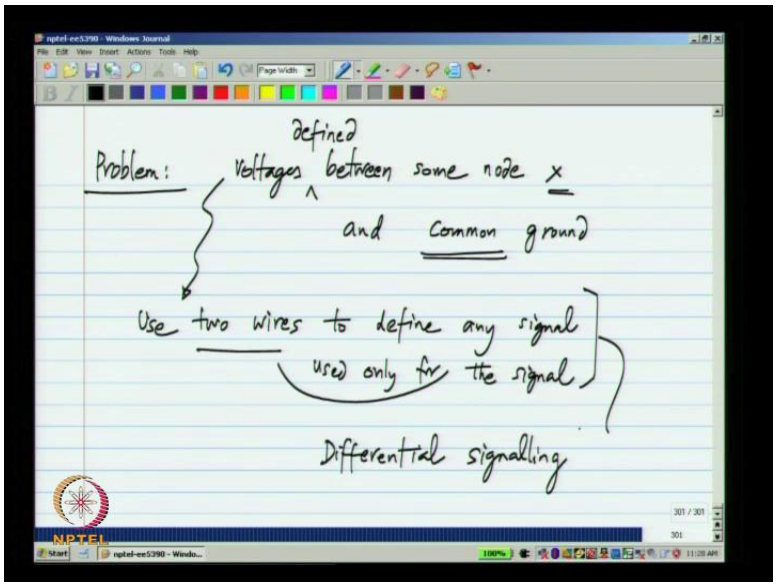

Now, what can we do about this the real problem is that voltage are always defined betweens two points, and in our case the voltages are defined between some node x, which is designated for the signal and a common reference line are common ground. Now, because one of the terminals, which is used to define the voltage is common to many circuits. You have this problem that the common ground may not be all that common to all the circuits.

So, if this was an ideal conductor without any inductance at all the voltages here, there and there will be the same it will be an equally potential, but in reality that is not the case. So, what should we do? We should use two wires to define any signal and this to wire be used only for the signal, then at least what happens is that? We have two wires used only for the signal. There can be no parasitic drops along those lines.

Hopefully, those wires will not be carrying any other signal. So, there will be nothing unrelated to the along those lines, where previously we were using the single wire and the common reference note will always use two wires to define every signal. So, that is

one thing and this is the basis of differential signaling. Differential signaling means a little more than this will come to that.

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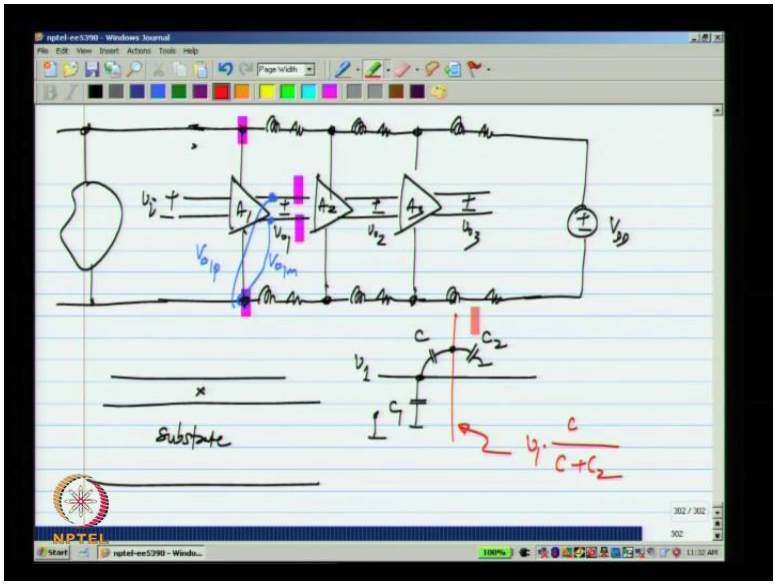

So, what we would like to have is not amplifiers with a single input and single output wire. I will redraw the previous scenario here, but I will assume that I will amplifier structures are, such that the input voltage is defined between this two wires, and the output of the first to one is defined between those two output of the second one is defined between those two and this is a final output. Now, also they have to be power from the same power supply that is something. We simply cannot avoid and then will be parasitic impedances everywhere.

So, let us say we also have some other circuit connected here, but the crucial difference is that the second amplifier is sensing the difference between the voltages of that wire and that wire. Now, let us assume that this two wires are equally affected by any change in the voltages at the top and bottom. That is what I mean is, if you measure the voltage of this with respect to let us say that one that node. So, let us say I call it vo1 p and I measure the voltage there v o1 m. They will be affected in the same way, let us make that assumption and that seems like a fairly reasonable one, because the amplifier is supplied by this voltage and that voltage and this amplifier is generating the two voltages with respect to that one. So, it is reasonable to assume that any shift in this can cause an equal shift in v o1 p v o1 m, what we are looking at is not the individual voltages v o1 p

and v o1 m, but the difference between the two. So, the common voltage drops will not affect the signal.

So, this is the idea by dedicating two wires to each signal, you will eliminate the effect of common voltage drops. So, that is one thing basically, we have common voltage drop due to sharing the common supply and ground lines, but if you do not define the signal as the signal between some node in the circuit, and the common point of the circuit, but there as the difference between to wire is dedicated to the signal. You will not be generally affected by the voltage drops along the supply and ground lines exactly. How to implement this will see, but at least it look like a reasonable thing to dedicate two wires to each signal.

So, there are not affected by common volt response also there are other ways in, which a signal can be affected. Let, us say we have a common substrate, which is usually some ground and will have two wires crossing each other. Here are two shown to as perpendicularly and, if I look at the top view. I will have two wires crossing each other like that and let us say this voltage as some v 1 with respect to the common point of the circuit. Now, whenever you have two wires crossing each other you will have capacitances between them.

Let, us say we also have some capacitance from each wire to ground, if you have wire number one it will induce a voltage on wire number two. Let us assume that v1 is sometime wearing voltage. So, the voltage on this wire will be v1 times c by c plus c2 is proportional to the overlap capacitance between the two wires. So, whenever you have two lines crossing each other, because of the capacitor coupling the signal in one wire can interfere with the other wire. So, this is again a problem, because you will always have wires crossing over each other and we should find some way to avoid that will use the previous idea of a using two wires to define a signal, and see how this coupling can be eliminated first of all.

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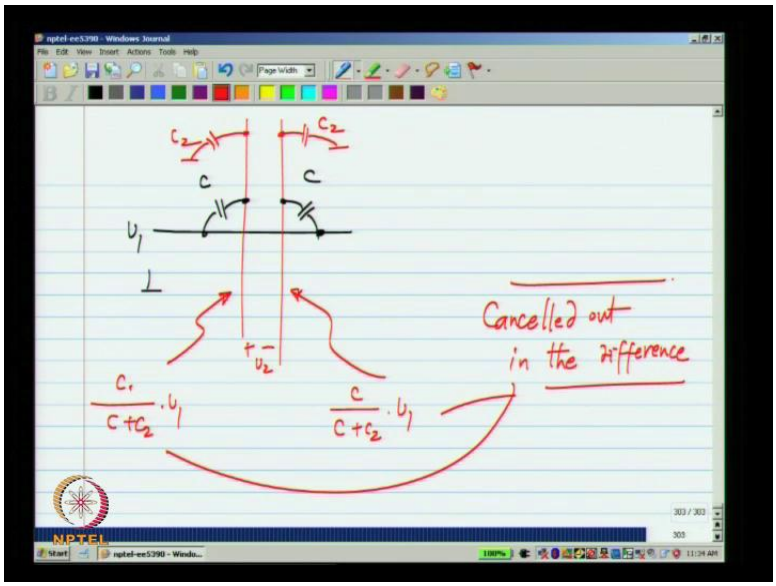

So, let us say we have a signal wire one with the signal v1 with respect to some reference note. Now, let us say I have a pair of wires. Now, whereas, I earlier had a the single wire to transmit this voltage v2 with respect to ground. What I will now, do is transmit v2 as a difference between to physically identical wires, which are closely separated and. So, on I will also assume that, because of physical symmetry of layout the coupling from wire one to each of this wires is the same again the two wires are physically the same. So, this will have some c2 and that will also have some c2. Now, it is quite obvious that if you apply v1 on wire number one, what appears here, will be c times c plus c2 times v1 and, what appears on the other wire will be exactly identical c by c plus c2 times v1. So, when you take the differences and voltage between the two, this too will get cancelled out.

So, that is one thing. So, if you use two wires you have an additional advantage, if you have a common interference that is coming to two wires. We already saw that the effect of voltage drops along the supply on the ground like is like a common interference, but we cannot… So, have wires crossing over the two wires, and have two common interference to the two wires. So, again you have a common interference to the two wires and if you are looking at the different voltage between the two wires that will get cancelled out. and finally,

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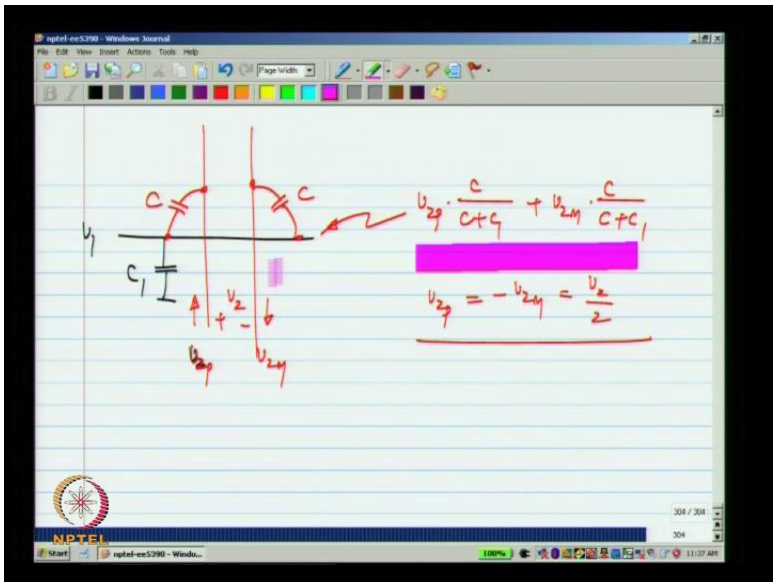

When, we have a scenario like this, it is not only that this v1 disturbs the signal on this two wires what we apply on the red wires also affect the signal on the black wire soul. Let, me call this v2 p and v2 m and, this is c and that is also c its assume that whenever, we have this differential signals. We also layout the lines with physical symmetry so, in the layout. So, the capacitance and other physical parameters will be the same for the two wires. Now, if you have two signal v2 p and v2 m, which basically represents the difference signal v2. What happens is that the interference on this line, the black line due to v2 p will be v2 p times c by c plus c1 and due to v2 m will be c by c plus c1.

Now, what happens we would like this also to be zero. It is not that we have only want to take in zero interference. We should also not be put out interference into other wires and that will happen, if v2 p and v2 m are equal and opposite of each other, and the equal to half the different voltage with respect to some common ground. If this is the case whenever, if let us say with respect to some common mode ground. If this voltage goes up and other voltage goes down by equal amounts. It also puts out zero interference into other wires, which may be crossing it.

So, this is the motivation for using what is known as fully differential signaling, the idea there is you use a pair of wires instead of single wire with respect to ground to define every signal voltage. Now, because if you use a pair of wires and tends only the difference between them and, the operation of the circuit will be immune to a changes in

the supply voltage, and ground voltage to a large extent. It observes less interference, because if you have a common interference to the two lines del get cancelled out. When take the difference they will also put out less interference, because each wire puts out an interference that is equal and opposite to the interference by the other wire.

So, in general for having clean or signal processing you always use the differential signals. Now, there is some trade of you are using two wires, instead of a single wire for every signal and that essentially increases the hardware size. So, when you use discrete circuits. You buy an large not to this you do it, when necessary that is, when you make circuits for discrete components. You do not want to double the number of wires and as we will see later.

The number of components required also tends to double in an integrated circuit. The scenario is different, what matters is the total area not the number of individual transistors wires. So, if you can pack twice the wire into the same area, and get better performance you always do that. So, it is very common in analog integrated circuit design to use fully differential signaling. So, you can you can assume that by default you will design fully differential circuits. You will use single ended inputs or outputs only, when necessary sometimes the input that you get from transducer or something like that will be single ended.

So, then you have to use a single ended input stage similarly, sometimes when you put out a signal to some transducer or whatever, it is that also has to be single ended in many cases, and then also you use a single ended circuits, but inside the integrated circuits itself. You tend to use fully differential signals and fully differential circuits as much as possible.

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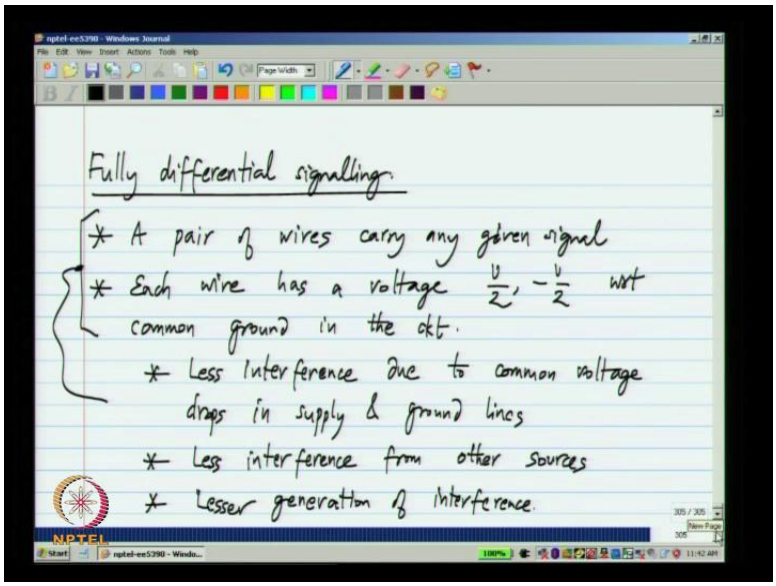

And fully differential signaling a pair of wires carry any given signal, and the two wires have voltages v by 2 and minus v by 2 with respect to the common ground in the circuit and, because of using this what we have is less interference due to common voltage drops, and supply and ground lines will also have less interference from other sources this is assuming that their layout is physically symmetrical, and the interference absorbed by each wire is same and also it puts out lesser interference. So, what will do from here, on is to translate the circuits that we had. So, far into fully differential versions now, it may be a little difficult to grasp, because of only talked in generalities, but the things will become clearer as we go along.

Now, were we earlier had a one wire as an input and one wire as an output. Now, again I emphasize that voltages are always defined between two wires. When we have single ended inputs and outputs it means that the second wire is the common reference or the ground of the circuit. When we have a fully differential circuits, we do not use the ground as a reference. We explicitly provide two wires each wire acts as the reference for the other wire.

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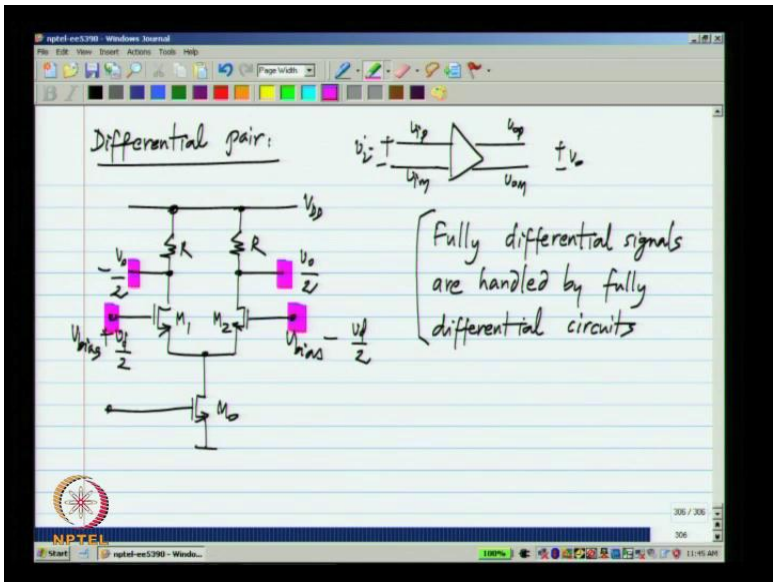

Now, we have already seen an example of fully differential circuit and that is the symmetrically loaded differential pair. In general fully differential circuits handle differential signals, and they should have identical transfer functions for the two half the signal. So, the circuit themselves also be fully symmetrical.

So, like this one is… So, this is symmetric, if I draw an axis vertically like this the circuit is symmetric about that axis. The output will have an increment of sum plus v o by 2 and minus v o by 2. So, the input is defined as the difference between these two voltages and the output is defined as difference between those two voltages. So, as I said fully differential signals are handled by fully differential circuits. Now, how do you analyze fully differential circuits? We have already looked that it earlier, if you have a perfectly symmetrical circuit. You can and you have either symmetric that is equal input to the two sides are anti-symmetric that is equal and opposite inputs to the two sides. You can reduce the circuit into half circuit.

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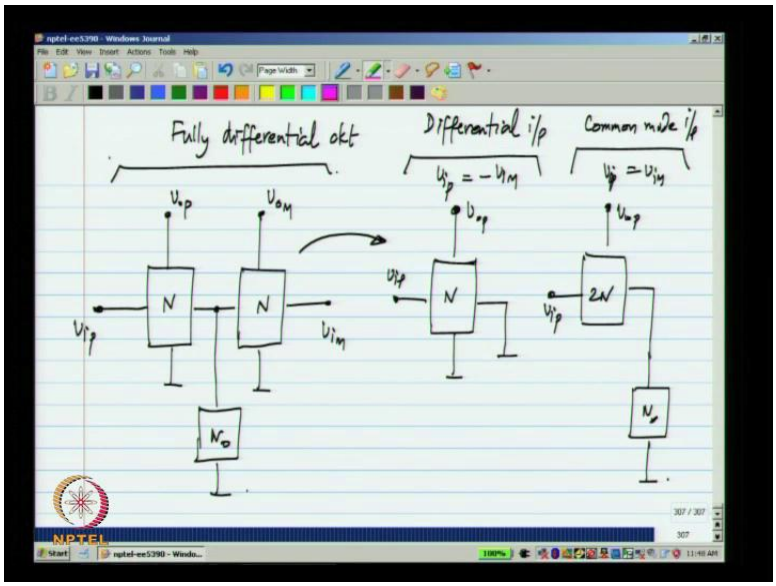

Let, us say this is the symmetrical circuit may be I will show it like that, I will show the two half's although sometimes to half's may not be separable I shown here, will be some common path to the circuit. So, this is the fully differential circuits. Let, us say this is the positive input, negative input, and this is the one of the output it could be positive or negative v o p and v o m and these two circuits are identical and this is the common circuit and zero. So, we have seen that for differential input, what it means is v I p is minus v I m. We can reduce circuit to n have v I p alone and along the axis of symmetry. You have zero incremental voltage and that can be grounded. So, this assume that the circuit is linear, which every small signal circuit is and by looking at the results of the circuit analysis of this. You can put negative voltages to the other side and complete the voltages in the every part circuit. If you have a common mode input that is v I p calls v I m, what happens is that the voltages in you are the two circuits will be exactly identical to each other.

So, I will have a network ill call 2 n, what is means is that every node of n on this side is connected to every node of n, on the other side that is you have to instants of n connected in parallel, and you have v I p and v o p and you have a n naught as it is and as I mentioned. When I when we first discussed this is only symmetry. It does not require linearity. So, using this we can analyze any fully differential circuit and. In fact, in many cases the analysis of fully differential circuit is easier than that of a single ended circuit.

So, we will first complete the analysis of the fully differential pair amplifier this way than already.

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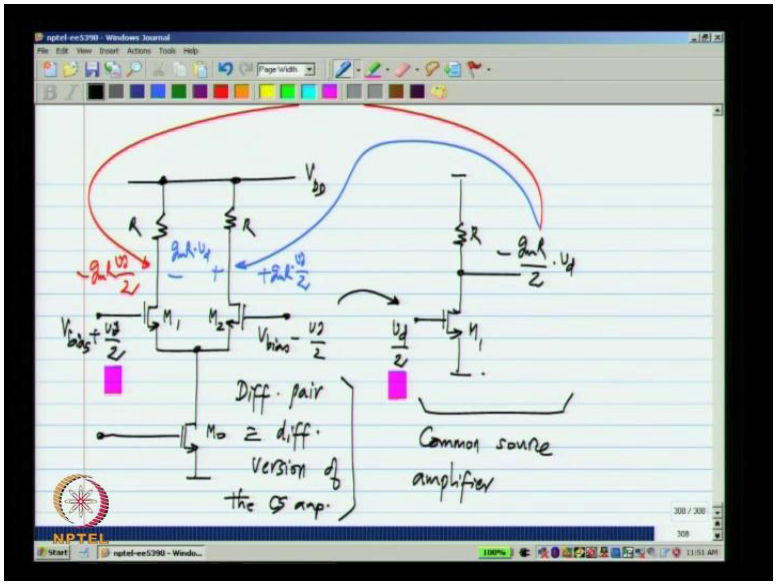

So, I will go little quickly through this. So, let us have a fully differential input the half circuit will be just that. Now, let us assume that this is the small signal model, because the differential half circuits requires linearity, and only in the small signal senses is this linear, this cannot be used when the increment v d is very large. So, I have an increment v d by 2 here, and this is just my common source amplifier. So, I know exactly what the output is it is minus g m r by 2 times v d that is minus g m r is the gain of the circuit and times v d by 2, which is the input now how do you get back to the solution of the fully differential circuit. I analyze the left part of the circuit, I assumed m1 here and applied an input v d by 2. So, now, the output there will be exactly minus g m r b d by 2 and the output on the other side will be equal and opposite to that. So, it will be plus g m r v d by 2 and between the two outputs. If you are interested in calculating that you will get g m r times v d.

So, that is how we solve the circuit and, we know that this is the common source amplifier. So, the differential pair can be thought of us the differential version of the common source amplifier. Now, many circuits which are in single ended form can be taken and converted into fully differential form away synthesize the differential, by we synthesize the differential pair by going down some other route. We wanted to take the

difference between the two voltages and amplifier only the difference, but now we can also think of it as a difference of fully differential version of the common source amplifier. Similarly, a we can analyze the common mode equal and circuit. We have already done this, while trying to calculate the common mode rejection ratio. So, you are not going to do that. Here, now we also are interested in calculating the noise and mismatch of, such a circuit let me again draw my differential pair.

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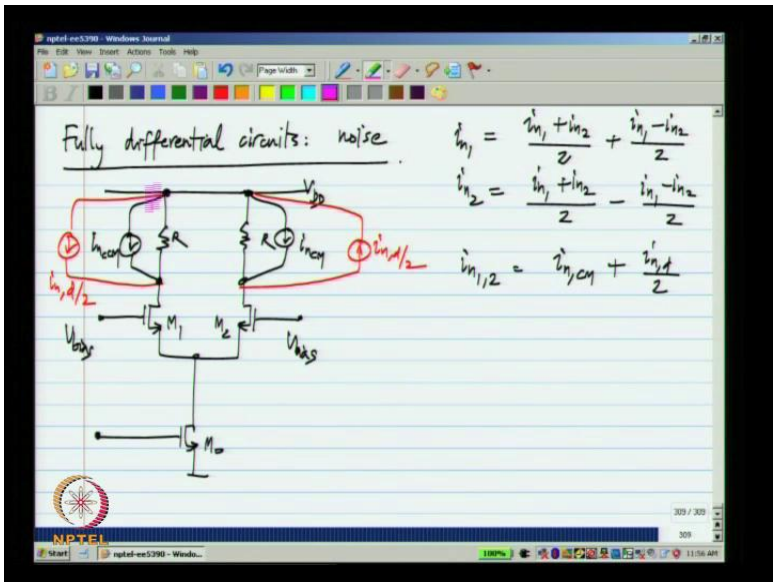

Now, in case of noise is let us say the noise from this particular resistance r is denoted by this current source. Let, us say I n I n r will see that the circuit itself is symmetrical except this current source. Now, if you include the effect these current source the circuit is not symmetrical at all are you can think it us a symmetrical circuit with a symmetrical expatriation. So, we cannot use the either differential are common mode of circuit directly for some circuit like this. So, what should be to one of the things that. We can do is to simply analyze the complete circuit right. We do not worry about the half circuit, we just analyze the complete circuit by putting down k c l and k v l, but that is a relatively complicated and also, there is easy way of reducing this also to the half circuit.

So, that is what we going to do now, what I will do is, I will show this for the case of the noise from the register and it will apply for any other noise is will let, me call this eigen one, and I will also consider the noise from other register eigen. Now, as usual in the nice sources eigen one and eigen two are any two sources eigen one, and eigen two can

be decomposed and to one part that represent the some, and another part that represented the difference. Similarly, eigen one eigen two will be eigen one plus eigen two by 2 minus eigen one minus eigen two divided by 2. So, I will use this representation.

So, eigen one and eigen two will be some common mode eigen plus the differential eigen divided by 2. Now, how this helps first of all these noise current source eigen are small signal sources. What I really have is eigen c m apply to both side with same polarity and I n d by 2 applied to the two side with opposite polarity and, because these are small signal inputs the resulting circuit that we use for its analysis fully linear. Now, once you have linearity you can use superposition and analyze the effect of different sources separately, and add up the result. Let, me copy this and remove

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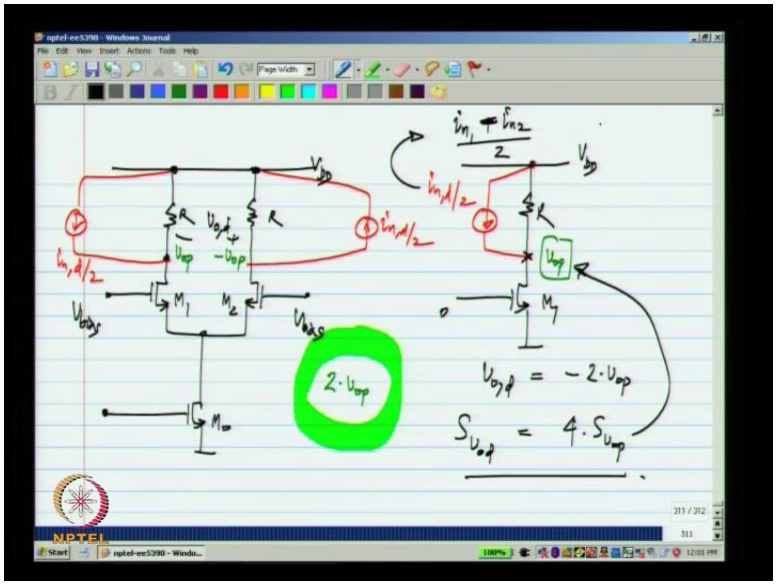

the differential part of the signal now. So, I have I n c m injected to two sides, what happens in this case I can use the common mode of circuit, because I have a symmetrical circuit with symmetrical excitation. Now, you already know how to do this? All I have to do the four, it the right side of the circuit and the left side and. So, on, but I want you to go through the complete analysis, because what I will get will be the same voltage on the two side. Let, us say I am interested only in the difference between the two sides remember my output the difference between the two I have fully differential output as well. So, I will have the output to be the difference between corresponding nodes of the circuit.

So, I will have the output to be the difference between this note voltage, and that note voltage and that will be zero, because in this with common mode excitation the voltage here, and the voltage there will be exactly same as each other the effect of in c m on the differential output will be zero and similarly, the noise from any part of the circuit that is common to the two half right. So, like m zero there is no replicated.

So, let us see that also will result in equal voltages on the two side and that also will have zero effect is a common components, it is common to the two half. So, like tail current source and that also will be zero. Now, this we see in earlier in the case of single ended single stage opamp, the effect of noise from the tail current source et cetera is zero, because the travel through that two-path identically and get cancel with output in this case c I is simpler, because it symmetrically injected the produce equal voltages, and the two output nodes, and then take the difference output will be zero and similarly, now what I will do is, I will consider the differential parts of the noise I will remove this and I will consider only the differential part shown in red. Now, what happens in this case we were symmetric circuit with anti symmetric excitation. So, I can use the differential half circuit like that now assume the this is the small signal equivalents circuit.

So, the gate is zero volt and I have single noise source, which is I n d divided by 2. So, I will get some output voltage here let me call that v o p. So, in the full circuit I will have v o p on this side and minus v o p on the other side. So, the total output voltage will be two times v o p. So, where v o p is the voltage due to this noise I n d divided by two and the total voltages 2 times v o p, let me call that the differential output will voltage. So, the total differential output voltages in this particular cases minus 2 times v o p. So, the spectral density of that will be 4 times the spectral density of v o p where v o p is whatever is obtain in the half circuit. Now, what is that is I n d by 2 is nothing but n1 minus I n 12 divided by 2, where I n 1 and I n 2 are spectral density of individual register.

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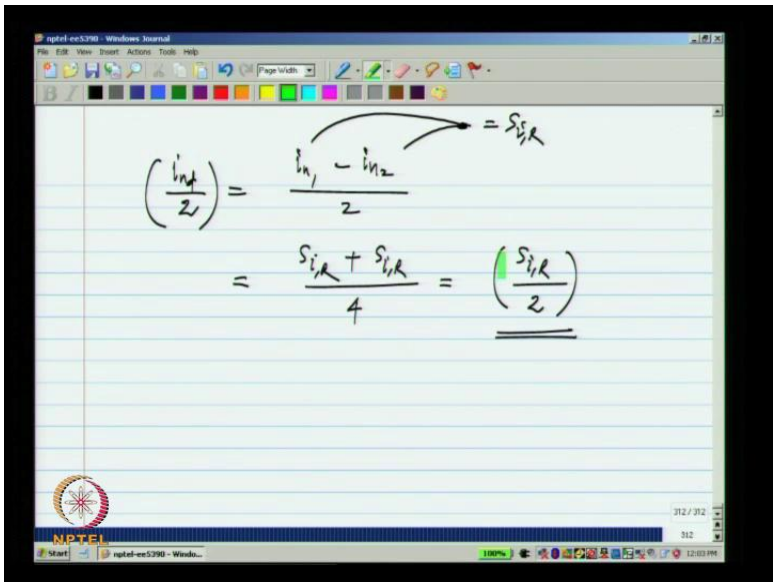

Each of this equals some s I r spectral density I n d by 2 simply equals the spectral density I n 1, which is s I r plus the spectral density I n 2, which is also s I r divided by 4 this is nothing but the spectral density of the resistant noise divided by 2. So, what we have now is a situation, where we have a register across that we inject a current, whose spectral density equals half the spectral density of the resistors noise, and we calculate the output and that will be 4 times the output that is obtain.

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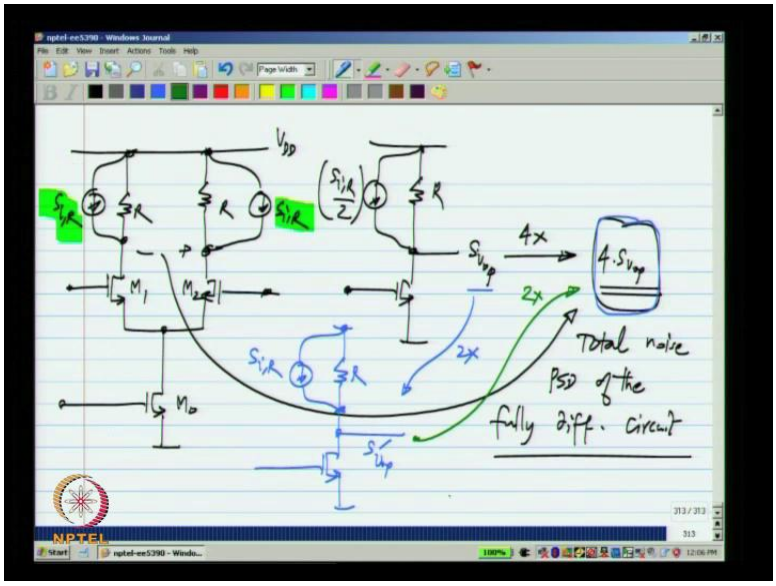

So, let me summarize again if you have a fully differential circuit will take the example of resistor, but exactly the same thing whole square any other component as well. So, each register will have some noise spectral density, and that will be the same on the two side, because the register themselves are the same on the two sides, but they will be two sources and correlated from each other. Now, in the half circuit let me highlight this just say that this is spectral density, this is not the in the half circuit. I will have the same resistance. I will inject half the spectral density of the register that is actually there. Now, I will calculate the output spectral density.

So, let us say that is s p o p and I have to multiply that by 4 get s p o 4 time s p o p is the output noise that is this is the total output nice spectral density of the fully differential circuit. Now, instead of dividing first spectral density by 2, and then multiplying by 4 what I can say you that. I will simply analyze the half circuit, as it is. That is I have a resistance r in the half circuit. Now, simply apply current source corresponding to the that resistance, which is s I r and I will get some output spectral density and I will call it s p o p prime to distinguish from that and the calculate this.

What should I do? Here, what I done is lot is to apply noise source with spectral density s I r instead of s I r by 2. So, s p o p prime 2 time s p o p and I have applied input current that is square root two times larger. So, I will have noise spectral density that is 2 times larger. So, I will also have an output that is two times larger, and instead of multiplying it by 4, to get this final value of noise spectral density have to multiply by simply 2. So, to analyze the noise of a fully differential circuit. What I have to do? Is to the analyze the noise of the half circuit and multiply the result by a factor of 2 and the result will be the total noise in the fully differential output.

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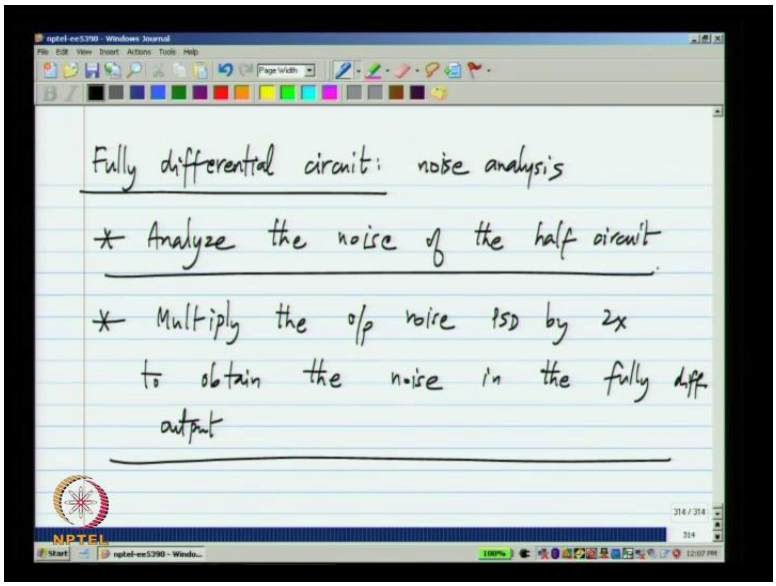

So, all I have to do is analyze the noise of the half circuit as, if that were in isolated circuit and I multiply the output noise spectral density by 2 x, to obtain the noise in the fully differential output. So, final algorithm for calculating the than noise in the fully differential circuit is very simple, all I do is to take the differential half circuit think of it as just some circuit and analyze the noise, I showed the example of the resistor, but the exactly the same thing holds for the noise from a mosfet, because that also simply adds current source in the parallel, but you have to be aware of what is happening in reality and of fully differential circuit.

Let, us say you take the noise current of one resistor that affects the voltages at all nodes in the circuit. So, it is not as to affects only the that half of the circuit so, but the noise from different component are uncorrelated. So, the final result is that you can simply analyze the half circuit along and multiplied the resulting spectral density by 2 get the noise of the fully differential output signal.

Thank you, I will see the next lecture.