Analog IntegrateDCircuit Design
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Lecture - 36
Two Stage Opamp

Hello and welcome to lecture 36 of Analog Integrated Circuit Design. We have been looking at opamp topologies and how to improve the DC gain. And, so far we investigated the couple of topologies; that increase the DC gain by increasing the output resistance of the Transconductor. Such an approach is not useful, when we have a resistive load; because the total output conductance will be dominated by the load. And, for a given Transconductance, we will only have a given DC gain. To increase the DC gain, we will have to increase the Transconductance and this enormously increases the power dissipation. So, we have to go to multistage topologies which inherently give a lot higher DC gain, even with resistive loads. So, that is what we will discuss in this lecture.

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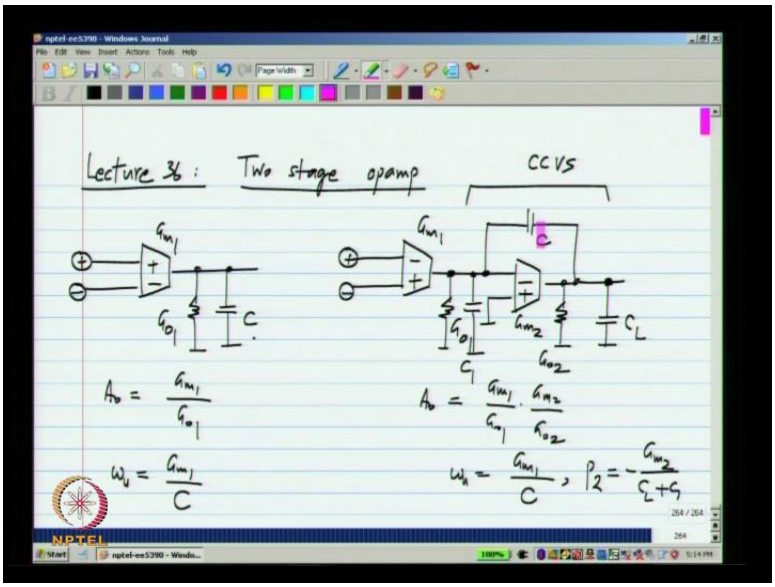

When discussing the opamp, at the control source level this was the basic opamp. Now, we said that the problem is the output conductance of this Transconductor to obtain a better I to V conversion. The problem here is not all of the output current to the Transconductor goes into the capacitor; some of it goes into this G out. To do better is a current controlled voltage source using a feedback circuit. The advantage here is that

because of feedback the input node is at a small voltage. So, the current that goes to G out is quite small; most of the current ends up going into the capacitor C. So, this is a much better integrator than this one. And, of course, the Transconductor that we use for the current control voltage source also will have an output resistance G o 2. So, this topology we saw that has a higher DC gain.

The circuit on the left side has a DC gain of G M 1 by G o 1 and the circuit on the right side has a DC gain of G M 1 by G o 1 times G M 2 by G o 2 and both of these integrators have a same unity gain frequency G M 1 by C. Now, we also analyze this in great detail. When we have this capacitance C 1 and a load C L, we saw what happens. So, we end up with two poles and 0 and we also evaluated the conditions under which we get sufficient place margin etcetera, etcetera.

So, we know that for instance the non-dominant pole is that approximately at minus G M 2 by C L plus C 1. Because G M 2 is in feedback, we get a more complicated expression; I am going to write that soon. So, we have all the things that we need to understand this topology. All we have to do is to implement this at the transistor level. Now, how do we go about doing it?

First of all you see that the input part of it is this is the same as before we have a Transconductance which was driving a capacitor, now it drives a current control voltage source. We already spend some effort coming up with topologies for this. So, we will use our single stage opamps for the Trans conductor. A single stage opamp is nothing but a Trans conductor and that will use in place of G M 1. We may have to realize this Trans conductance G M 2 and connect the integrating capacitor across it; that we will do see how to do and complete the circuit.

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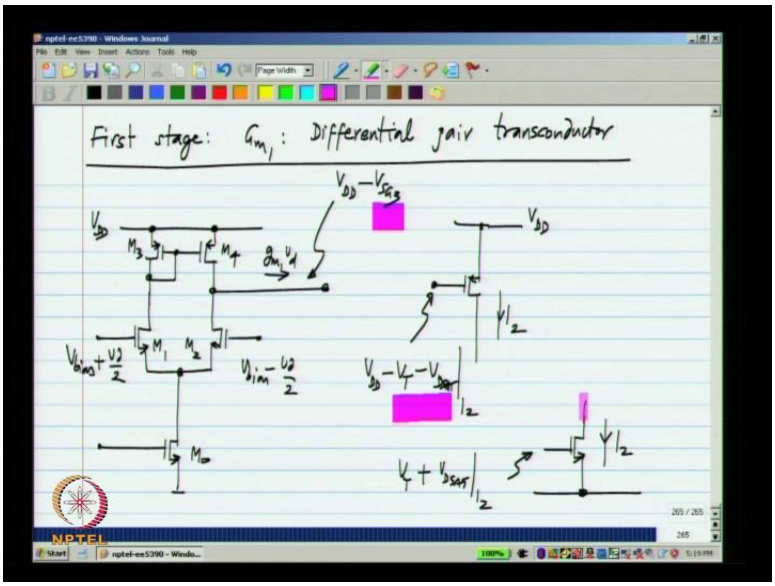

The basically G M 1 will be made by using the differential pair Trans conductor. This is what we have and this is G M 1. We know that, if we have V bias plus V d by 2 and V bias minus V d by 2. There is a current G M 1 V d that tends to flow out if there is some proper termination on this side ok. Now, what do we need here? We need another Trans conductor, voltage control current source around which we connect the integrating capacitor.

Now, what is the Trans conductor that we need to use here? There is a variety of choices, but will try to use the simplest that is possible. And, we recognize that a transistor by itself is a voltage control current source or a Trans conductor. A common source amplifier for instance is nothing but a voltage control current source loaded by a load resistor. So, that is what we will use.

Now, we can use either P Mos or N Mos transistor. We know that the quiescent output voltage here is V d d minus V s g 3. So, typically especially for large values of V d d; this is lot closer to V d d than to ground. Now, let us say you want to have a P Mos, how much source amplifier or a P Mos Trans conductor biased at some current I 2; let us say. Then, the gate needs to be biased at V d d minus V t minus V d sat corresponding to a current I 2.

Instead if you had a N Mos transistor biased at let us say the same current I 2; the voltage would have to be V t, the threshold voltage plus V d sat at a current of I 2. And, you see

that the output voltage of the first stage is lot more suitable for biasing a P Mos transistor than an N Mos transistor. If V d d minus V s g 3 as to be equal to V d V t plus V ds at there is some constraint between V d d V s g 3 V t and so on.

On the contrary, if you want to make this equal to V d d minus V t minus V d sat, V s g 3 has to be equal to V t plus V d sat. And, V s g 3 itself is the threshold voltage of the P Mos transistor plus some over drag. So, all we need is to have the same overdrive for this transistor as well as that transistor and the entire circuit will get biased. So, it is lot easier to interface a P Mos stage to a N Mos differential pair compared to an N Mos second stage. So, for this reason we will use P Mos second stage with an N Mos first stage; that is N Mos differential pair first state.

Now, the other topology is also possible; you can use an N Mos second stage with an N Mos differential pair and that is sometimes used when the supply voltage is very low and you can satisfy this constrains. But usually an N Mos differential pair will be followed by a P Mos common source amplifier. If I say common source amplifier; what it is really? It is a voltage control current source that will use as an amplifier.

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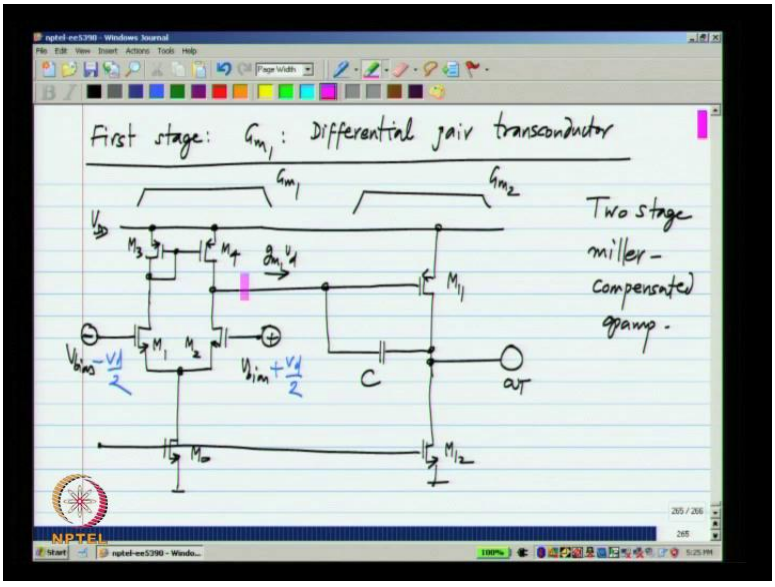

So, my second stage M will be that and I would want as higher DC gain as possible in this as well. So, I will not loaded by a resistive load; I will be loaded by an active current source load. Let me call this M 11 and this is M 12. I can connect it like that and the gate of M 12 is bias from a current mirror. I will assume that if the bias is derived from the

same place that we derive the bias of M naught from. By adjusting the size of M 12 compared to M naught and the direct connected transistor, we can get any current that we want, we have. Now, this is G M 2, this is G M 1. The first stage is a differential pair because we also have to take the difference between the desired and the actual quantities; that is done in the first stage that is why it is a differential G m.

The second stage is simply a single ((Refer Time: 11:17)) one because it has to take the output of the first stage. Across this we need to connect the capacitor C, this is the integrating capacitor C and we have done and this is the output, this is the positive input and that is the negative input. That is obvious from these polarities, this is negative and that is negative. So, the gain from there to the output is positive. So, this is our two-stage opamp. If you recall, it was also called the miller compensated opamp. Now, we already know the small signal parameters of the such a topology; let me put this down again.

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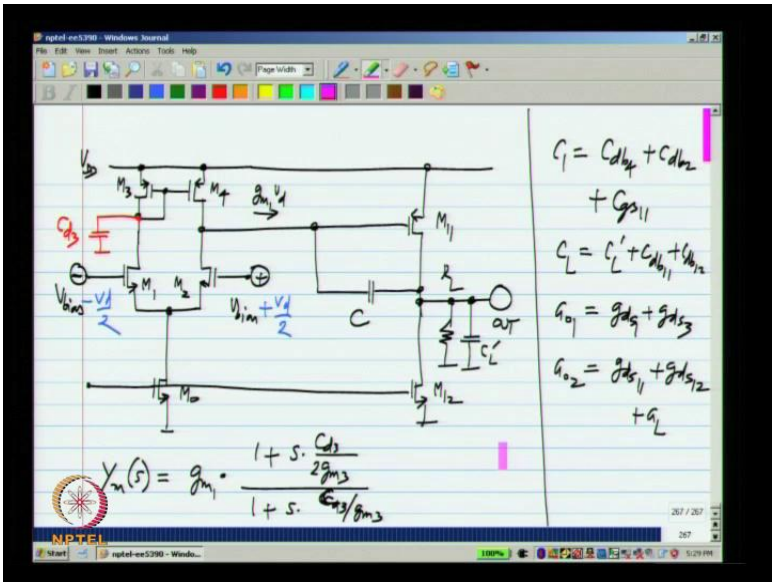

I will show only the output conductance, but if there is a load resistance that can be absorbed into the output conductance G o 2. This is G M 1. Now, what is the transfer function that we had for this for V naught divided by the difference voltage V d or the error voltage V e? We had the DC gain G M 1 G M 2 by G o 1 G o 2 and we had a right of plane 0. And, we had a second-order denominator which we approximately result into to first-order factors s by p 1 and s by p 2. And, the 0 g 1 is at G M 2 by C pole p 1 is at G o 1 by it is proximately at G o 1 by C 1 plus C times G M 2 by G o 2 plus 1. Because

some other terms which we can neglect and the second pole is approximately at G M 2 with this feedback fraction C by C plus C 1 plus G o 2 divided by C L plus series combination of C and C 1.

So, we know all of these things we have to find this for our transistor level opamp. So, the first thing we need to do is to simply identify the values of the different components C 1 C L and C; that we already know G o 1 G o 2 etcetera. And, also one more thing to keep in mind is that, in this diagram we assume G M 1 to be an ideal Trans conductor. In reality, we know that from our analysis of the simple differential pair; between the input is here let us say I apply plus V d by 2 and minus V d by 2. And, the output current that is coming out of the first stage Trans conductor, there is a pole and a 0; that is because of the mirroring. So, this G M 1 has to be replaced by Y M 1 which is the Trans admittance that includes the pole and 0.

So, if we do all of that, we will get the frequency response of our miller compensated two-stage opamp at the transistor level. Let me copy over this picture. So, first of all what is C 1? C 1 is the total capacitance at the output of the first stage and that consists of parasitic capacitances from every transistor that connected there M 4 M 2 and M 11. As usual I will neglect the values of C g ds because the transistor's are operating in saturation region. So, C 1 will be C d b 4 plus C d b 2 plus C g s 11. So, that is what we have this one, that one and that one; remember V d d is small signal ground. Similarly, what is C L?

The total C L will be, whatever load capacitance we connect C L prime plus the parasitic capacitances due to M 11 and M 12. So, we do not usually calculate all these exact values by hand we resort to the simulator. But we need to know how each of those values influences the total capacitance; how the total parameter and which consequently effects the pole value. Now, what is G o 1? G o 1 is the output resistance of the first stage and that will be equal to g d s 1 plus g d s 3; this again we have evaluated. And, g o 2 that is the total conductance at the output of the second stage will be g d s 11 which is due to this transistor M 11 and g d s 12 due to the current source transistor M 12. Whenever, you bias something with the current source, a current source contributes an incremental resistance which appears in parallel.

Now, if you have a load resistance R L to easily get the results; we simply absorbed that into the total conductance at the output of the second stage. The value of C the integrating capacitors known; so, everything is known and also the trans admittance of the first stage is nothing but the DC Trans conductance of the first stage times 1 plus s C d 3 by 2 g m 3 divided by 1 plus s C d 3 by g m 3.

As we found out while discussing the single stage opamp there is a parasitic capacitance C d 3 here; contributed by M 1 M 3 and M 4. And, because that acts on only half through the current, we get a pole under a 0. So, the total transfer function will consist of not this G m 1, but Y m 1 which as a pole under 0 and the two poles here and the 0 over there. So, all we have to do is to substitute the terms and find out what each of these things is.

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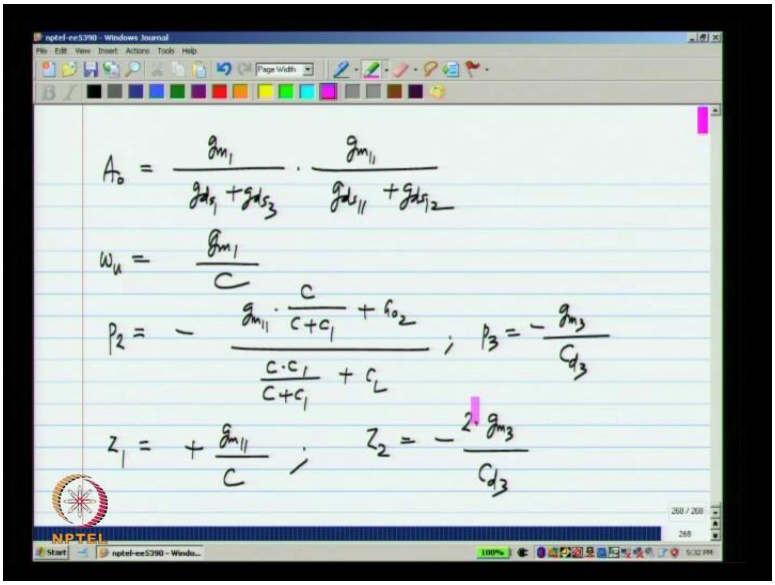

The DC gain is the product of the DC gains of the two stages which is g m 1 by g d s 1 plus g d s 3 times g m 11. Remember, g m 11 is g m 2; I will write that down as well. g m 2 is nothing but g m 11; the trans conductance of this stage. g m 11 by g d s 11 plus g d s 12 and the unity gain frequency should be g m 1 by C. This is what we have calculated and we will place the non-dominant poles and zeros beyond the unity gain frequency.

Now, the non-dominant pole that we have calculated is minus g m 11 C by C plus C 1. C 1 value can be substituted from the expression over here plus the total output conductance g o 2 whatever that is, usually that is negligible. C is combination of C and

C 1 plus the total C L; this is one of the non-dominant poles. In addition to this, we also have the non-dominant pole due to the first stage which is g m 3 by C d 3. Of course, it is in the left half plane.

And, there is a right half plane 0 that we are quite familiar with from our earlier analysis and that is at g m 11 by C. There is also a left half plane 0 due to the first stage which is at minus 2 times g m 3 by C d 3. So, overall we have a dominant pole which is very close to the origin of and we have these non-dominant poles and zeros. We have two non-dominant poles and two non dominant zeros and we should position this; so that our phase margin is a healthy value of a let say 45 degrees or 60 degrees or whatever we desire ok. Now, a couple of things; first of all these expressions are general and any external load that you have either load resistance or load capacitance can be absorbed in to these things. All you have to do is to manipulate the value of C L or G o 2.

Now, what happens to the DC gain? Why is this better for a resistive load compared to the single stage opamps? When we have resistive load it is only the DC gain of the second stage that is affected. The first stage gain is not affected. Now, we can offer to have low gain in the second stage because we have two stages of gain. Let say the second stage is designed for a modest gain of only 10 or even 6 and we get the bulk of our gain from the first stage. So, this way even with a very heavy resistive load, we can get a high DC is gain without increasing the Trans conductance significantly.

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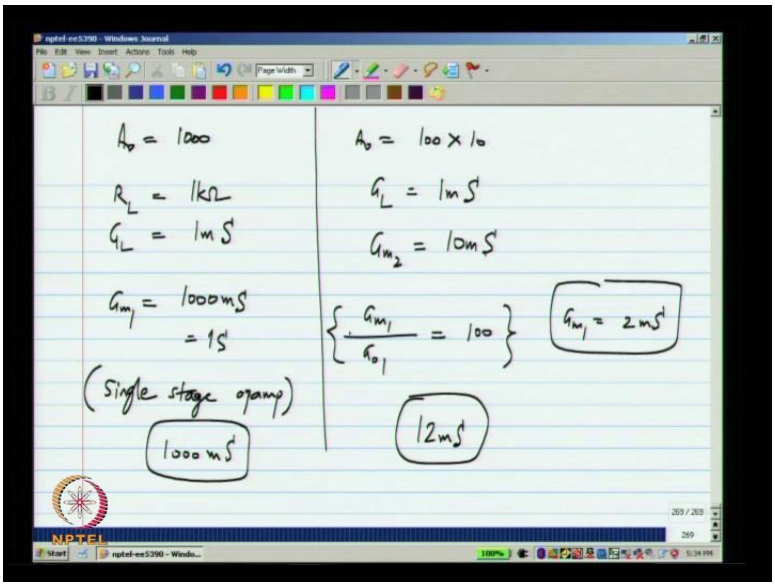

What I mean is, let us say I want a DC gain of 1000. Now, let say my load resistance is 1 kilo ohm or equivalently the load conductance is 1 milli siemens. If I tried this with the single stage opamp, the Trans conductance would have to be 1000 milli siemens or 1 seimen. This is with a single stage opamp. Now, let us say we partition this into 100 from the first stage and 10 from the second stage.

So, again we have the same R L and G L which is 1 milli siemens. Since, the second stage has to offer a gain of only 10 by G m 2 can be 10 milli siemens. And, my G m 1 can be any value that I want; because I have to adjust the value of G m 1 by G o 1 which is independent of the load to be equal to 100. I do not know what G m 1 is going to be apart from stability considerations. I know that G m 1 has to be significantly less than G m 2.

So, let us say I will say G m 1 is 2 milli siemens. So, clearly in this case we have to realize a total Trans conductance of 12 milli siemens. And, here the total is 1000 milli siemens. Now, of course, how much power we burn to realize a given Trans conductance, depends on the topology. But just from the basics of mass transistors, we know that if you want a larger G m, you have to have larger transistors operating at higher currents. So, to get 1000 milli siemens, you have to burn significantly higher power turn to get 12 milli siemens. So, it is not possible to drive resistive loads and have high gains to the single stage opamp. Whereas, it is quite easily possible with a two-stage opamp; that is the reason two-stage opamps are very popular and very widely used.

Now, these summarize the small signal DC and AC performance of the opamp and we have a higher DC gain. And, we have number of parasitic poles and we know what to do with them. We have to place them sufficiently beyond the unity loop gain frequency; of whatever feedback loop we operate that. Now, let us evaluate some other relevant parameters of this opamp like the noise of sets slew right in the swing.

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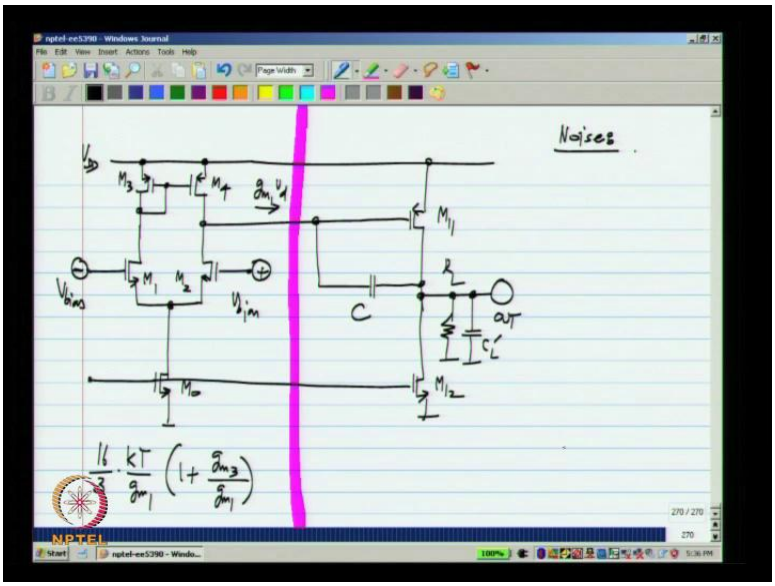

Now, let us first consider the noise. We know that the input referred noise of the single stage opamp alone is 16 by 3 k t by G m 1. Where G m 1 refers to m 1 and m 2; 1 plus G m 3 by G m 1.

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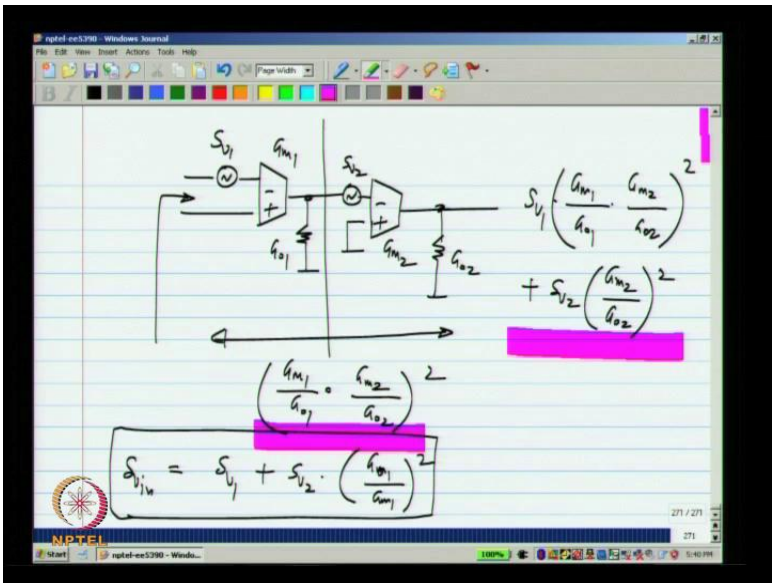

Now, let us say we have a two stage structure. We already know the input referred noise of the first stage. Let me call it has V 1 and this is G m 1 G o 1. One thing I will do is, I will also ignore all the capacitors while calculating the input noise spectral density. So, it will be valid only for low frequencies, but that is ok; that serves usually good enough

estimate of the noise. So, let us say this is a G m 2. Now, I do not have to recalculate noise from the first stage. So, what I will do is I will calculate the effect of the second stage; either on its inputs or on its output. So, let us say evaluate the second stage noise refer to its input and as I mentioned I will remove the capacitor C. Now, what happens? I will have some S v 2. So, that is some voltage noise is added over there.

So, what will be the total input referred noise? It is a quite easy to see. So, one way to do that is to simply calculate the total output noise first. From S v 1 we have gain of G m 1 by G o 1 times G m 2 by G o 2 and this is a spectral density. So, the total spectral density at the output due to S v 1 will be G m 1 by G o 1 G m 2 by G o 2 square. And, due to this S v 2 the input referred noise of the second stage will have S v 2 times G m 2 by G o 2 square. And, the overall gain we know is G m 1 by G o 1 times G m 2 by G o 2 whole square.

So, if I want to represent this effect of both these noise sources with the single input source here; what I have to do is to divide this by that one. So, I will have S v 1 adding directly; that is what we expect. S v 1 simply adds to the input plus S v 2 G o 1 by G m 1 squared. As I said many times, when you have a cascade of multiple stages the input referred noise will be the input referred noise of the first stage plus the input referred noise of the second stage divided by square of the gain of the first stage. Input referred noise of the third stage divided by square of the product of first and second stage gain and so on. And, if these games are significant; then, only the contributions of the first stage will be significant all others will be insignificant and that is apparent from this expression as well.

Because we have S v 2 times G o 1 by G o 1 whole square which means that S v 2 is attenuated by a large factor. One it is referred to the input G o 1 by G m 1 is nothing but the inverse of the DC gain of the first stage which could be 50 or 100 or something. So, effectively when we calculate the input referred noise; all that matters is the noise of the Trans conductance G m 1. The input referred noise of the two-stage opamp will be exactly the same as the input referred noise of the simple single stage differential pair opamp. Any extra contribution from the second stage will be quite negligible.

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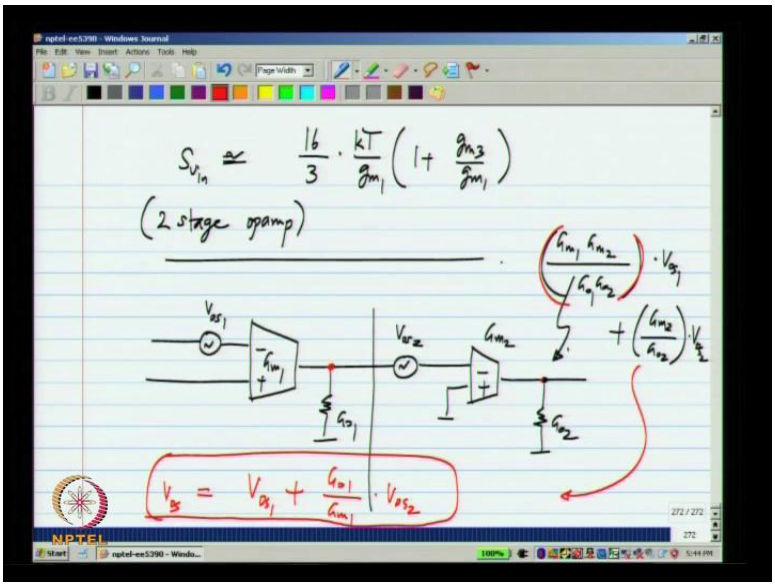

Now, the next thing will consider is the input referred offset. Now, what do we mean by the offset here? Let us take the example of a unity gain follower for instance. Now, if I apply an input, the output should the exactly follow the input, but because of the offset there will be a difference between the input and output. So, that is the offset. Now, we have already calculated the offset of the first stage, right. Now, just ((Refer Time: 31:47)) with noise, any mismatch contribution from the second stage will be divided by the gain of the first stage and will not matter when refer to the input.

Again, let me consider the two-stage structure, G m 1. Let us say we have some V o s 1 and we have G o 1 over here and have here S 2. Offset is by definition DC and I do not have to include any capacitors in the calculation, I have G m 2 and G o 2. So, V o s 2 is the input referred offset of the second stage V o s 1 is the input referred offset of the first stage. So, the total offset at the output will be G m 1 G m 2 by G o 1 G o 2 times V o s 1 plus G m 2 by G o 2 times V o s 2.

Now, when we refer this to a single offset source of the input, we divide this by the overall gain which is this number. So, V o s the input would be V o s 1; because this from the first stage it adds directly plus G o 1 by G m 1 times V o s 2. Just as with noise V o s 2 is divided by the gain of the first stage. So, when we compute the input refer offset, the contribution of the second stage will be quite negligible.

So, again the offset of this is the same as the offset of the single stage opamp with the differential pair. That is the random offset of the two stage miller compensated opamp is the same as the random offset of the first stage differential pair. Which is of course, determine by the differential pair transistor and the load transistor.

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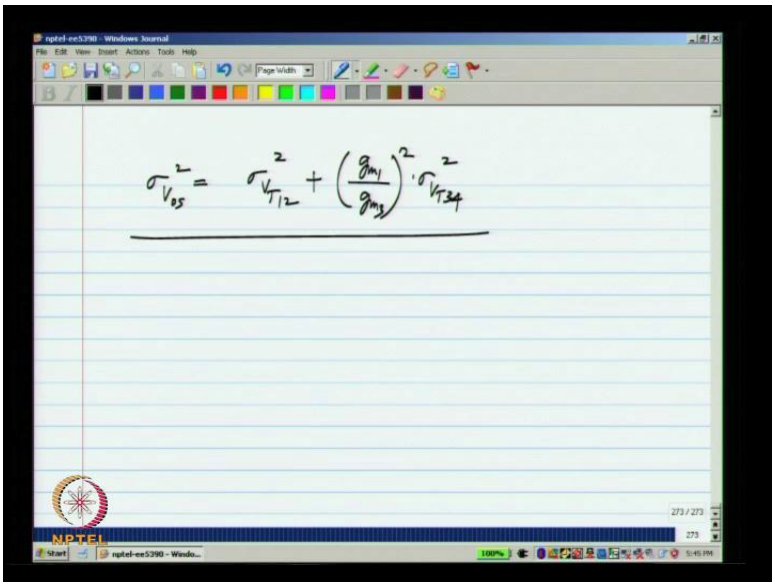

So, the random offset variance will be sigma V T 1 2 square plus G m 1 by G m 3 square times sigma V T 3 4 square.

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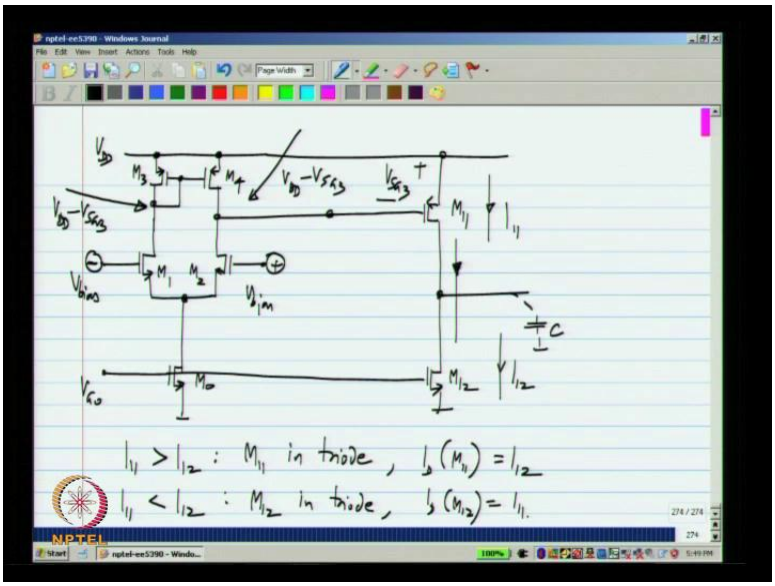

Now, in case of the single stage opamp that is we are considering only this part. The operating point here was the same as the operating point there in absence of offset. That is when the inputs are V bias that drain of M 4 and M 3 are the same voltage by symmetry. And, because of the offset it will be different and the input referred offset can be calculated purely on the basis of random mismatch.

Now, in case of that two stage opamp, let me just not show the load explicitly, but it can be there. What will be this value? When the inputs are at V bias and there is perfect symmetry between two offset the differential pair. Now, this voltage and that voltage will be the same as each other by symmetry. So, this is V d d minus V s g 3 and that is V d d minus V s g 3 as well.

And, let me call this voltage V g 0 at a the voltage V g 0 M 12 tends to carry a current I 12, if it is in saturation region. This pair lost of volts only in saturation region and this current I 12 will be carried if it is in saturation region. Now, if you look at this we have M 11 which behaves like a current source and M 12 which behaves like a current source connected together. Obviously, the current in M 11 has to be equal to the current M 12. Now, can both of those in saturation, it is possible if the voltage happens to be bias in the middle.

Now, what will be the current that M 11 carries if it happens to be saturation region? So, to imagine this perhaps first of all we are discussing DC situation; so, we can neglect the capacitor. So, let us say connect the drain of M 12 to be V d d and M 11 to ground. In this case, these transistors will be guaranteed to be saturation and I have some current I 12 here, which is the intended bias current for the second stage.

Now, let us say with a gate voltage V d d minus V s g 3 or source gate voltage of V s g 3 M 11 carries some current I 11. Now, what happens if we connect these two together? The current has to be the same. It does not matter what the M 1 tended to carry, if it was in saturation region M 12 tended to carry it was in saturation. When you connect them together like this, they have to be the same. If I 11 is greater than I 12; that is saturation current of M 11 is more than the saturation current of M 12.

What happens is, let us say this voltage start from the somewhere in the middle; so, that board transistors are in saturation region. A net current of I 11 minus I 12 will flow into the parasitic capacitance that is at the output. So, this voltage will keep on arising. And,

finally, M 11 will reach the triode region and the current in M 11 will reduce to be equal to I 12. Similarly, if I 11 happens to be less than I 12, the voltage will fall down and till M 12 is triode and idea of M 12 equals I 11. Now, this is visualize very easily graphically.

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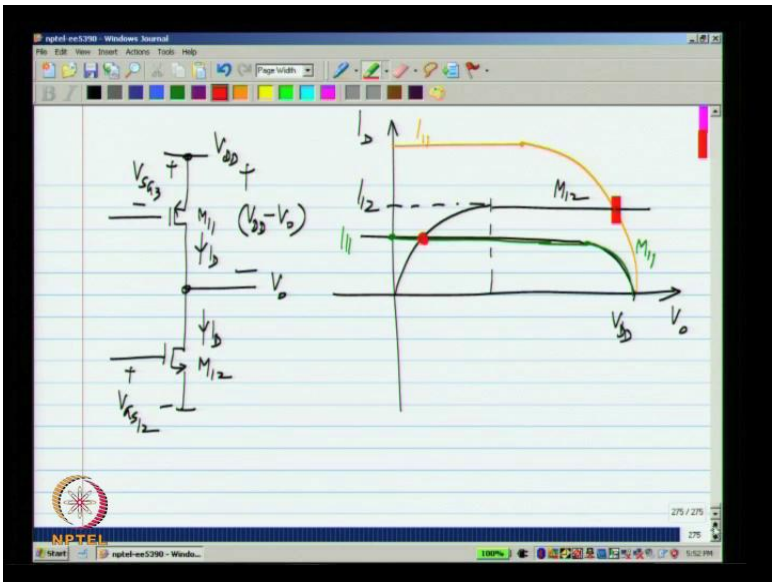

This operates with certain V s g and this operator with the certain V g s 12 and let us say the output voltages V out. I will draw the I d V d s characteristics; let us say that is I d, if I draw the I d V d s characteristics of M 12, what I will get? Is the usual output characteristics of the ((Refer Time: 39:47)) transistor. Let me show it with the very small output conductance. This is V o; V o is nothing but V d s of M 12. Now, I will also draw I d versus V o characteristics; I know that the V s d of M 11 is V d d minus V naught.

So, I d versus V o characteristics is nothing but I d versus V s d characteristics, but with the curve flipped around at V d d. You would have done this calculation when you are calculating the characteristics of ((Refer Time: 40:30)) C Mos inverter. So, if this is V d d; V d d minus V naught is the V s d of that and that will look something like that. So, this is what I call I 12; the saturation current of M 12, this is for M 12. I can show this in different color and this is for M 11 and that is I 11. Now, what will be the value of V naught? It will be the point of intersection. We can clearly see that, if I 11 is smaller than I 12 than M 12 will go into the triode region. Similarly, if M 11 characteristics happened

to be something like that; that is I 11 happens to be more than I 12, then M 11 go in to triode region.

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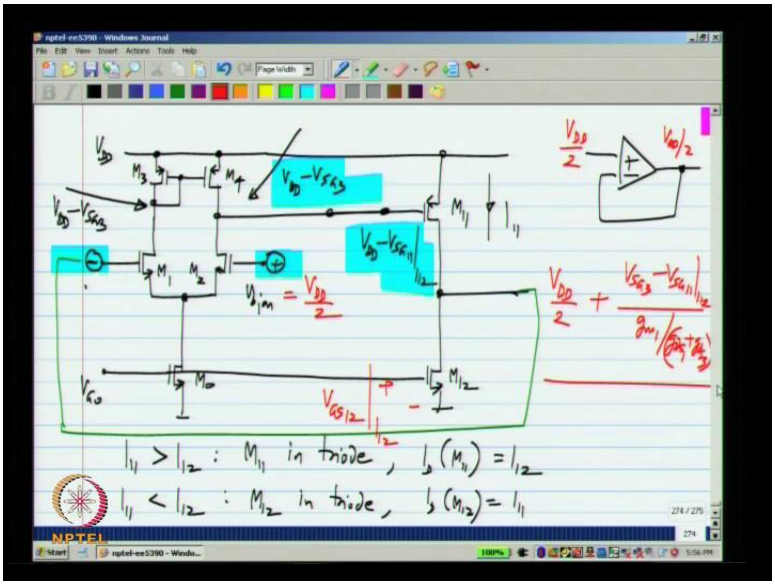

So, one of this two will be in triode region if I 11 is not equal to I 12. Now, let us connect this in feedback and then see what happens? Let us say we connect this in unity feedback. Now, here we are talking about the case where there is no mismatch between transistors. Let me connect it up in unity feedback like that and apply V bias to that stage and let us say V bias somewhere in the middle of the supply. Let us say V d d by 2. Now, what we expect is the opamp is ideal if this is V d d by 2; I would expect V d d by 2 over there.

Now, clearly the currents in M 11 and M 12 have to be equal to each other that is just from Kirchhoff's law here. And, also if this is around V d d by 2 and this is V d d board transistor will be in saturation region. You imagine large V d d; so, the V d s of M 11 and M 12 were very large, so, they will be in saturation region. Now, if the two transistor are in saturation region and there currents are equal; the voltage here will be V g s 12, that is require for current of I 12. And, the voltage here will be V s g 3 that is required for a current of I 12. Now, we know that in the balance conditioned the differential pair by itself would give you V d d by minus V s g 3.

The voltage required at the gate of M 11 would be V d d minus V s g 11 for a current of I 12, whatever that is. We say that the two currents are same of course, and they are both

in saturation region. Now, the differential pair will tend to given output of V d d minus V s g 3 when it is balanced. Let say the V d d minus V s g 3 is not equal to V d d minus V s g 11 require for a current I 12. So, what happens when we connect this two together? The output of the first stage has to move from its natural value of V d d minus V s g 3 to the gate voltage required for a M 11 to carry a connect of I 12. So, what I am saying here is that the first stage differential pair would naturally carry some current. But it has to change from there different values which will make that transistor M 11arry a current of I 12.

Now, how will that happen? The only way for that to happen is for the differential pair to have a non zero input voltage. Because the input was 0 the output to the V d d minus V s g 3. So, this of course, means that there is a difference between this one and that one. So, the output will not be add V d d by 2, but it V d d 2 plus some delta V and what will be the delta V? It will be the change required output at the first stage which is V s g 3 minus V s g 11 for a current of I 12 divided by the gain of that stage which is G m 1 by g d s 1 plus g d s 3. Please go through the reasoning carefully. What I am saying here is that, the first stage has some natural output voltage when you connected up in feedback loop with a second stage, the first stage output has to change. So that the second stage carries a current of I 12 which is what to supply by the current source of the second stage.

And, because it has to change the input voltage of differential pair has to change which means that there is an offset. Now, this offset is not because of random is mismatch between the transistors; this is because output voltage of first stage is not equal to the input voltage required by the second stage to carry a current of I 12. And, this is known as a systematic offset and the way to avoid this is quite obvious. If you make V s g 3 equal to be V s g 11 for current of I 12 than the first stage output does not have to change when you connected to the second stage and connected in feedback loop. So, it will make sure that there is no systematic offset.

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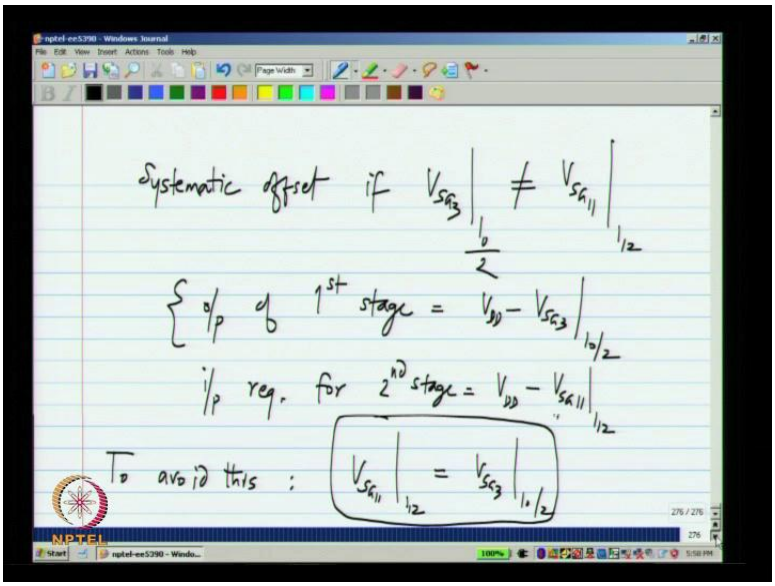

V s g 3 for a connect of I naught by 2 is not equal to V s g 11 for a connect of I 12. This is because output of first stage is V d d minus V s g 3 for a current I naught by 2. And, the input required for the second stage V d d minus V s g 11 by current of I 12. And, to avoid this you make deliberately V s g 11 current of I 12 equal to V s g 3 for a current of I naught by 2. Now, can we do this? We can certainly do that because M 11 and M 3 and M 4 are all p Mos transistors.

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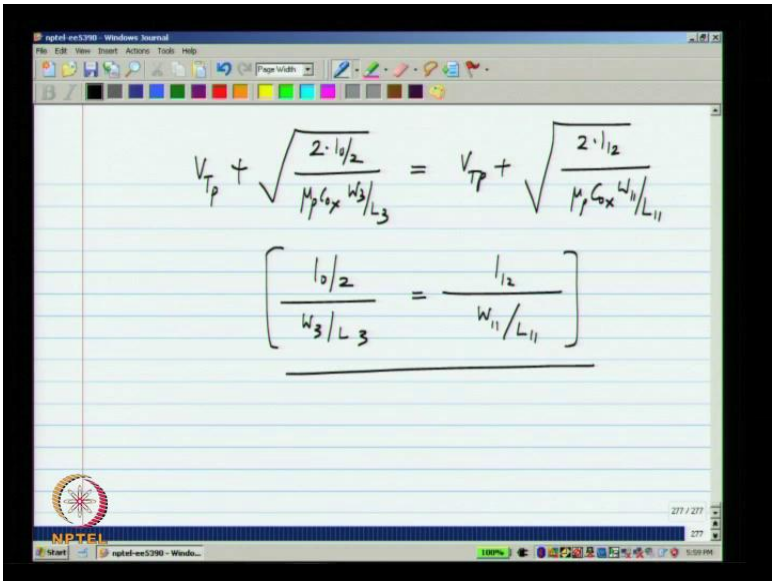

What we have to make sure is that, V T both have the same V T; V T plus square root 2 times I naught by 2 divided by mu p C o X W 3 by L 3 should be equal to V T p plus square root 2 times I 12 divided by mu p C o X W 11 by I 11. What this means is of course, I naught by 2 divided by W 3 by L 3 equals I 12 divided by W 11 by L 11. This is usually refer to as the transistor M 3 and M 4 are transistor M 11, operating at identical current densities. If you make length equal the width ratio will be equal to the current ratio between the transistor M 11 and the transistors M 3 and M 4.

Now, this is done to avoid systematic offset. If you do not do this is, there will be a systematic offset which is equal to the difference in the V s g divided by the gain of the first stage. It turns out that, this is not always possible to do; sometimes is not easy to arrange this. So, in cases where the gain of the first stage is very very large; the systematic offset will be very small anyway and you do not have to do this. This is the gain of the first stage is modest and you are looking for very small offsets. You go on and make the current density of the transistor M 11; that is the second stage transistor equal to the transistors M 3 and M 4 and you will not have any systematic offset. The offset will be governed only by random mismatch of the transistor in the first stage.

So, what we have done is to take the two states opamp and the realize it at the transistor level; it is quite convenient. You take the single stage opamp and follow it up with the common source amplifier loaded by the current source. Very easy to calculate the small signal parameters and noise and offset and so on. Noise and offset contributed primarily by the first stage and systematic offset will be eliminated by equalizing the current densities. In the next lecture, we will calculate the slew rate, swing limit etcetera of this opamp and compare it to the other opamp; that we have discussed earlier.

Thank you.