Analog Integrated Circuit Design
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Lecture - 35
Folded Cascode Opamp

Hello and welcome to lecture 35 of Analog Integrated Circuit Design, in the previous lecture we analyze the telescopic cascode opamp in great detail. Also we came up with a different topology by using a p MOS cascode device, or p MOS common gate amplifier with M MOS differential pair, we had this topology, which first called the folded cascode opamp, in this lecture we analyze this in detail.

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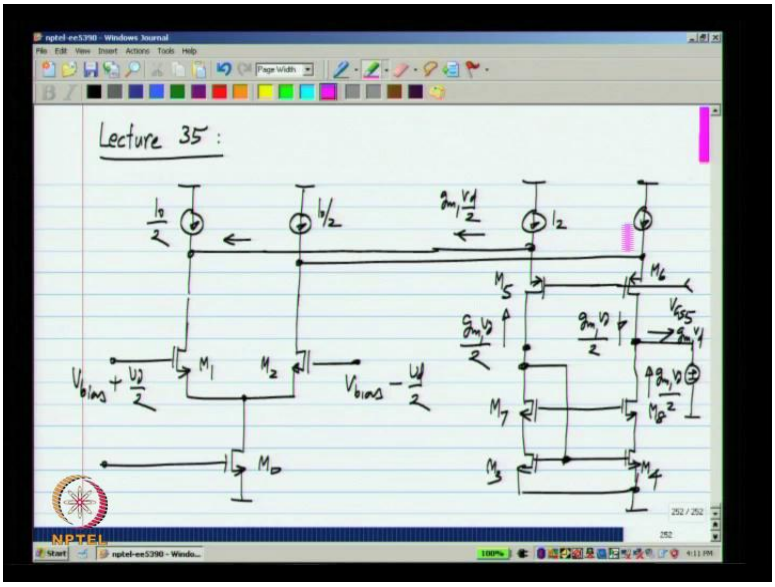

This is the circuit we have the M MOS differential pair followed by a p MOS cascode device, and in n MOS current mirror to take the current from this side and combine it, and given output of g m 1 v d, where v d is the differential input. Now, you see that the bias sources I naught by 2 used to subtract the current from M 1, and the bias sources I 2 of these cascode devices are in parallel, so they will be combine into a single source and implemented with MOS transistors.

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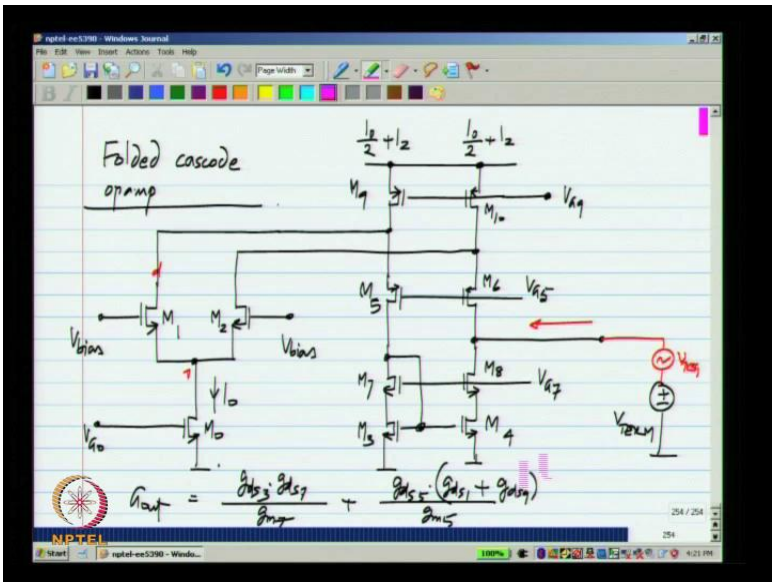

I will draw the circuit including that modification, these are current source devices, these are the cascode devices M 1, M 2, M 5, M 6, M 0, and we have the M MOS cascode current mirror. The gate voltage is some bias voltage generate from a p MOS current mirror, it could be something other ((Refer Time: 03:18)) I will not show it here, but that is how it is generate.

Similarly, V G 0 is generated in the same way, so this forms current source I 0 and M 9 and M 10 implement a current source of I naught by 2 plus I 2, the output is taken from here. It can be loaded by a capacitor, if you are implementing an opamp or it could be loaded by just a voltage source, when we are testing it as a trans conductor by monitoring the output current, and these are fixed bias voltages to bias the common gate amplifier.

So, this were folded cascode opamp, now compare to the telescopic cascode opamp, we have these two extra devices M 9 and M 10, in the telescopic cascode opamp everything was tacked on top of each other. And we did not need these extra sources for biasing, but now we do, we have to see what the effect of those things are, because of we are already analyze the cascode opamp in detail. I will not going into every detail of this particular opamp, I will only analyze those aspects, which are different from this compared to the telescopic cascode.

So, first of all let me draw the quiescent currents, write down the quiescent currents here, in the two arms it will be I naught by 2 and I naught by 2, and in M 5 and M 6 and these

other transistors. It will be I 2 and I 2, now if I apply an incremental voltage, v d by 2 and minus v d by 2 to the differential pair, a current in M 1 increases by g M 1 v d by 2 this voltage is alMOSt at 0, v 1 with this symmetrical loads. As, we analyze it earlier, and this is at minus g M 1 v d by 2, now if you work it out you will see that in this transistor in M 6, we will have I 2 plus g M 1 v d by 2 that comes from Kirchhoff law this node.

And similarly, in M 5 will have I 2 minus g m 1 v d by 2, and it also gets mirrored in M 4 and M 8, so finally here we will have I 2 minus g M 1 v d by 2 and I out as we knew was simply g M 1 times v d. Exactly, the same as before, so the trans conductance of the folded cascode opamp is also g m 1, it is simply the trans conductance of the input differential pair.

This is not very surprising, because all we have done is to use current buffers with unity gain after the differential pair, now the important thing is the output conductance, because the high output conductance is the region we go to cascode topologies. Let me remove all of these, now by symmetry just like in the differential pair, and in the telescopic cascode opamp, the voltage here and there are the same in the quiescent condition.

Let me remove the load all together if the devices are exactly matched, the voltage on the drain of M 7, and at the drain of M 8 will be exactly the same, you can assume them to be different, and come up with the contradiction as usual. And that is the voltage, with which we will terminate the trans conductor, let us say to this I had a test voltage, v test and we have to find out, how much current will flow there. Now, it turns out that the situation is exactly the same as before, in fact the transistors are numbered, so that they are functionally identical to the similar number transistors.

M 1 and the M 2 are the differential pair, M 3 and M 4 are the main current mirror, M 5 and M 6 are the cascodes for the differential pair, M 7 and M 8 are the cascodes for the current mirror, we also have these extra transistors M 9 and M 10. Now, before what we had was that the contribution of the current source to the output conductance was simply the output conductance to the cascode source. So, we have g out to be g d s 3 g d s 7 by g m 7, that is the contribution due to this, and the contribution due to the differential pair

was g d s 5, g d s 1 divided by g m 5, that is because the total conductance in the source of M 5 was contributed by the differential pair.

Now, to the addition to that we see that we have another transistors M 9 over here, so it turns out, that the output conductance due to the differential pair will also include the output conductance of these current source transistors M 9 and M 10. So, I will not analyze this please go add and do that, and you will find that this g d s 9 simply adds to g d s 1, we have g d s 1 looking this way. The actual situation is complicated, because of the asymmetric injection, and this way what we earlier, but the final result is that g d s 1 will appear in parallel with g d s 9.

So, the total output conductance will be that much, the only difference is that, because of this extra current source transistors, we also have an additional output conductance, which will reduce the d c gain, so this is in fact a disadvantage.

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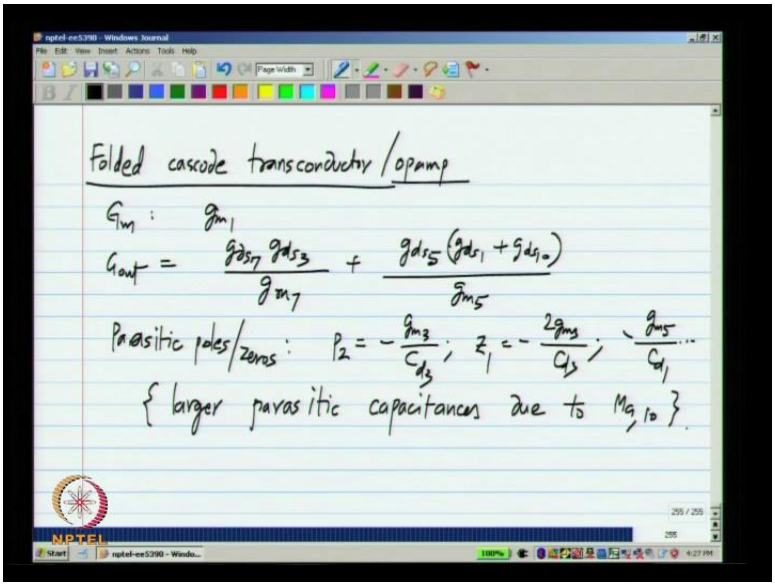

We have the folded cascode trans conductor, and when it is loaded by capacitor c, it becomes a folded cascode opamp of unity gain frequency g m 1 by c, so that the trans conductance of this is g m 1 the output conductance is that one. Now, what about the frequency response, we see that the number of nodes in the circuit is exactly the same as before. And qualitatively they are also the same, except that there are these two transistors M 9 and M 10, so we will have parasitic capacitance at this node.

So, we will have this, which I have been calling c d 3, this causes a pole in the current mirror, so if you inject a current into this the output will be that current times 1 over 1 plus s by this pole. And the pole value we know is g m 3 by c d 3, and because it acts only one half of the current, the current from M 1, they also be a 0 at twice that frequency.

This is exactly the same as what was the case, with the simple differential pair opamp and also the telescopic cascode opamp, in addition to that we have c d 1, c d 2, and here I should call this c s 7 and c s 8. Each of these capacitors c d 1, c d 2, c s 7, c s 8 are at the input nodes of common gate amplifiers, and the input resistance of the common gate amplifier is simply 1 over g m of the cascoding device.

So, each of these will create poles of value g m 7 by c s 7, g m 8 by c s 8, g m 5 by c d 1, g m 6 by c d 2, now there is an additional complication, because this particular pole c s 7 and g m 7 is inside this local feedback loop. And also all these poles from the lower side in the current mirror will act only onem half of the current they will act only the current from the M 1 not from M 2, so they will also create additional 0's, they will have to be take into an account, it is just to comber some to calculate.

For now, we will just be satisfied with saying that there will be poles at these frequencies, and also some additional 0's at similar frequency. Now, this pole at the source of M 5 and M 6 due to c d 1 and c d 2, they act on both the current from M 1, and the current from M 2. So, they will be pole of value g M 5 divided by c d 1 in the transfer function, so qualitatively the results are exactly the same as for the telescopic cascode opamp.

One difference is that because of these additional transistors we also get additional parasitic capacitances before c d 1 consisted of c d b of M 1, c s b of M 5, c g s of M 5, now in addition to these we also have c d b of M 9. So, while qualitatively it is the same the parasitic capacitance value will be higher, and so pole frequency will be at a lower value, also note that these transistors M 9 and M 10 carry large currents compare to M 1 M 2 or these other transistors.

So, they tend to be larger to produce larger currents, we have to have larger transistors, so their parasitic capacitance also tends to be larger and the poles will be further post to lower frequencies. So, the folded cascode has similar parasitic poles as the telescopic

cascode, but dealt into be at lower frequencies, so overall the telescopic cascode will be slower in that. If you have parasitic poles at lower frequencies, you have to push the unity gain frequency to a sufficiently low value, where you have enough phase much. These are the non nominate poles in 0's, and then many more of the type of g m 5 by c d 1 and so on, but we will have larger parasitic capacitances due to M 9 and M 10. First of all there will be additional, and the parasitic capacitance due to M 9 and M 10 tend to be larger than those of other transistors.

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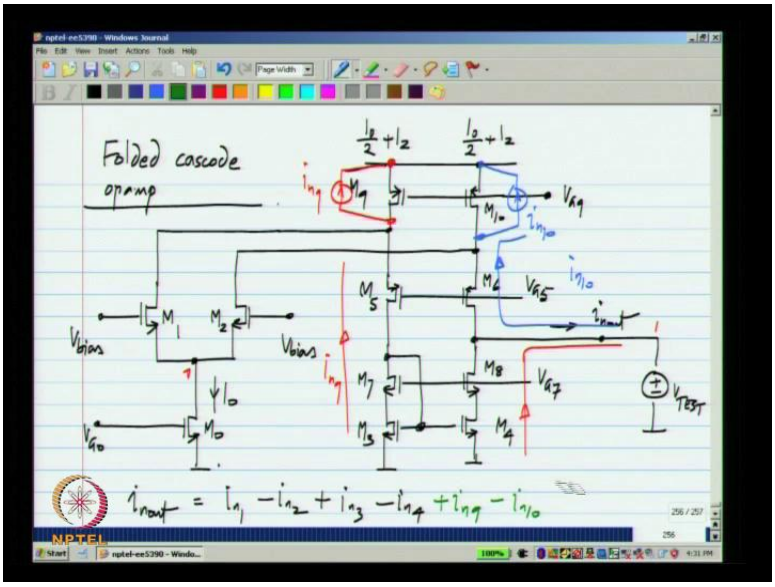

And the next thing is noise and offset, usually they have similar behavior, so that is why we treat them together, as before we evaluate the output noise of the trans conductor operating into a voltage source load. Now, just as before the noise from the cascode transistors the node reached the output and noise from the differential pair, as well as the current mirror M 3 and M 4 reach the output in their entirety they will contribute completely to the output noise.

I am not going to work this out again, but please work it out for these individual transistors M 1 and M, 2 M 3, M 4, M 5 and M 6 and M 7 and M 8 the arguments are very similar to what we had earlier. Now, in addition to those transistors we also have transistors M 9 and M 10, we will see what happens to the noise from those devices. Let us say I have this noise I n 9, what happen to it, the incremental current I n 9 is applied at the input of this common gate amplifier M 5.

So, I n 9 flows that way it will get mirrored in this current mirror, so it will flow that way, and it will flow to the output, similarly the noise current of M 10 I n 10, as you can see this is applied to the input of the common gate amplifier M 6. So, it will go entirely into the current before, because the common gate amplifier or the current buffer presents very low input impedance.

So, you apply a current in the input the same current appears at the output of the current buffer, so I n 10 appears there, now as usual please do the analysis including g d s and so on. I assumed that there is no g d s at all, so all of this simply appears through M 6 and at the output. Now, the contribution of M 1 for instance can be split into two parts, the part is connected to the tail node will not contribute anything, the part that is connected here, will go through the current mirror and contribute to the output.

So, I will not work out all those things again, but I will just say that the output current will be I n 1 minus I n 2 plus I n 3 minus I n 4, this part is exactly the same as before in addition to this, we will also have plus I n 9 minus I n 10. These are due to the current source, which are used to bias the p MOS cascode as well as the current source is used to subtract the bias from the input differential pair, so what is the output noise spectral density is the sum of the spectral density of all these.

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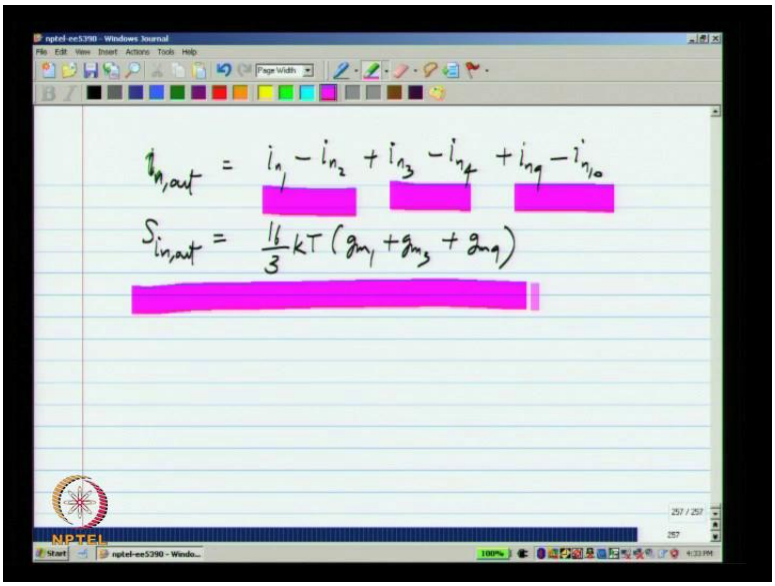

The spectral density is of these two are identical, these two are identical and those two are identical, we will end up getting 16 by 3 k t g m 1, due to the first pair g m 3 due to

the second pair g m 9 due to the third pair. So, first of all there is extra noise, the noise from devices M 9 and M 10, also M 9 and M 10 carry a large current, so they also at tend to have a larger g m.

They carry a larger current than either the differential pair transistors or the other cascode current mirror transistor, so they also have larger noise they tend to have a larger g m. It is possible to design them with the small g m, but that needs I over triode voltage and compromise the swing limit, so that is the story with the noise.

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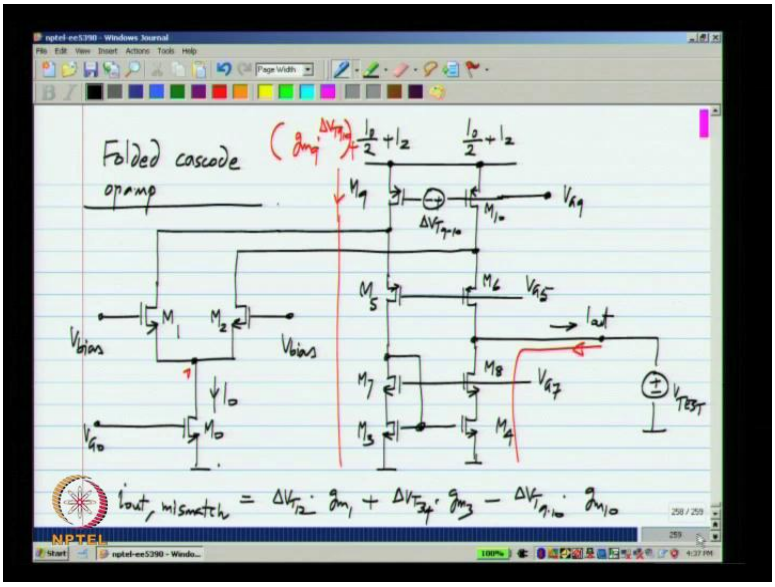

Let us see what happens to offset, again there will be offset between the pairs in M 1 and M 2, M 3, M 4, M 5, M 6 and 7 and M 8, and just as before the contributions from the cascode devices M 5, M 6, M 7, M 8 will be 0. And the input pair will contribute completely to the output, and this pair also contribute exactly the same as before, so I will not work it out, but just as practice please do, so the output current due to mismatch.

Is delta v t 1 2 times g m 1 delta v t 1 2 is simply being applied at the input of the trans conductor plus delta v t 3 4 times g m 3, it is applied here and comes to the output with the trans conductance. So, g m 4 which is the same as g m 3m as usual we have to take care of these extra devices we have to see what happens due to the o s change, now let us say I have a mismatch between these two transistors.

First of all if there is no mismatch at all this will be biased from a current mirror, such that there is a current I naught 2 plus I 2 and M 9, and I naught by 2 plus I 2 in M 10. And I will represent the mismatch as though it is acting only on M 9, it is the mismatch between the two transistors that we are concerned about. Now, you see that the gate voltage of M 10 is a V G 9, and the actual gate voltage M 9 is at V G 9 minus delta v t 9 10, so this of course, as a representation of the changed v t the difference in v t between M 9 and M 10.

So, what will these two compare to the idle current of I naught by 2 plus I 2, they will be an incremental current, which is given by g M 9 delta v t 9 10, so that we will get added onto this flowing in the downwards direction. So, what happens to this incremental current the other part remains the same as before, so we will examine only the incremental part of the current.

And that goes into the cascode transistor or common gate amplifier M 5 through the current mirror and comes to the output, in other words it goes here, and then gets mirrored and its run from the output this current equals g m 9 times delta v t 9 10. So, in addition to these contributions we will also have minus delta v t 9 10 times g m 10, and if we divide the entire result by g m 1m and take the variance to get the input referred offset.

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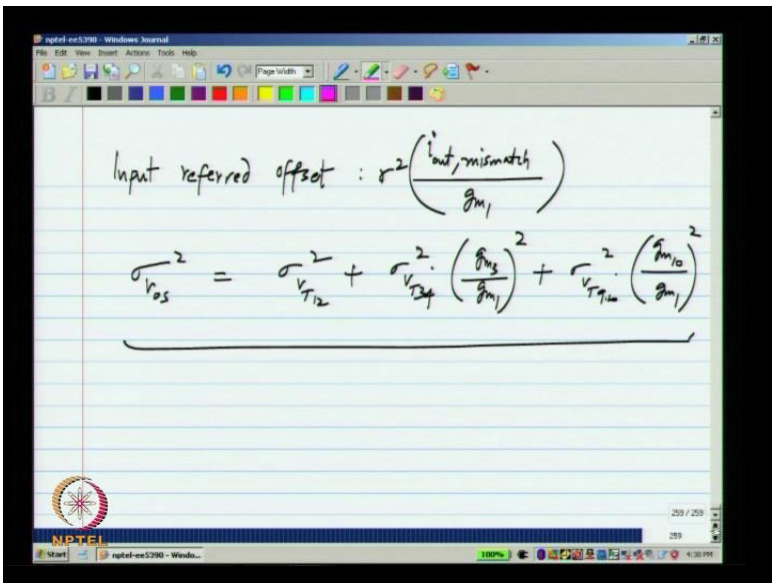

The variance of input referred offset is nothing but, this mismatch in duets output current divided by g m 1, and the sigma square of that one. What will have is sigma v over square the variance of input referred offset is sigma v t 1 2 square, which appears directly as usual, sigma v t 3 4 square multiplied by g m 3 by g m 1 square. And also sigma v t 9 10 square times g m 10 by g m 1 square, so just as with noise there is the extra term due to the current source transistors M 9 and M 10.

And as before we observe that g m 9 tends to be large value, because of the larger currents in those transistors, so the contribution of mismatch from the these current sources can be significant. So, what we have got by changing the n MOS cascode devices to p MOS as to extra devices, and they contribute to d c gain they reduce the d c gain, because they contribute to the output conductance. They also increase the value of the input referred noise, and the input referred offset voltage, what other affect do they have, so for that we will calculate the other large signal parameters which are the s quirate and the swing.

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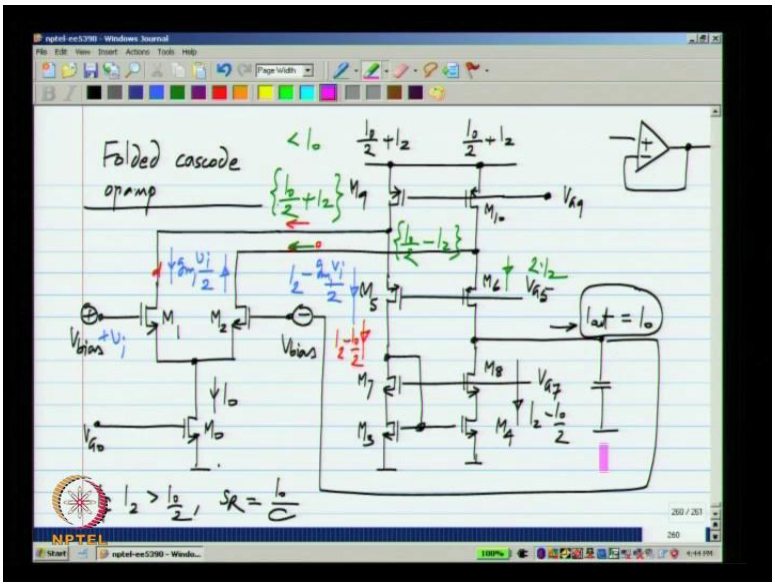

Let us first calculate the quret, I have the opamp and I will assume a unity feedback configuration, though that it is not necessary, this is the minus input terminal I will connect it to the output, basically I am making this amplifier. And I apply input step v I what happens then, as usual this voltage does not change immediately, so we have an incremental current g m 1, v I by 2 going in this direction.

And the current in M 5 would be I 2 minus g m v r by 2, and current in the M 6 would be I 2 plus g M 1 v I divided by 2, as we go on increasing the value of v I, this current will go on increasing, but clearly it cannot increase beyond the tail current I naught. So, at some point we will have I naught here, and nothing here that will be just 0, so under those conditions the current here will be I 2 minus I naught by 2 this fine, and the current in this arm would be I 2 plus I naught by 2.

So, what will be the rate of change of the output, I 2 minus I naught by 2 will flow through M 8 and M 4, so what goes to the output will be equal to I naught, so it appears to be exactly the same as before. Now, this makes one particular assumption, this calculation, what we have assume is that this value of I 2 is greater than I naught by 2, so that is what we assume here.

Now, so far we have not made any assumptions about the value of I 2, now we see that we will get a current of I 2 minus I naught by 2 flowing through M 5. Only if I 2 is greater than I naught by 2 if I 2 happen to be less than I naught by 2, nothing will flow here the transistor M 9 will go off into the triode region and nothing will flow through these.

So, if I 2 is greater than I naught by 2, the square root will be I naught divided by c, what happens if I 2 is less than I naught by 2, as you increase the magnitude of v I at some point this g M 1 v I by 2, this current in M 1 will go on increasing. Now, v 1 before it reaches a value of I naught, it reaches value of I naught by 2 plus I, remember now I 2 is less than I naught by 2.

So, this entire number is less than I naught this current flowing in here is less than I naught, at that point what happens, if you have I naught by 2 plus I 2, and I naught two by I 2 coming here. So, the current in M 5 is 0, and so, the current through this is also 0, let us calculate the current through this part that will be I naught by 2 minus I 2.

So, the net current flowing through M 6 is the difference of I naught by 2 plus I 2, and I naught by 2 minus I 2, so what is that that number is simply two times I 2. And no current is flowing through M 8 and M 4, because this side is off there is no current flowing here either, so two times I 2 will flow into the output capacitor and that will be the maximum rate of change of the output voltage.

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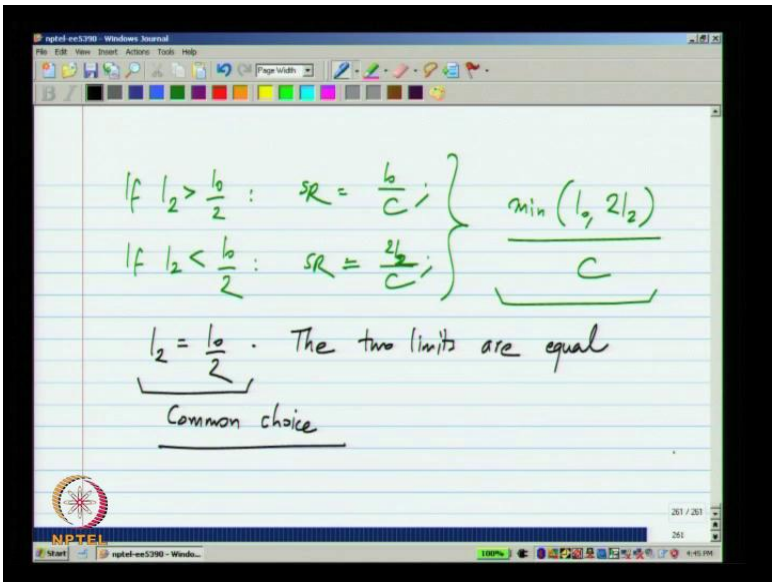

So, what we have is if I 2 is greater than I naught by 2 square root is I naught by c, and if that is not the case, this square root will be 2 I naught by c, and this can be simply written as the minimum value of I naught, this is I 2 by c. So, minimum value of I naught and 2 by 2 divided by c, now this gives you a guideline of how to choose I 2, we do not like the q rate to be limited to a small value because one current is smaller than the other.

So, the normal choice is to make I 2 to be exactly equal to I naught by 2, so the these two limits will go inside and this is common choice, now earlier I said that M 9 and M 10 contribute to noise and mismatch an output conductance and so on. Now, because they carry more current than other transistors, they will also have more g m, so more noise etcetera, etcetera.

It could try to reduce that by making this I 2 very small that is as small as possible, but if you do that the square root will be severely compromised, the reasonable value of I 2 is to make it equal to I naught by 2. So, what happens in that condition is that the quiescent current in M 1, M 2, M 5, M 6, M 7, M 8, M 3, M 4 will all be equal to I naught by 2, and the quiescent current here in M 9 and M 10 will be equal to I naught.

So, that is the q rate now, so far it look as though this new topology, where we use the p MOS common gate amplifier with n MOS differential pair, has only disadvantages it has more noise more offset more output conductance and so on. It also has more power dissipation, because as you can see the total current is equal to I naught plus 2 I 2, we

have extra branches here, so the total current, which was originally I naught is now I naught plus two I 2.

If you make I 2 equal to I naught by 2, we will have a total current of two I naught exactly double, what we had for the simple differential pair as well as the telescopic cascade opamp. So, this topology looks like it has only disadvantages, but there is one aspect in which this is more advantageous compare to the other one, so that is what we will see now and that is the swing limit.

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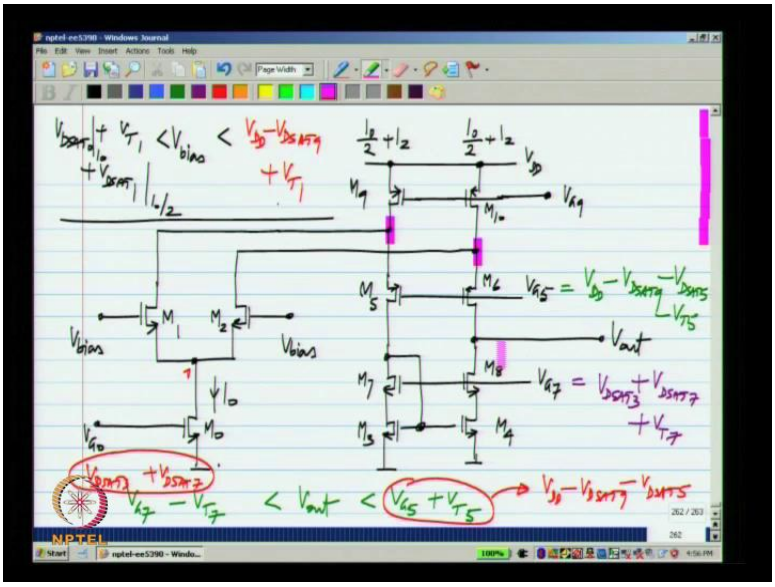

As before we have a swing limit on the output and swing limit on v bias, what is the limit on v bias, as v bias reduces the transistor M naught gets squeezed, and it will go into the triode region. So, v bias has to be at least equal to the familiar value of v d sat 0 plus v t 1 plus v d sat 1, v d sat one at the current of I naught by 2, and v d sat 0 at a current of I naught and what is the upper limit.

What happens to the transistors as v bias keeps on increasing, now we see here that these two nodes are bias startup fixed voltage, which is given by V G 5 plus v h d 5. In the quiescent condition current of I 2 flows through these transistors, and the voltages here is V G 5 plus v h d 5 at a current of I 2, so that is the drain voltage of M 1 and M 2.

Now, this v bias can go above that, but not by more than 1 v t, so the upper limit on v bias would be V G 5 plus v h d 5 plus v t 1, whatever that value is, now what would be

the normal voltage chosen for these points. Now, these transistors M 9 and M 10 must be in saturation, so whatever this voltage is that voltage plus v t 1 is the limit on a input, so we would like to maximize this voltage. Now, if you take this voltage very close to the supply voltage v d d, what happens is that M 9 and M 10 will enter the triode region we would not want that.

So, these two nodes will be bias that something like v d d minus v d sat 9, at whatever current it is carrying which is I naught by 2 plus I 2. It may be a little lower than this, but you would not make it much lower, because the these are fixed current sources and these voltages are also fixed. So, you keep this voltage to be the minimum required ,to keep the transistor in saturation region, so in that case the upper limit on v bias will be whatever these voltages plus v t 1, so it is v d d minus v d sat nine plus v t 1.

Now, typically the gate over triode voltages or the saturation voltage v d sat will be of the order of 150 200 or may be three 100 milli volts, and the threshold voltage is at least half a volt even in sub micron technologies. So, you see that this limit is actually more than v d d, so in this particular case the input common mode range can go all the way up to v d d. Now, it depends on the choice of the voltage at the drain of M 9 and M 10, but it can be easily arranged, so that the input common mode range includes the supply voltage v d d.

And what about the output range, if v out goes on reducing it will go below V G 7, and if it goes one threshold below V G 7 M 8 will enter triode region, so the lower limit is V G seven minus v t 7 which is same as v t 8. And the upper limit is as it goes on increasing transistor M 6 will enter triode region, if it goes above V G 5 by one threshold voltage, so the upper limit is V G 5 plus v t 5.

Now, this limits depend on the choice of V G 7 and V G 5, we would like to minimize V G 7 and maximize V G 5, so that will give us the maximum swing limit. Now, what is the maximum V G 5 as V G 5 goes on increasing, the source of M 5 and M 6 also follow V G 5, so M 9 and M 10 will enter triode region, if V G 5 is too high. So, the highest possible value of V G 5 is v d sat 9, so that this transistor is just in saturation plus v s d 5, which is v t 5 plus v d sat 5. If you do adjust this value at the highest value of v out, the highest possible value of v out will be nothing but, this plus v t 5.

Now, as V G 5 goes on increasing the source of M 5 and M 6 will go on increasing and M 9 and M 10 will enter the triode region, so the highest value is where M 9 and M 10 are biased at the edge of triode region, and you have one v h d across M 5 and M 6. So, across this we have v d sat and across, this we have v h d, so the maximum value of V G 5 is equal to v d d minus v d sat 9 minus v h d 5, which is basically v d sat 5 minus v t 5.

Now, if you set V G 5 to its highest possible value the upper swing limit, here will be this would be nothing, but v d d minus v d sat 9 minus v d sat 5, this is not surprising we have just one v d sat across M 9 and M 10, and 1 v d sat across M 6. So, this can go within 2 v d sat of v d d, similarly what is the lowest value of V G 7, when V G seven reduces the source of M 7 and M 8 hold down, and if they become too small M 3 and M 4 will enter triode region.

So, the smallest value of V G 7 would be to accommodate v d sat across this and V G s of M 8, so that will be v d sat three plus v s d 7, which is v d sat 7 plus v t 7. Now, if I substitute that over here what do I get I will have v d sat three plus v d sat 7, so just like on upper side all I have to do is to leave 1 v d sat for M 4 and 1 v d sat for M 8.

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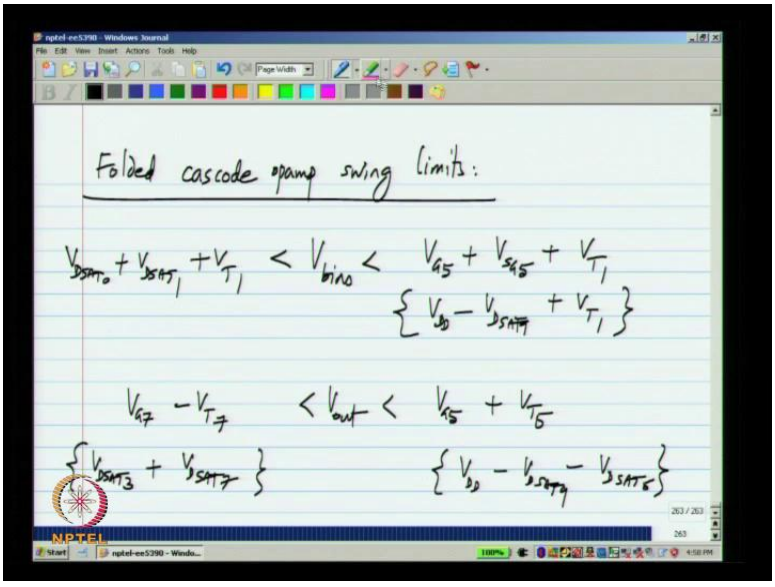

So, it can also come within two saturation voltages of the lower rail and ground, so swing limits of the folded cascode opamp are given by this is the range for the input common mode voltage. And this can be a maximum of v d d minus v d sat 9 plus v t 1 the lower limit is the same, as it is always been v d sat 0 plus v d sat 1 plus v t 1.

And the output voltage has a limit of V G 5 plus v t 5, and here V G 7 minus v t 7 and with the optimum values of V G 5 and V G 7 will have v d sat 3 plus v d sat 7 on the lower side. And v d d minus v d sat 9 minus v d sat 5 on the upper side, so the output can go with in two v d sat supplies. And this is the advantage of the telescopic cascode opamp the swing limits are a lot higher than in the differential pair, and also in the telescopic cascode opamp.

To the folded cascode opamp has a lot higher swing limit, and that is why it is used in many cases where the signals swing is important. And also another important to note is that in the telescopic cascode opamp, unlike in the other cases the input is applied to some devices and the output node is from a different device.

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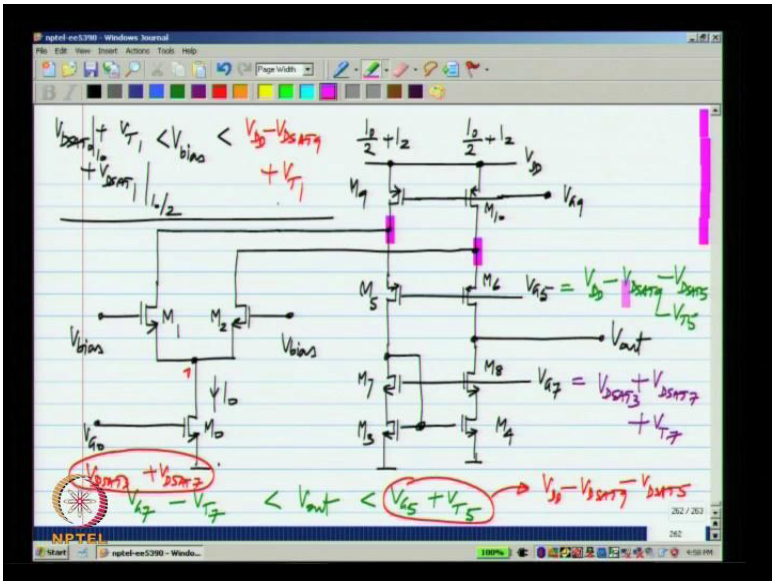

So, the constants on the input and output are more independent in this case than in the simple differential pair or the telescopic cascode, what we have done, so far is to analyze single stage opamps. What are known as single stage opamps, these are called single stage opamp, because there is a single trans conductor g m 1. As you recall the expression for trans conductance for all these three opamps that differential pair, telescopic and folded cascode g m 1, what is different is the output resistance and that gives you different value of d c gain.

Now the details of noise and offset are bi and large similar in the three opamps, except that in the folded coscode, you have extra devices, so you have extra noise and offset.

Now, the telescopic and folded the cascode opamps give you higher d c gain, that is why they are popular, and finally if you really want a high swing you go for the folded cascode, because it gives you the high swing that is possible.

Now, the square root is similar for all three opamps and because the telescopic and folded cascodes have more nodes compare to differential pair. They also have a more parasitic poles and 0's and this limits their speed to lower value compare to the differential pair. That is if you have more parasitic poles, you need to make sure that you are unity gain frequency is low enough, your integrator is, so, enough, so that in spite of all those parasitic delays you are stable.

That is your face margin is sufficient, so that is a quick summary of single stage opamp, now we know that single stage of opamps are not very useful, when you have resistive loads, because they have some trans conductance g m 1. And the telescopic and folded cascode have higher output resistance, but let us say we load all these three opamp with the given load resistance r l, which happens to be much smaller than the output resistance of the opamps.

Then all three will give same d c gain, so it is only with the capacitive load, that the telescopic cascode and folded cascode opamps give you higher gain than the differential pair. If you put a resistive load, and a typical resistive load as lower value, than the output resistance of transistors, all three will give equal gain and that is not useful. In order to have high d c gain with the resistive load, as we have discussed earlier, when we discuss the opamp at the control source level, we have to go to two stages.

So, instead of converting the output of the trans conductor into a voltage by passing, it through a capacitor directly. We should use a current controlled voltage source stage, the second stage across which we connect the integrating capacitor c and form the 2 stage opamp, and we will discuss the details of that in the next lecture.

Thank you.